Laboratory Manual

ELEN 474: VLSI Circuit Design

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Summer 2008

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Lab 0: Introduction

This laboratory complements the course ELEN 474: VLSI Circuit Design. The lab manual details basic CMOS analog integrated Circuit design, simulation, and testing techniques. Several tools from the Cadence Development System have been integrated into the lab to teach students the idea of computer aided design (CAD) and to make the analog VLSI experience more practical.

To fully appreciate the material in this lab course, the student should have a minimal background with the following computer systems, equipment, and circuit analysis techniques. Students should be familiar with the UNIX operating system. Previous experience using a SPICE-like circuit simulator is also important. This course does not explain the various SPICE analyses and assumes the student is capable of configuring the appropriate SPICE analysis to obtain the desired information from the circuit. Finally, the student should have general familiarity with active circuit "hand" analysis. All of these prerequisites are satisfied by having credit for ELEN 325 and ELEN 326.

The lab manual develops the concepts of analog integrated circuit design in a bottom-up approach. First, the basic devices of CMOS circuit design, the NMOS and PMOS transistors, are introduced and characterized. Then, one or more transistors are combined into a subcircuit such as a differential pair, current-mirror, or simple inverter and these small circuits are analyzed. Finally, these subcircuits are connected to form larger circuits such as operational transconductance amplifiers and operational amplifiers, and the idea of design methodologies is developed. Continuing with the bottom-up approach, these circuits can be combined to form systems such as filters or data converters (not currently covered in this course). The following figure illustrates the bottom-up approach used in the laboratory.

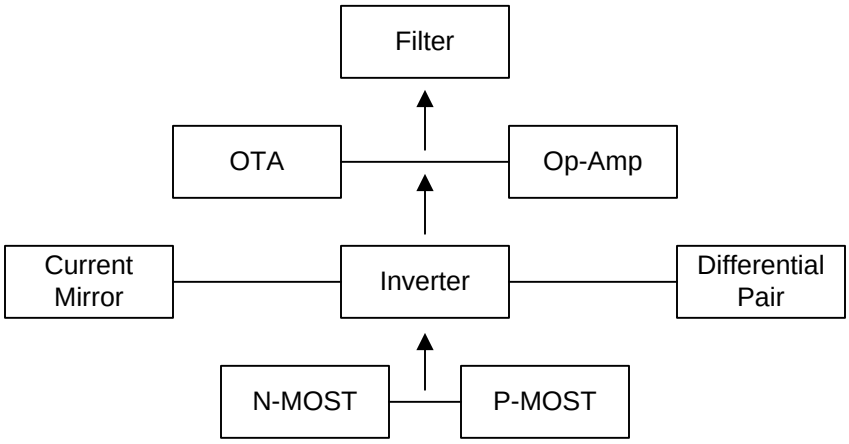


Figure 0-1: Bottom-Up Approach

The lab activities will generally be one week labs. However there will be some longer labs toward the end that will be two week labs. **Before the lab, the student should read through the lab description and perform the pre-lab exercises. Generally, the pre-lab exercises are the "hand" design for the circuit being studied.** During the lab students will perform circuit simulations to verify their hand calculations. Tweaking circuit parameters will usually need to be done since hand calculations will never be 100 % accurate. Also, the integrated circuit layout will be created. This will often require more time to do than 3 hour lab time that is allocated and will need to be finished outside of lab sometime before the next lab meeting.

Lab Report

Each team will submit one lab report for each lab. Reports are due at the beginning of class. Lab reports will consist of not more than three typed pages of single-spaced text. Be concise. **Late reports will not be accepted unless there is a valid excuse approved by instructor.**

- **TITLE PAGE**
- **DESCRIPTION**

  Include three or four sentences which describe the significant aspects of the lab. This section specifies problems or theory that will be investigated or solved. The description is a more detailed version of the objective.

- **DESIGN**

  Include circuit diagrams and design formulas/calculations. All circuit diagrams must be descriptively titled and labeled. A design formula/calculation must be given for each component. Do not derive equations.

- **RESULTS**

  This section usually consists of tables and SPICE plots.

- **DISCUSSION**

  This is the most important part of the lab report. Simply justify the difference between the theoretical and simulated values and answer and needed questions.

- **CONCLUSION**

  Two or three sentence summary of what the lab demonstrated. The conclusion usually responds to the problems specified in the DESCRIPTION section.

Lab 1: Introduction to Cadence

Objectives

Learn how to login on a UNIX station, perform basic UNIX tasks, and use the Cadence design system to simulate and layout simple circuits.

Introduction

This lab will introduce students to the computer system and software used throughout the lab course. First, students will learn how to login and logout of a Sun SparcStation. Next, basic operating system commands used to perform file management, printing, and various other tasks will be illustrated. Finally, students will be given an overview of the Cadence Development System.

In-class examples will demonstrate the creation of libraries, the construction of schematic symbols, the drafting of schematics, and the layout of simple transistors. The student will apply this knowledge to the creation of a CMOS inverter.

Logging-In/Logging-Out

In order to use the UNIX machines, you must first login to the system. As with the PC lab, enter the logon id and password at the prompts. Login using the logon ID and password obtained from the electrical engineering office. This is your account and all files stored in this area will be retained by the system after logging-out. Do not insert a floppy disk in the SparcStation. There is no need to attempt to make floppy disk back-ups of your data files.

Using the UNIX Operating System

Using the UNIX operating system is similar to using other operating systems such as DOS. UNIX commands are issued to the system by typing them in a “shell” or “xterm”. UNIX commands are case sensitive so be careful when issuing a command, usually they are given in lower-case.

The following list summarizes all the basic commands required to manage the data files you will be creating in this lab course. All UNIX commands are entered from the shell or xterm window. Do not use UNIX commands for modifying, deleting, or moving any Cadence data files.

Table 1-1: Common UNIX Commands

ls [–la]	Lists files in the current directory. ”l” lists with properties and “a” also lists hidden files (ones beginning with a “.”).
cd XXXX	Changes the current directory to XXXX.
cd ..	Changes the current directory back one level.
cp XXXX YYYY	Copies the file XXXX to YYYY.
mv XXXX YYYY	Move file XXXX to YYYY. Also used for rename
rm XXXX	Deletes the file XXXX
mkdir XXXX	Creates the directory XXXX.
lp -dXXXX YYYY	Prints the textfile or postscript file YYYY to the printer named XXXX, where XXXX can be either “ipszac” or “hpszac”.
gedit XXXX&	Starts the gedit text editor program and loads file XXXX.
icfb &	Starts the Cadence software.
top	Check available processes and memory usage.
quota –v	Check for disk space available
who|grep my_name	Display the terminal where I am connected

Note: The command “&” tells UNIX to execute the command and return the prompt to the active shell.

Cadence

The Cadence Development System consists of a bundle of software packages such as schematic editors, simulators, and layout editors. This software manages the development process for analog, digital, and mixed-mode circuits. In this course, we will strictly use the tools associated with analog circuit design.

All the Cadence design tools are managed by a software package called the Design Framework II. This program supervises a common database which holds all circuit information including schematics, layouts, and simulation data.

From the Design Framework II also known as the "framework", we can invoke a program called the Library Manager which governs the storage of circuit data. We can access libraries and the components of the libraries called cells.

Also, from the framework we can invoke the schematic entry editor called "Composer". Composer is used to draw circuit diagrams and draw circuit symbols.

A program called "Virtuoso" is used for creating integrated circuit layouts. The layout is used to create the masks which are used in the integrated circuit fabrication process.

Finally, circuit simulation is handled through an interface called "Analog Artist." This interface can be used to invoke various simulators including HSPICE, Spectre, and Verilog. We will be using the SpectreS simulator in this course.

Starting Cadence for the First Time

Before Cadence can be run, some basic configuration of your system needs to be done. We need to first edit our .cshrc file so that the correct version of cadence is run. You can do this with any text editor that you wish. If you are new to UNIX, I recommend a program called "gedit" since it is very similar to Notepad in Windows. From a terminal type:

```
cd
gedit .cshrc &
```

In the text editor that opens, you need to add the following two lines to the end of the file:

```
source /usr/local/bin/setup.ic5141
setenv CDK_DIR /baby/cadence/ic50/local
```

Save the changes you made to .cshrc and close the file. At the terminal type:

```
source .cshrc
```

Next we need to make a new directory called "cadence" which will hold all of our cadence files. This will also be the directory you need to run Cadence from in the future. In this folder we will also put two more configuration files, cds.lib and .cdsinit.

```
mkdir cadence
cd cadence
cp /baby/courses/474/cds.lib ~/cadence
cp /baby/courses/474/.cdsinit ~/cadence
```

Cadence should be ready to run now. From now on, you can launch Cadence when you login by typing

```
cd cadence
icfb &
```

This will load Cadence. The Command Interpreter Window (CIW) will now load as shown in Figure 1-1.

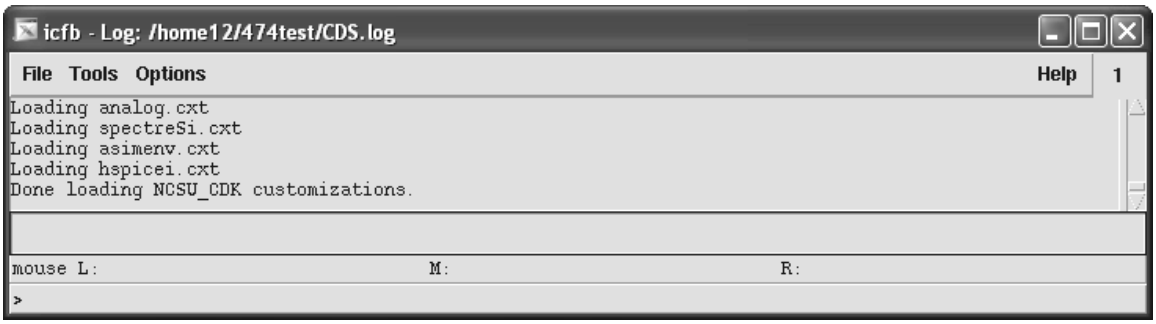


Figure 1-1: The Cadence CIW

Starting a Design

From the CIW select Tools → Library Manager to load the Library Manager (Figure 1-2). The Library Manager stores all designs in a hierarchal manner. A library is a collection of cells. For example, if you had a digital circuits library named Digital, it will have several cells included in it. These cells will be inverters, nand gates, nor gates, multiplexers, etc. Each cell has different views. These views will in general be things such as symbols, schematics, or layouts of each cell.

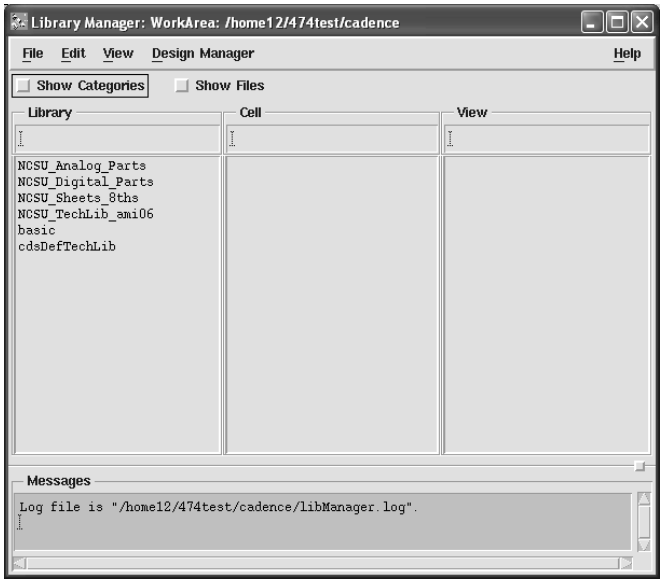


Figure 1-2: Library Manager

The first thing you need to do to start a design is create a library to store the cells you will be designing in this lab. Let's call this library "ee474". From the Library Manager select File → New → Library. Name the library "ee474" (without quotes) and select OK. In the window that appears select "Attach to an existing techfile" (Figure 1-3) and select OK. In the next window (Figure 1-4) make sure that NCSU_TechLib_ami06 is selected and select OK.

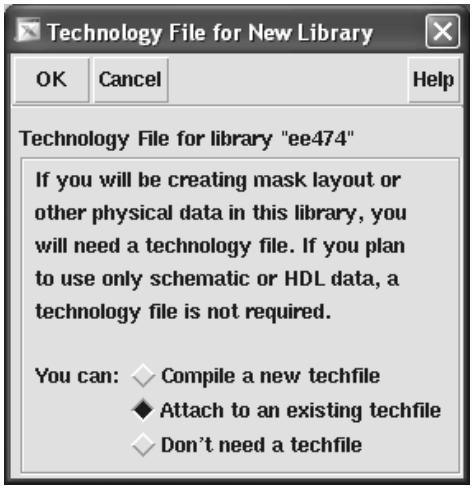


Figure 1-3: Attach to an existing techfile

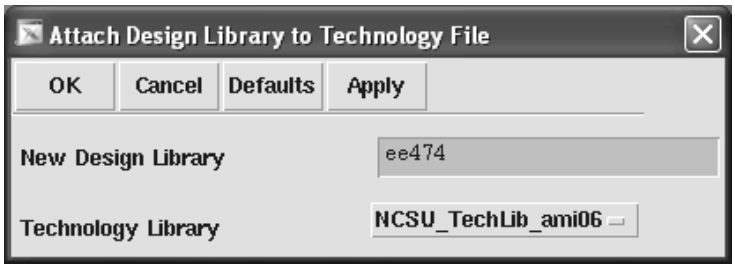


Figure 1-4: Attaching to a library to a technology file

Creating a Schematic

The first circuit we will design is a simple inverter. Select which library you want to put the cell into, in this case "ee474", and then File → New → Cell. Name your cell inverter. The tool you want to use here is Composer-Schematic as seen in Figure 1-5.

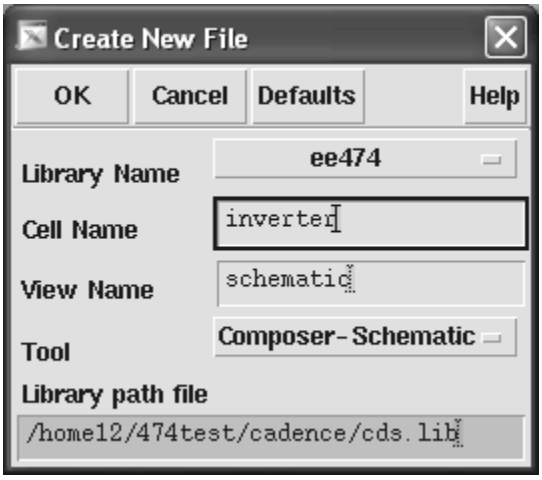


Figure 1-5: Creating a new cell view

After selecting OK, the schematic window opens. We wish to add two transistors so that we can make an inverter. To do this we need to add an instance. You can do this by either clicking Add → Instance or by pressing "i" on the keyboard. A window titled "Component Browser" should pop up. Make sure that the library NCSU_Analog_Parts is selected. Select N_Transistors and then nmos4. Go back to the schematic and select where you would like to add the NMOS transistor. Go back to the Component Browser and select P_transistors and then pmos4. Add this transistor to your schematic. Hit ESC to exit the Add Instance mode.

Connect components together using wires. You can select Add → Wire or use the "w" hotkey.

Pins identify the inputs and outputs of the schematic. Click Add → Pin or use the "p" hotkey. Pin names and directions must be consistent between the symbol, schematic, and layout. The name uniquely identifies the pin while the direction indicates the usage of the pin. I recommend using the inputOutput direction for all pins.

To change the properties of a device use Edit → Properties → Objects or use the "q" hotkey. Try changing the width of the PMOS transistor from 1.5u to 3u. When finished, your schematic should resemble Figure 1-6.

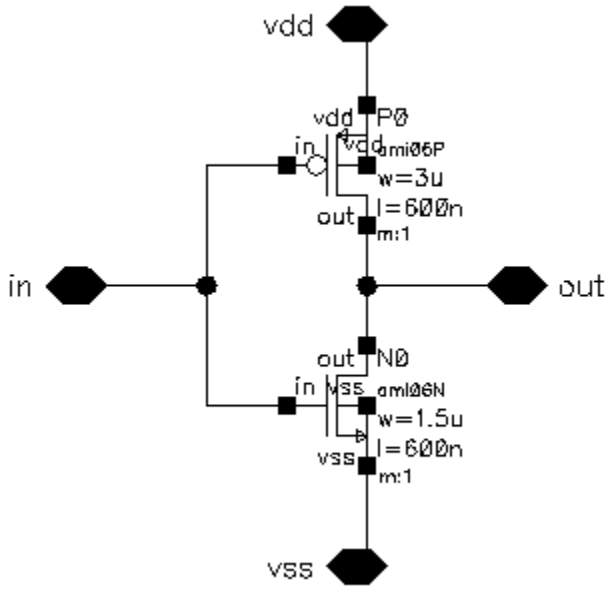


Figure 1-6: Inverter

Select Design → Check and Save to save your schematic and make sure that there are no errors or warnings.

Creating a Symbol

Without closing the schematic window select Design → Create Cellview → From Cellview. Make sure that "schematic" is selected in the "From View Name" field. Tool / Data Type needs to be "symbol". Select OK and then OK again on the next window.

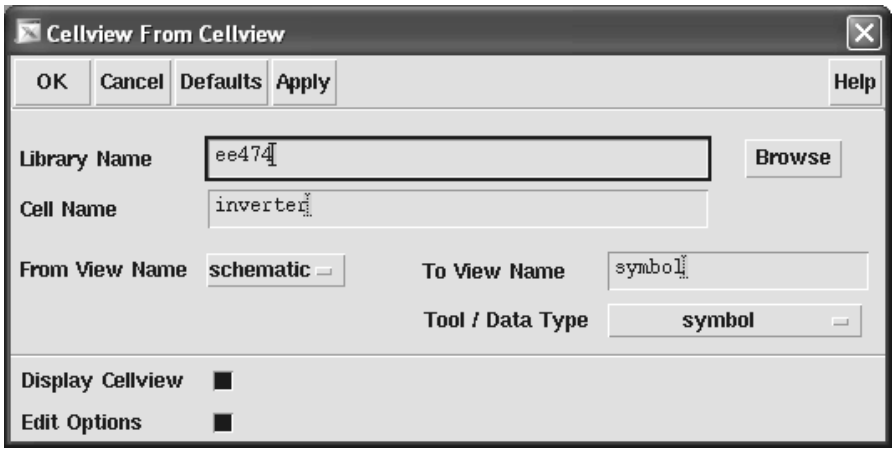


Figure 1-7: Create cellview from cellview

The symbol created should resemble the one in Figure 1-8. This does not resemble an inverter symbol at all. We can redraw it by deleting some lines and adding new ones. The final symbol should resemble Figure 1-9.

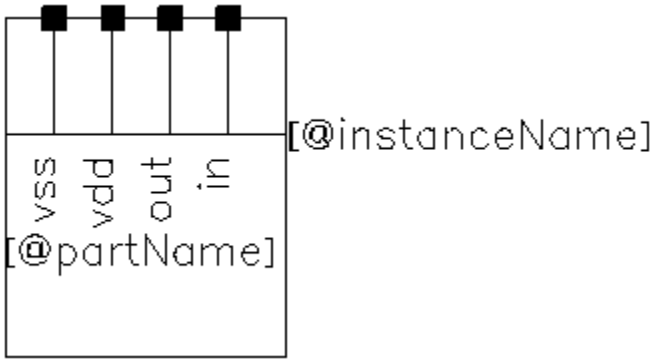


Figure 1-8: Default Symbol

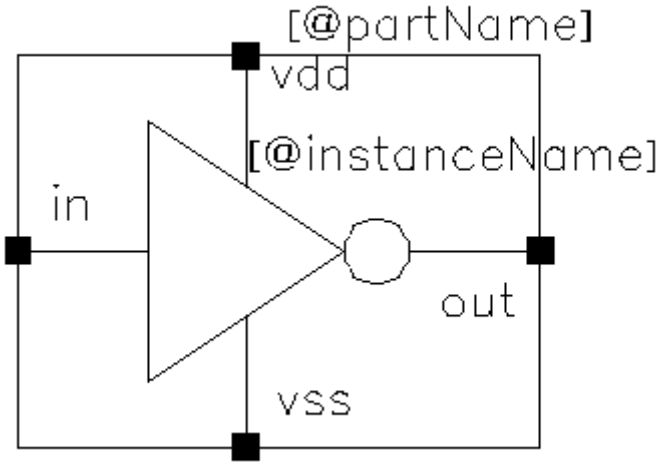


Figure 1-9: Final Inverter Symbol

Creating a Layout

After the schematic and symbol have been designed, it is time to move onto the layout of the circuit. From the library manager select File → New → Cell View. Layout is done using the tool named Virtuoso. Select Virtuoso as the toolname (Figure 1-10). After clicking OK, Virtuoso should open as well as the layer selection window (LSW, Figure 1-11).

The layout consists of rectangles, instances, and pins. A rectangle is used to create gate, diffusion, and metal regions for the transistor. The gate region is created by drawing a rectangle with poly (drw). The diffusions for a transistor are created by drawing a rectangle with the active (drw) layer. The intersection of poly and active regions defines the size (length and width) of the transistors. In order to define whether a

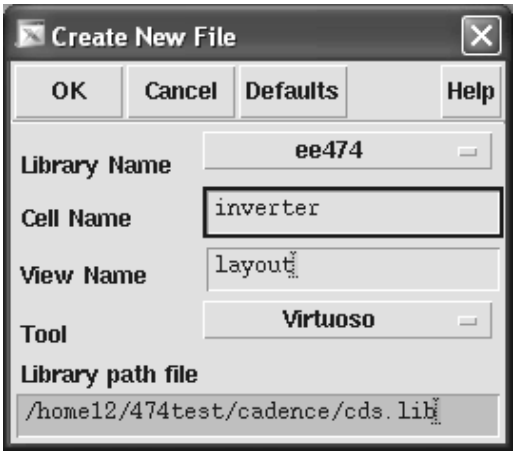


Figure 1-10: Creating a layout cell view

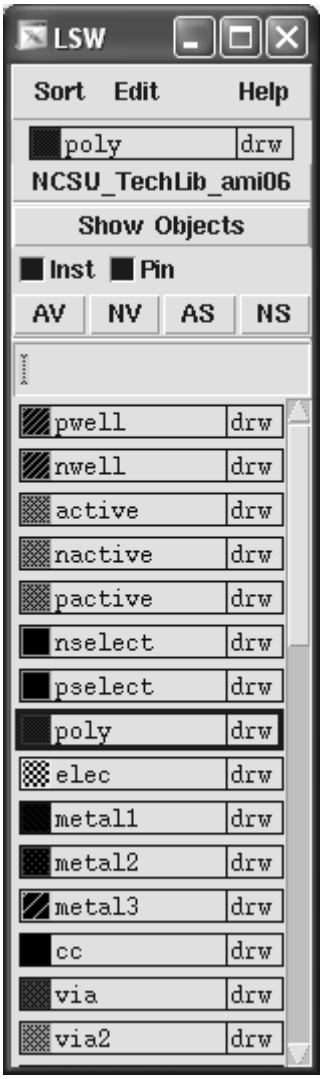


Figure 1-11: The LSW

transistor is NMOS or PMOS, nselect (drw) or pselect (drw) needs to surround the active area. The design rules describe minimum spacing and size requirements for various rectangles. Some basic design rules for this technology are shown in Figure 1-12.

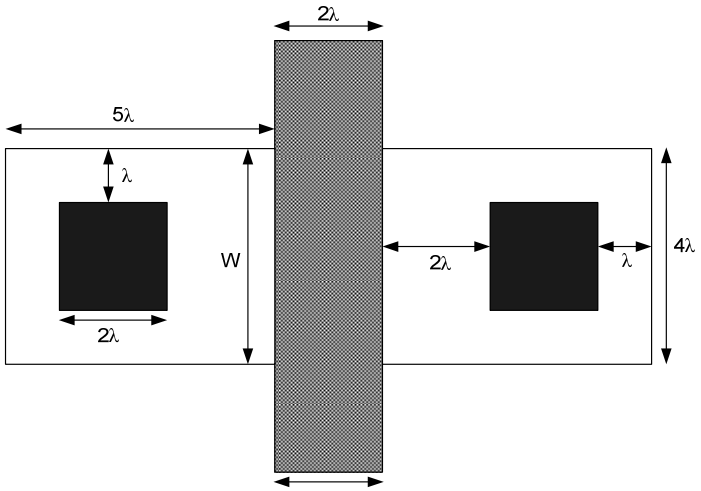


Figure 1-12: Basic design rules

Substrate contacts and vias between layers of metal can be drawn by hand, be added by selecting Create → Contact, or by using the "o" hotkey.

To add a pin, select Create → Pin. "Terminal Name" should be the name of the pin in the schematic. Make sure that the "Display Pin Name" option is selected so that the pin name will appear in the layout. "Pin Type" should be the same as the metal layer that it is connecting to.

After completing the above steps, you should obtain a layout of the inverter which resembles Figure 1-13.

After the layout is done, several steps have to be followed to insure that the layout is correct. These steps involve performing the following analysis:

Table 1-2: Post layout steps

DRC	Design Rule Check. Checks physical layout data against fabrication-specific rules. Typical checks include spacing, enclosure and overlap.
Extract	Device parameter and connectivity are extracted from the layout in order to perform ERC, Short Locator, LVS and post-layout simulation and analysis.
LVS	Layout Versus Schematic. Compares a physical layout design to the schematic from where it was designed.

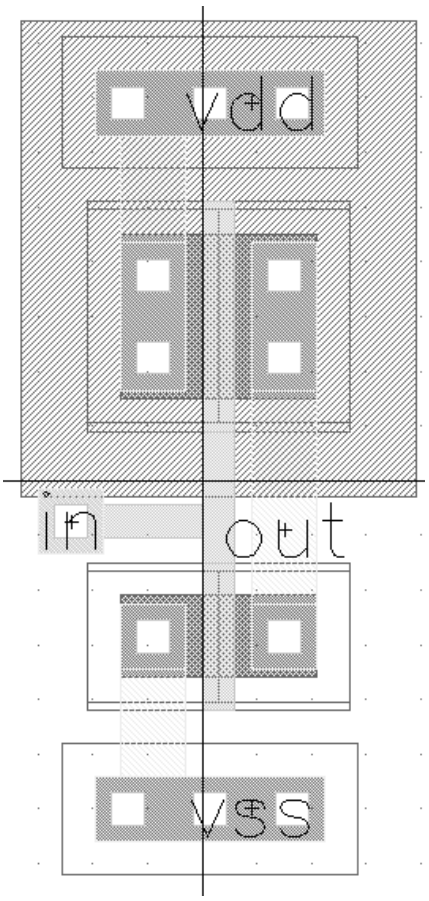


Figure 1-13: Inverter layout

DRC

To run DRC for the layout, select Verify → DRC. You do not need to make any modifications to the window that opens up. Select OK to run the DRC. The total number of errors will show up in the CIW as seen in Figure 1-14. Before going further we have to reduce the number of errors to 0.

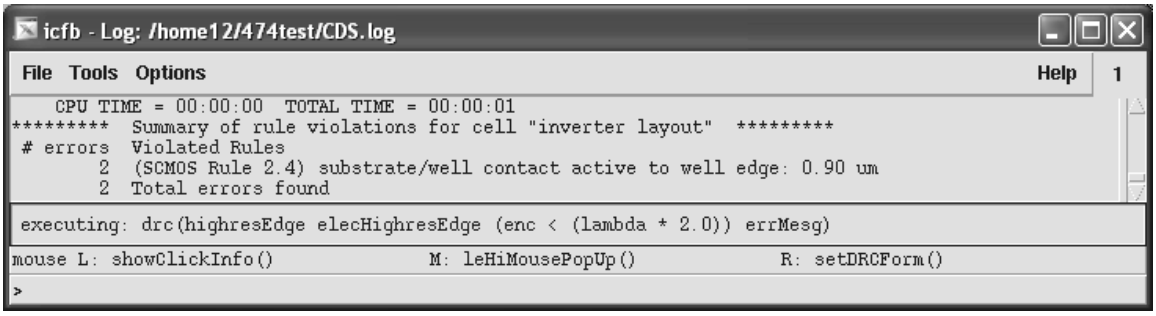


Figure 1-14: CIW showing DRC errors

The errors will usually show up in the layout as white lines. To have Cadence explain what the error is, select Verify → Markers → Explain. Click on one of the white lines, and Cadence will explain what design rule you broke. Adjust the layout to fix these errors and then rerun DRC until you have no design rule errors.

Extract

Once DRC is completed, you can now extract the layout. Select Verify → Extract. From this window, select "Set Switches". Highlight "Extract_Parasitic_Caps" and then click OK. Click OK again to extract the layout to make the extracted netlist.

LVS

The LVS window is shown in Figure 1-15. Make sure Rewiring, Device Fixing, and Terminals are selected under LVS Options. Click Run. A window should pop up once LVS has completed saying that the job succeeded. Click OK. From the LVS window select output. The output should have a line that says "The net-lists match." If they do not match, go back to the LVS window. Select Error Display to find out what your errors are. Adjust the layout to match, rerun DRC, Extract, and LVS until the netlists match.

Once the schematic and layout match, go back to the LVS window and click Build Analog and then OK.

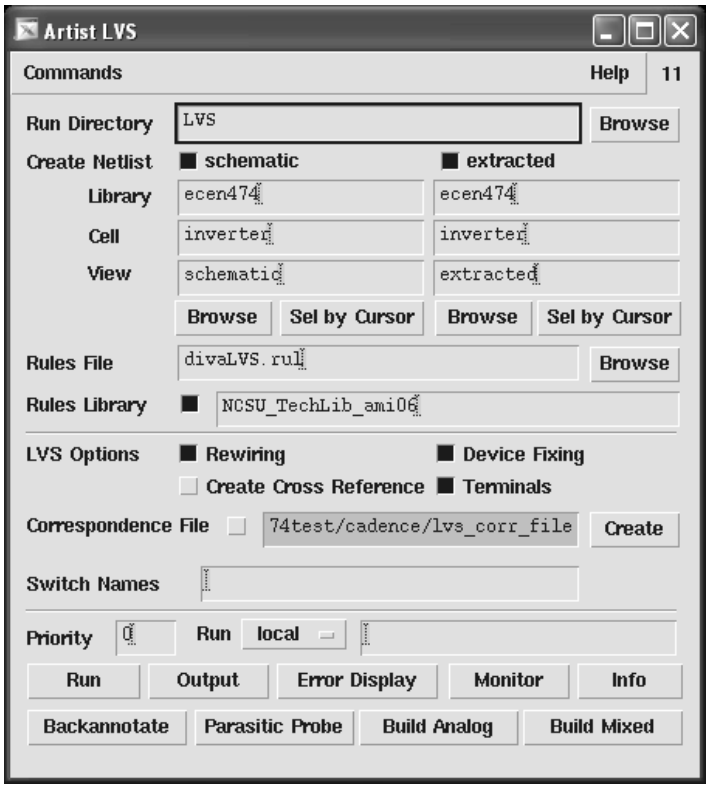


Figure 1-15: LVS window

Simulating the Schematic

To test the inverter, we need to create a new schematic cell view called "inverter_test". To simulate the design, add the inverter symbol, signal sources, power supplies, and loads as illustrated in Figure 1-16.

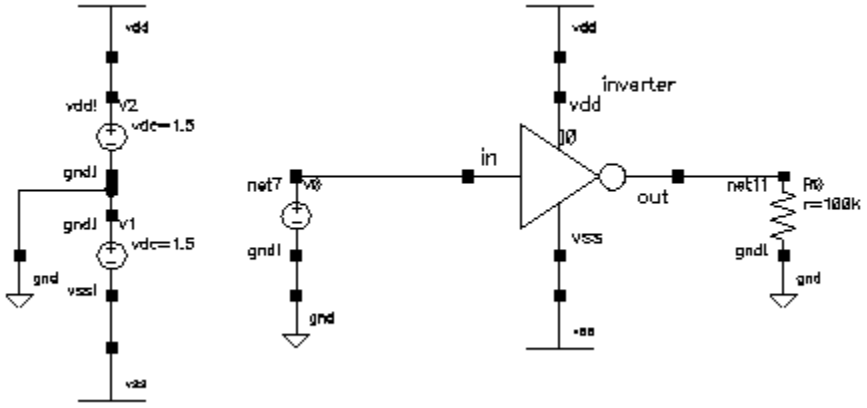


Figure 1-16: Inverter test schematic

Start the simulator environment by selecting Tools → Analog Environment. The simulator should appear in a few moments. Select Setup → Simulator/Directory/Host and verify that spectreS is the simulator.

Next we need to configure the environment to run our first simulation. In the Analog Environment window select Analyses → Choose. Select "dc" and then "Component Parameter". Select "Select Component" and then click on the desired voltage source in the schematic to sweep. In this case we want to sweep the input voltage source which is V0 in Figure 1-16. Select "dc" as the variable to sweep when the popup window opens. We wish to sweep the source from the negative supply to the positive supply, so input -1.5 into "Start" and 1.5 into "Stop". Select OK.

The simulator should now be configured to run the simulation. Select Simulation → Run or click on the green light in the bottom right corner. Once the simulation has completed, we can plot any outputs that we wish. To do this we use the calculator. To access the calculator, select Tools → Calculator in the Analog Environment.

Since our analysis that was ran was a dc sweep, select the "swept_dc" tab in the calculator. Click on the "vs" bubble and then click on the output node in the schematic. You can now plot the output as a function of the swept variable, which in this case is the inverter input, by clicking "Eval". Your output waveform should resemble Figure 1-17.

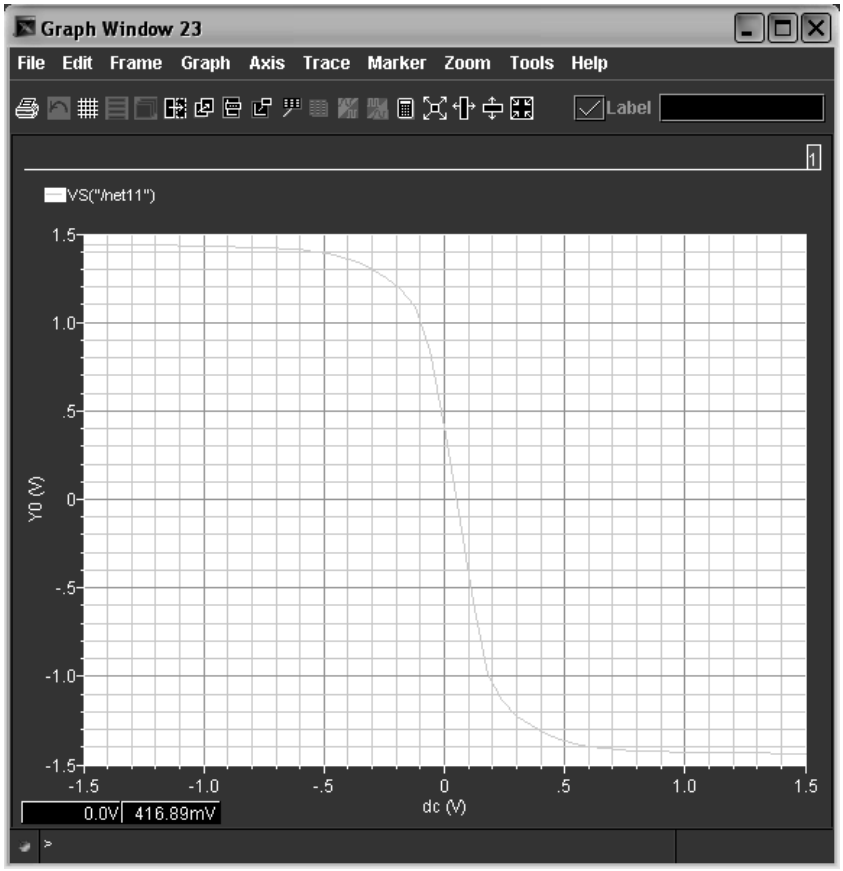


Figure 1-17: Inverter output plot

Simulating the Extracted Layout

To simulate the layout to verify that it operates as desired, you must do one thing in the Analog Environment before running simulations. You will still open the Analog Environment through the schematic window.

In the Analog Environment, select Setup → Environment. In the field labeled "Switch View List" add "analog_exracted" before "schematic" as shown in Figure 1-18. All other steps in simulation of the extracted view will now be the same as they were for simulating the schematic.

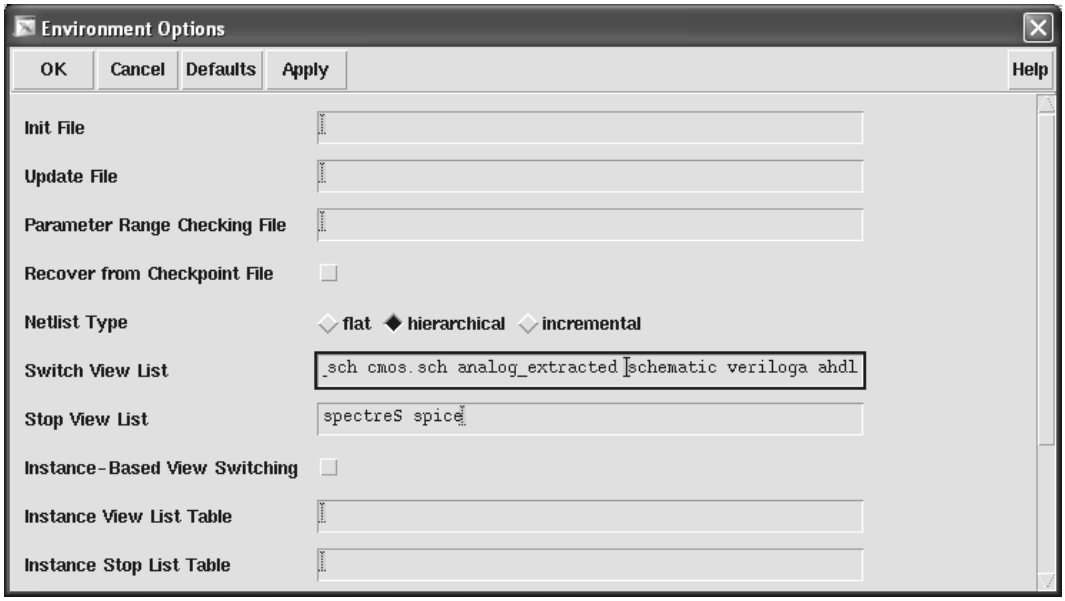


Figure 1-18: Adding extracted view to switch view list

Prelab

This prelab exercise is to be done during the lab under supervision of the TA. Turn in print outs of the following with the lab report next week:

1) Inverter schematic

2) Inverter symbol

3) DC sweep output graph showing the inverter was simulated

4) Inverter layout

5) Copy of the LVS output file showing that the netlists match

Lab Report

No lab report is required this week other than the printouts listed in the Prelab section.

Lab 2: Layout Design

Objective

Learn techniques for successful integrated circuit layout design.

Introduction

In this lab you will learn in detail how to generate a simple transistor layout. Next, techniques will be developed for generating optimal layouts of wide transistors and matched transistors. Layout techniques for resistors and capacitors will also be illustrated. Finally, you will use all of these layout techniques to produce a two-stage opamp layout (Lab 3).

Layout Techniques

Transistors

In Lab 1 you learned how to layout small size transistors. Most analog designs will not be limited to these small width transistors, thus special layout techniques need to be learned to layout large width MOSFETS. Luckily, wide transistors can be broken into parallel combinations of small width transistors as seen in Figure 2-1. By doing this horizontal expansion technique for the wide transistor, the drain and source area can be reduced which decreases parasitic capacitance and resistance.

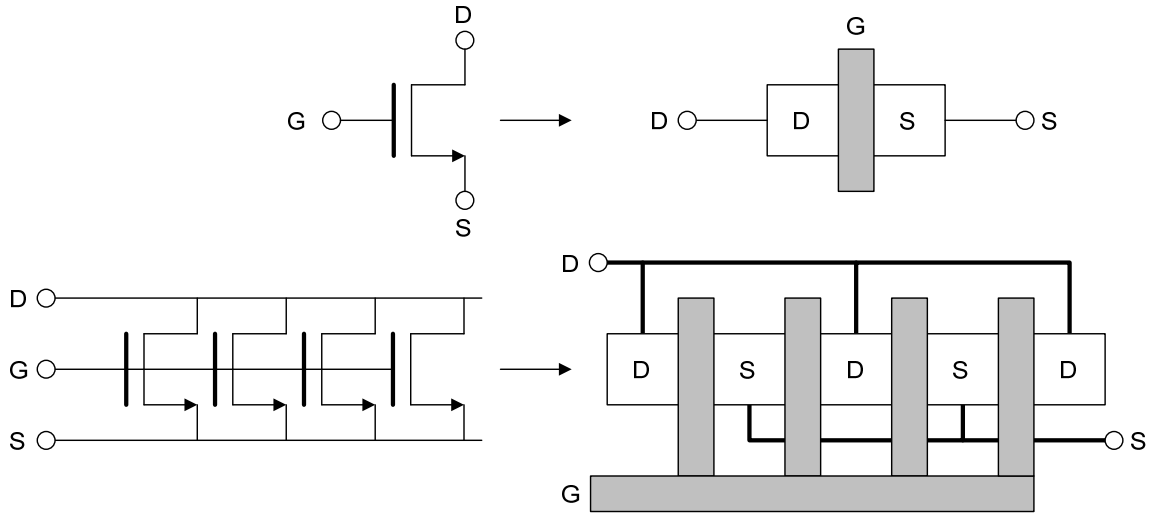


Figure 2-1: Wide MOS transistor layout

Another good layout technique is to use "dummy" transistors on both ends of a transistor layout. These dummy transistors insure that the etching and diffusion processes occur equally over all segments of the transistor layout.

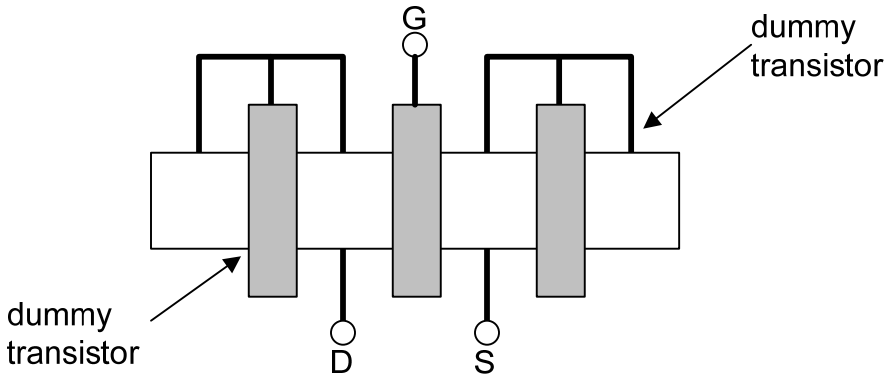


Figure 2-2: Dummy transistor layout

Notice the gate, drain, and source are connected together which keeps it from conducting any current. This shorted transistor is connected to the drain or source of the functional transistor. Another alternative for dummy transistors is to have the gate and source tied together.

When laying out any device the key is symmetry, especially when laying out fully-differential components. For matched devices, use interdigitized or common-centroid layout techniques. A matched device is one where two transistors need to have exactly the same geometries. Examples include current mirrors and differential pairs.

An interdigitized layout is shown in Figure 2-3. Notice that the two transistors have been split into smaller size devices and interleaved. This layout minimizes the effects of process variations on the parameters of the transistors.

The idea behind splitting a transistor up is to average the process parameter gradient over the area of the matched devices. For example, the process variation of KP and of the transconductance parameter on the wafer is characterized by a global variation and a local variation. Global variations appear as gradients on the wafer as in Figure 2-4. However, local variations describe the random change in the parameter from one point on the chip to another nearby point. By using layout techniques such as interdigitized and common-centroid, the process variation can hopefully be averaged out among the matched devices.

When laying out wider matched transistors the common-centroid layout may be a better choice. This layout technique is illustrated in Figure 2-5 for the case of 8 matched M1 and M2 transistors of a differential pair.

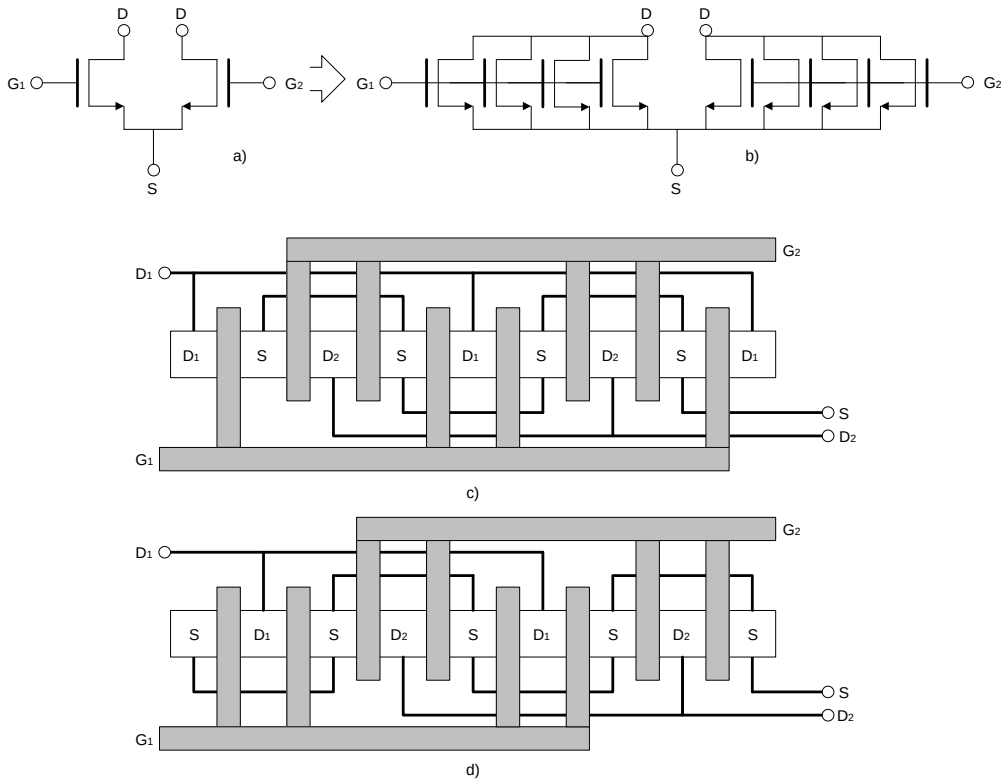


Figure 2-3: Interdigitized layout of a differential pair

a) Differential pair
b) Horizontal expansion
c) Interdigitized layout (Drain areas are different. Common centroid.)
d) Interdigitized layout (Drain areas are equal. Not common centroid.)

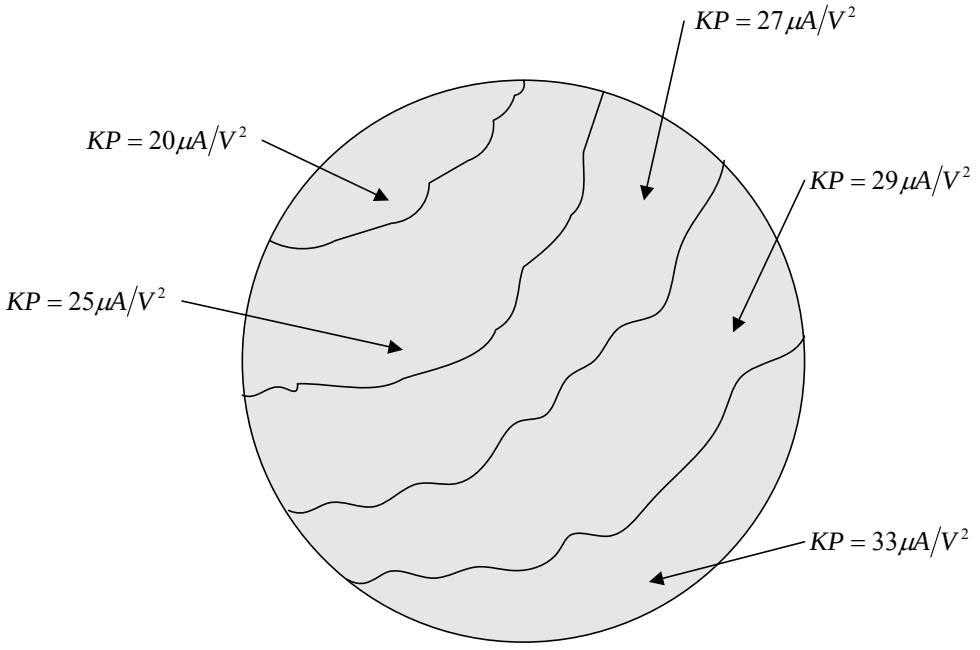


Figure 2-4: Gradient of KP on a wafer

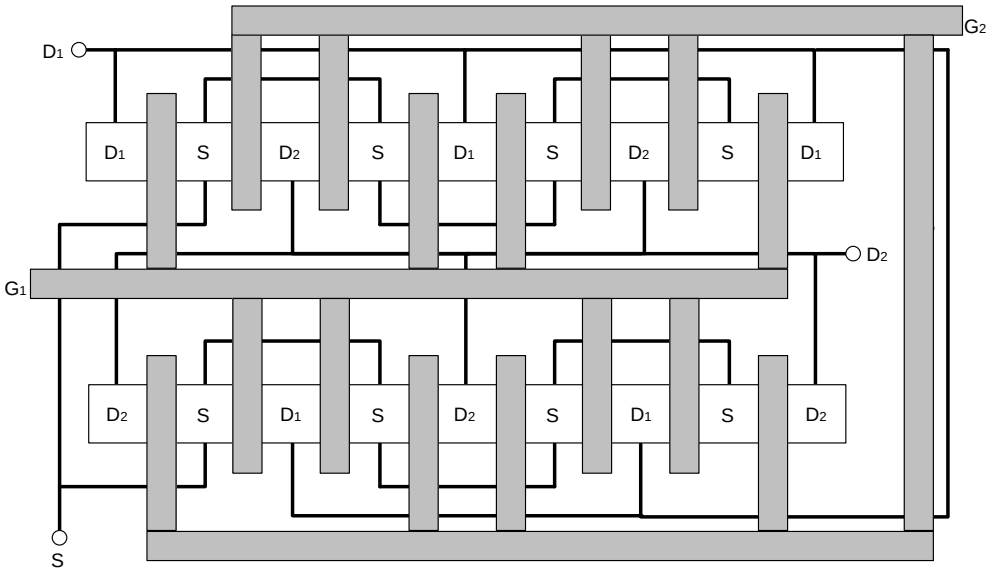


Figure 2-5: Common-centroid layout of a differential pair

The idea behind the common-centroid layout is to average linear processing gradients that affect the transistors' electrical properties. Common-centroid layouts should have the centroid (center of mass) of each transistor positioned at the same location. The following examples illustrate what is common-centroid and what is not common-centroid.

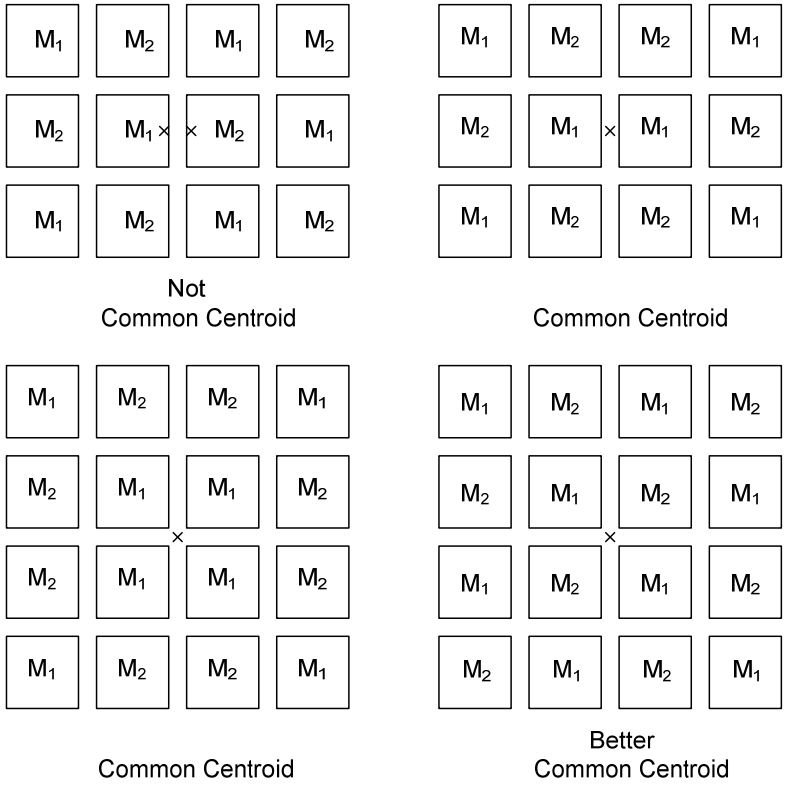


Figure 2-6: Common-centroid examples

Capacitors

Capacitors of various types can be fabricated on integrated circuits. A capacitor is formed when an insulator separates two conducting sheets. Two methods of forming capacitors are by using poly and poly2 (elec layer in LSW) as the capacitor plates.

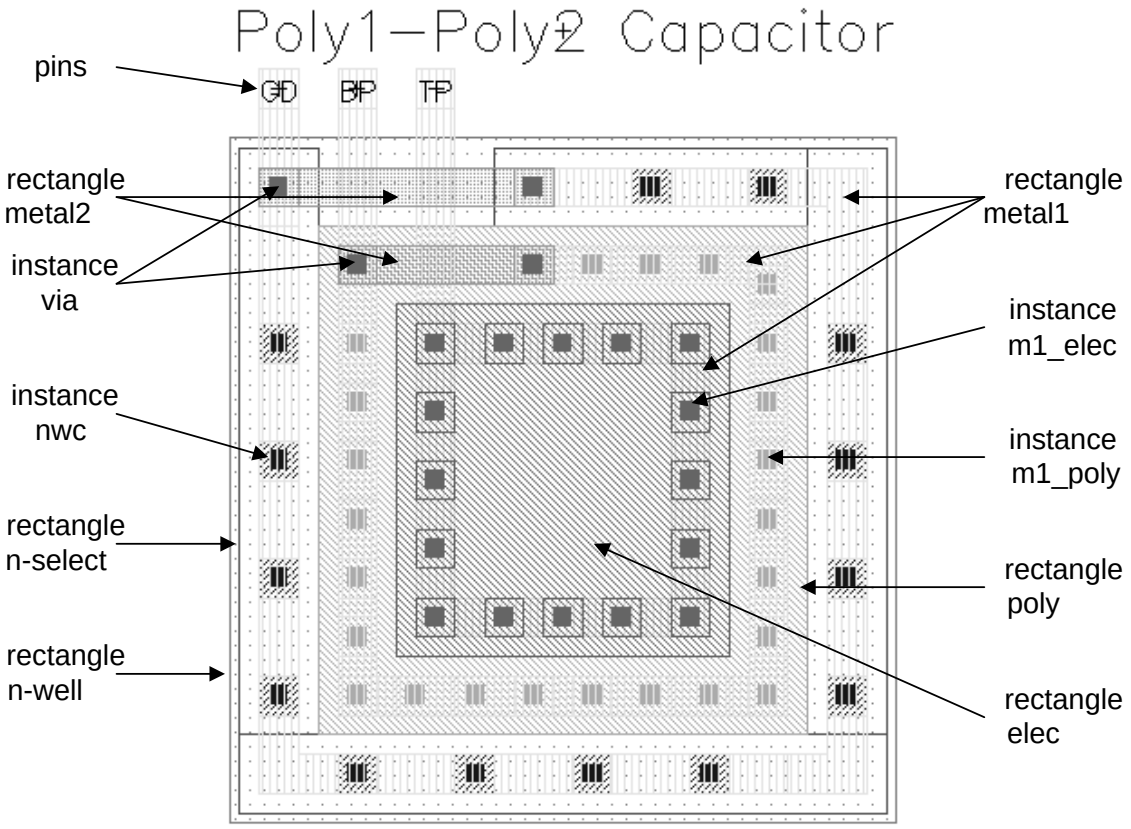


Figure 2-7: Poly-Poly2 capacitor layout

Figure 2-7 illustrates the layout of the poly-poly2 capacitor. The capacitor is formed by laying a second layer of polysilicon over the gate polysilicon. The area of the top plate (poly2) and the perimeter determine the capacitance by the following equation:

$$C = C_A \cdot A + C_F \cdot P$$

where:

C_A is the capacitance per unit area for the chosen capacitor type

A is the area of the top capacitor plate

C_F is the fringe capacitance per unit length for the chosen capacitor type for diffusion based capacitors

P is the perimeter of the top capacitor plate

For poly-poly2 capacitors, a parasitic capacitance between the substrate and poly can inject unwanted signals and noise into the circuit at the bottom plate of the capacitor.

To reduce this problem, put the capacitor in an N-well (for an N-well process) and connect the well to a "clean" ground. A ground plane (metal sheet connected to ground) can be used as a shield by covering all capacitors where possible.

For poly-diffusion capacitors, the bottom plate is placed in a special capacitor well to reduce noise injection and to prevent voltage signals from altering the capacitance. This produces a high quality linear capacitance.

To prevent the injection of noise from the substrate into the bottom plate of the capacitor, always be sure to connect it to a low impedance node such as ground or the output of an op-amp. Do not connect the bottom plate of a capacitor to an op-amp input. The substrate noise is due partly to power supply noise and connecting the bottom plate to the op-amp input allows direct injection of power supply noise into the op-amp input. The power supply is used to bias the substrate, so they are usually directly connected.

When designing circuits, sometimes desired circuit performance depends on the ratio of two capacitors. In such cases, it is important that two are more capacitors are properly matched. Divide each capacitor into many smaller "unit" capacitors. For matched devices this keeps the ratio of the areas and the ratios of the perimeters the same.

Like matched MOSFETS, the common-centroid layout technique can be employed for matched capacitors. Figure 2-8 gives a simplified layout floor plan for two equally sized, well-matched capacitors.

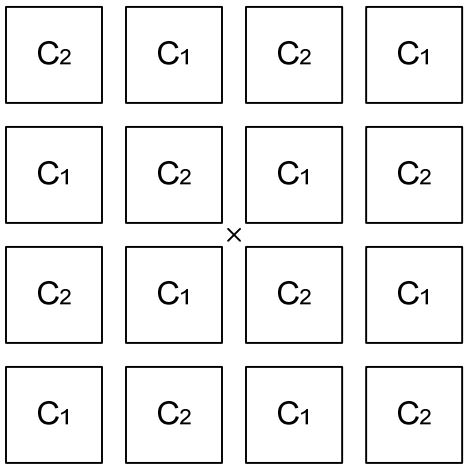


Figure 2-8: Common-centroid capacitor layout

The absolute and matching accuracy for various types of capacitors is given in the following table:

Capacitor	Absolute Accuracy	Matching Accuracy
Poly1-Poly2	±20%	±0.06%
Poly-Diffusion	±10%	±0.06%

Remember, the purpose of using the unit capacitor is to keep the ratio of the areas and perimeters the same. This prevents (delta) variations in capacitor dimensions from changing the capacitor ratio. If a non-integral number of unit capacitors are required, then

the perimeters and areas can still be kept the same. If the ratio of capacitors is $\frac{C_1}{C_2} = I + N$, where 1<N<2, then the unit capacitor has side length L_0 and the non-unit capacitor has side lengths L_1 and L_2. Use the following formulas to calculate the side lengths of the non-unit capacitor:

$$L_1 = L_0\left(N + \sqrt{N(N-1)}\right)$$

$$L_2 = N\frac{L_0^2}{L_1}$$

Keep the unit capacitor side length L_0 in the range from 10μm-25μm. Also, within the capacitor array, use a consistent method of routing lines between the capacitor segments. Each unit capacitor should be surrounded by similar routing lines. For capacitors near the edge of the array, use "dummy" routing lines. Also, be sure that parasitic capacitance formed by overlapping conductors is the same for the matched capacitors.

Large unmatched capacitors can be divided into smaller unit capacitors to reduce distributed effects caused by the relatively high resistivity polysilicon. This prevents a large capacitor which possesses considerable resistivity as well as capacitance from acting as a lossy transmission line.

Resistors

As for capacitors, many different types of resistors are available in integrated circuits. Other than active devices biased to act as resistors, we can use the inherent resistivity of the polysilicon or diffusions to create resistors. The following table shows the typical values of resistance for the AMI 0.5μm process that we will be using to design circuits.

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.9	109.5	22.3	1014	40.3	0.09	0.09	ohms/sq
Contact Resistance	64.7	169.6	15.6		25.9		0.90	ohms

The total resistance of a monolithic resistor is the sum of the contact resistance and the ohmic resistance of the diffusion material. The following formula can be used to estimate resistance for polysilicon and diffusion resistors:

$$R = R_S \cdot \frac{L}{W} + 2 \cdot R_C$$

where:

R_S is the resistance per square for the chosen resistor type

L is the length of the resistor

W is the width of the transistor

R_C is the contact resistance

Figure 2-9 shows a polysilicon resistor layout. The resistor is constructing by adding a strip of poly and then by adding poly contacts. Next the "res_id" layer is added which tells the extraction program that this is a resistor that needs to be included in the extracted netlist.

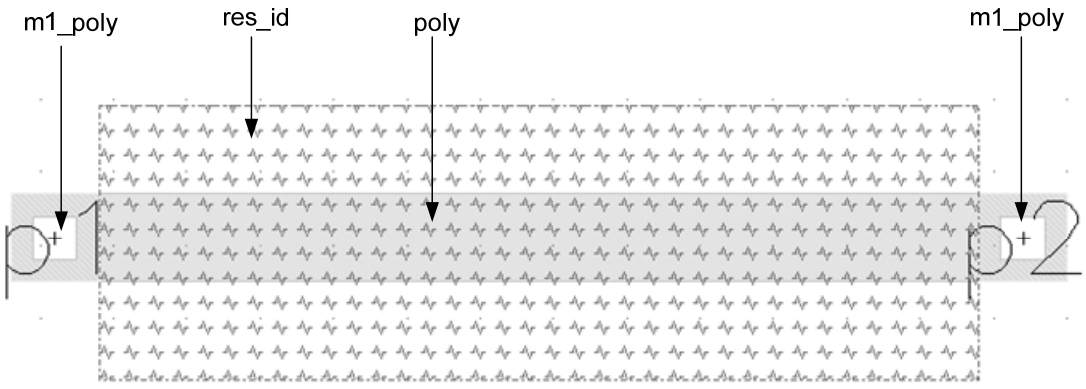


Figure 2-9: Poly resistor layout

If the circuit operation depends on the ratio of resistance, then good matching can be obtained by using interdigitized or common-centroid techniques. When matching resistors, be sure to keep device orientation and sizes the same. Also, since contacts contribute resistance, keep the contacts in the same ratio. An interdigitized layout of resistors is illustrated in Figure 2-10. Notice that the interconnecting metal is overlapping the resistor array and non-overlapping the resistor array in equal lengths for the two resistors.

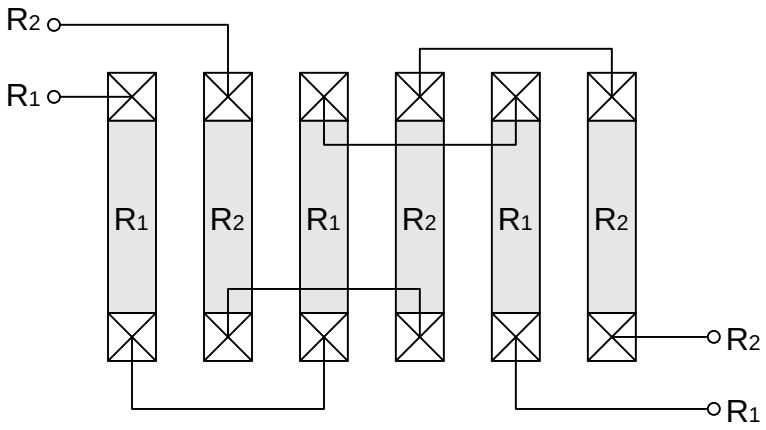


Figure 2-10: Interdigitized resistor layout

Prelab

Answer the following questions. No computer work is required for the prelab. The prelab is due at the beginning of class.

1) What are the absolute minimum dimensions of a transistor? Explain your reasoning. Remember to consider minimum contact size. Do we actually use this minimum size of do we use a slightly larger size for convenience.
2) Draw a common-centroid layout of a current mirror with equal size transistors of L = 0.6 μm and W = 19.2 μm. Use a finger length of 2.4 μm devices for each transistor segment. Remember to draw drain, source, gate, and bulk connections. Use dummy transistors and all other good layout techniques learned in the lab. Include a floor plan.
3) Design a common-centroid layout for a poly1-poly2 capacitor array. The capacitors have a ratio of 1.32:1. The capacitor array should consist of eight unit capacitors and one non-unit capacitor. Determine the form of the common-centroid layout and interconnect the capacitors. Each unit capacitance should have a separate top and bottom plate. Do not use a common bottom plate. Use the techniques described in the lab manual to give good matching. Also, give the size of the non-unit capacitor. The unit capacitor is 25 μm by 25 μm.
4) Design a matched polysilicon resistor pair to realize a resistance of 1200 Ω each. Remember to include contact resistance. Determine the approximate length and width of the diffusion. Use an interdigitized layout with six resistance segments. Use good layout techniques.

Lab

1. Practice good layout techniques by laying out the following:
    A) Current-mirror from prelab question #2
    B) Capacitor array from prelab question #3
    C) Matched resistors from prelab question #4
2. Include in the lab report
    A) Schematic printout
    B) Layout printout
    C) LVS printout showing that layout and schematic match

Lab 3: More Layout Techniques

Guard Rings

When laying out sensitive analog blocks, we need to help minimize the effect of substrate noise. One way to do this is with a guard ring. A guard ring is an array of substrate contacts which will then be connected to a clean supply (VSS or ground).

Figure 3-1 illustrates an example of a guard ring. This example shows a ring with a single contact. For more isolation, this ring can be made wider with more substrate contacts.

It is also important to note that the PMOS devices have an n-well contact ring surrounding them. This is good practice because it helps to act as an additional guard ring while also minimizing the possibility of latch up between the n-well and substrate.

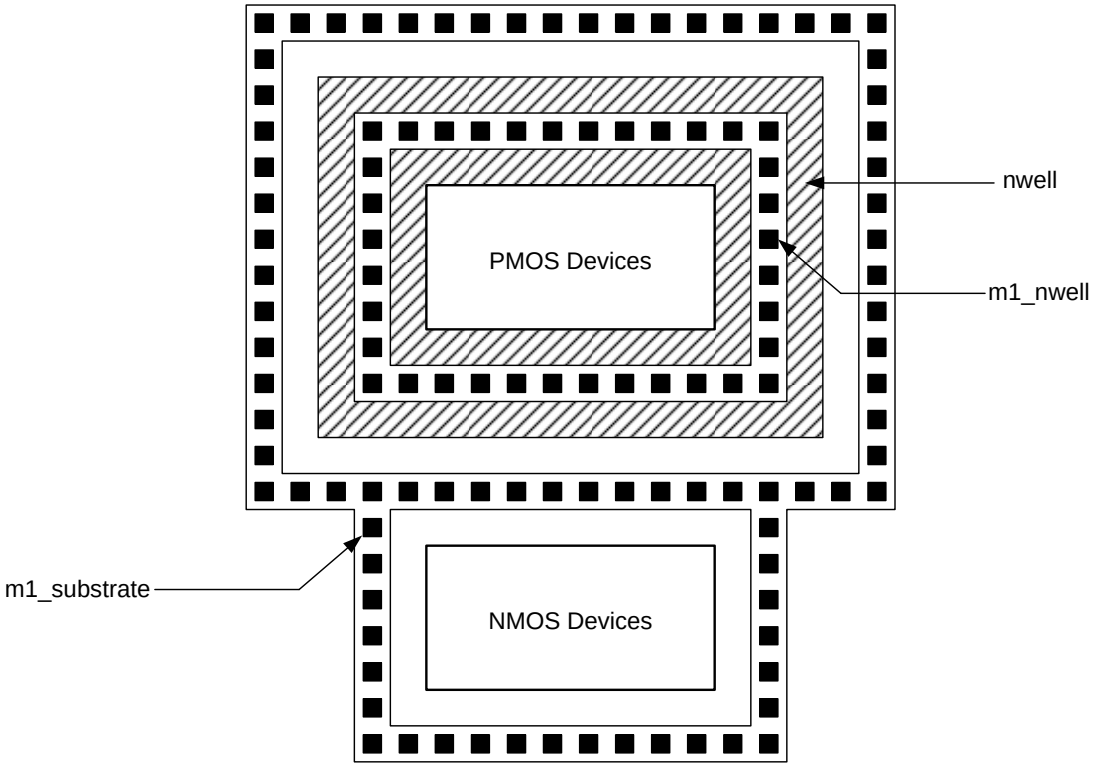


Figure 3-1: Guard ring illustration

Prelab

There is no prelab work required for this lab.

Lab

Use good layout techniques with guard rings to create a layout of the two-stage op-amp in Figure 3-2. Table 3-1 lists the transistor sizes for the op-amp. Figure 3-3 is a suggested floor plan to use. In this floor plan each transistor has a finger width of 2.4µm.

Include in the lab report:

A) Schematic printout

B) Layout printout

C) LVS printout showing that layout and schematic match

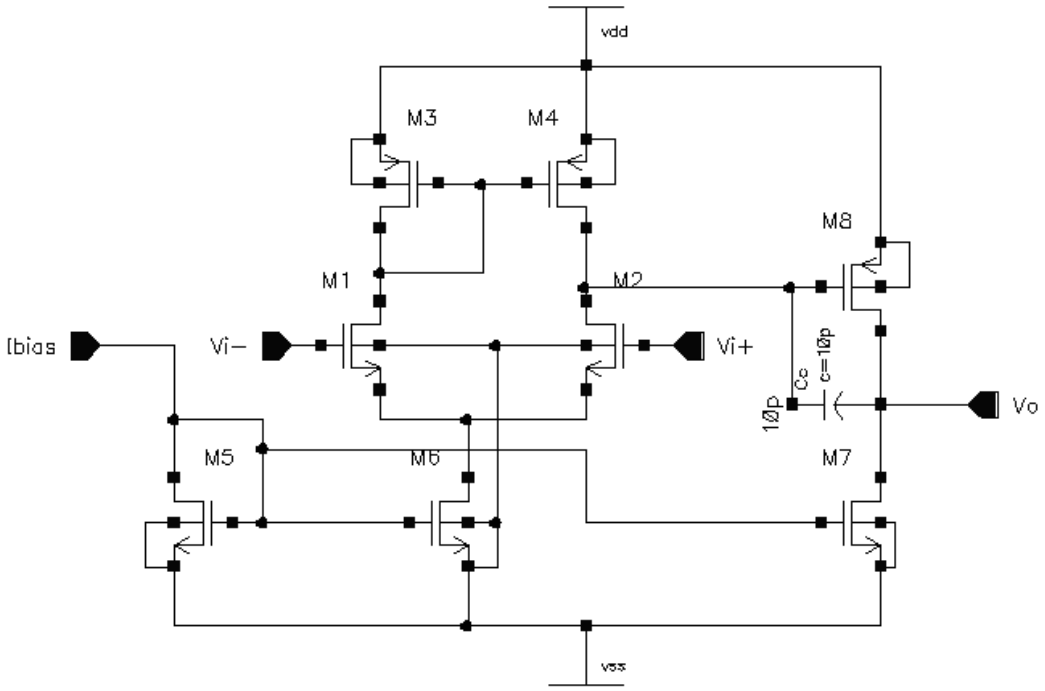


Figure 3-2: Two-Stage Op-Amp

Table 3-1: Transistor Sizes

MOSFET	W	L
M1	9.6u	600n
M2	9.6u	600n
M3	19.2u	600n
M4	19.2u	600n
M5	4.8u	600n
M6	9.6u	600n
M7	19.2u	600n
M8	76.8u	600n

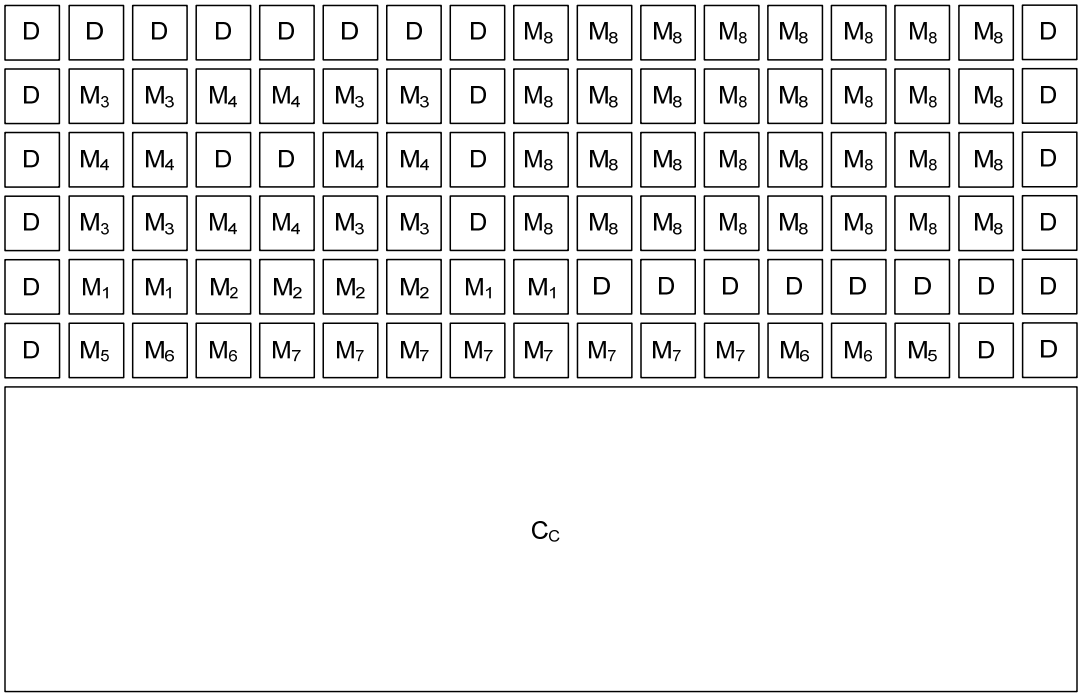


Figure 3-3: Floor plan for two-stage op-amp layout

Lab 4: MOS Device Characterization

Objective

Understand and measure transistor model parameters.

Introduction

In this lab you will review basic transistor operation and learn how the SPICE model parameters relate to the physical structure and electrical equations of the device. Then you will measure various electrical model parameters: V_{T0}, λ, KP, and γ.

Transistor Operation

MOS transistors are the fundamental devices of CMOS integrated circuits. The schematic symbols for an NMOS and PMOS transistor are illustrated in Figure 4-1 and Figure 4-2.

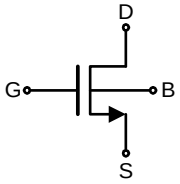


Figure 4-1: NMOS Transistor

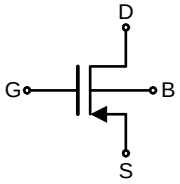


Figure 4-2: PMOS Transistor

A cross sectional view of an NMOS transistor is shown in Figure 4-3. When the potential difference between the source (S) and drain (D) is small (~ 0V), and a large potential (> V_{T0}) is applied between the gate (G) and source, the transistor will be operating in the linear or ohmic region. The positive gate potential causes electrons to gather below the surface of the substrate near the gate in a process called "inversion". This region of mobile charge forms a "channel" between the source and drain. The amount of charge is a function of the gate capacitance (C_{ox}) and the gate-to-source overdrive voltage:

$$Q_m = C_{ox}\left(V_{GS} - V_{T0}\right)$$

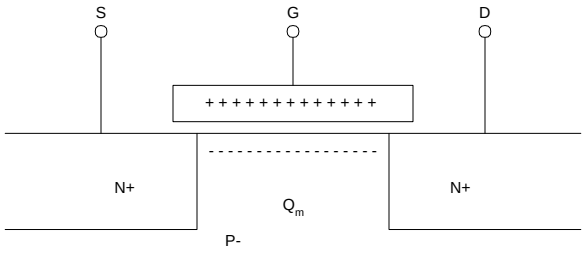


Figure 4-3: Cross-sectional view of an NMOS transistor

The term V_{T0} is the threshold voltage with zero source-bulk voltage. When the gate-to-source voltage (V_{GS}), exceeds this value, an inversion region is formed. Before reaching the inversion region, as the gate-to-source voltage is increased, the transistor passes through the accumulation region where holes are repelled from and electrons are attracted to the substrate region under the gate. Immediately before inversion, the transistor reaches the depletion region (weak-inversion) when the gate-to-source voltage is approximately equal to the threshold voltage. In this region a very small current flows.

In the linear region, the MOSFET acts as a voltage-controlled resistor. Resistance is determined by V_{GS}, V_{DS}, transistor size, and process parameters.

When the drain-to-source voltage (V_{DS}) is increased, the quantity and distribution of mobile charge carriers becomes a function of V_{DS} as well. Now the total charge is given by:

$$Q_m = C_{ox}\left(V_{GS} - V_T - V_{DS}\right)$$

The threshold voltage (now denoted as V_T) becomes a function of V_{DS}. The distribution of this charge is such that Q_m is greater near the source and less near the drain. To find the channel conductance, the charge must be recast as a function of position $Q_m(y)$ and integrated from the source to drain. Since the charge was a function of V_{DS}, the conductance depends on V_{DS}. The channel current becomes:

$$I_D = \mu_0 \cdot C_{ox} \cdot \frac{W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) \cdot V_{DS}$$

or

$$I_D = KP \cdot \frac{W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) \cdot V_{DS}$$

As V_{DS} increases, eventually the drain current saturates. That is, an increase in V_{DS} does not cause an increase in current. The saturation voltage depends on V_{GS} and is given by $V_{DS(sat)} = V_{GS} - V_T$. The equation for the drain current becomes:

$$I_D = \frac{1}{2} \cdot KP \cdot \frac{W}{L}\left(V_{GS} - V_T\right)^2$$

At this point the transistor is operating in the saturation region. This region is commonly used for amplification applications. In saturation, I_D actually depends weakly on V_{DS} through the parameter λ. Also, the threshold voltage depends on the bulk-to-source voltage (V_{BS}) through the parameter γ. A more accurate equation for the MOSFET in saturation is given by:

$$I_D = \frac{1}{2} \cdot KP \cdot \frac{W}{L}\left(V_{GS} - V_T\right)^2 \cdot \left(1 + \lambda \cdot V_{DS}\right)$$

In the equation above V_T includes the effects of V_{BS}.

When V_{GS} is less than the threshold voltage, the channel also conducts current. This region of operation is called weak-inversion or sub-threshold and is characterized by

an exponential relationship between V_{GS} and I_D. Also, when V_{GS} becomes very large the charge carrier's velocity no longer increases with the applied voltage. This region is known as saturation and has an I_D that depends linearly on V_{GS} as opposed to the squared relation shown above.

Figure 4-4 is a three-dimensional cross-sectional view of a MOSFET. Notice in the figure the overlap between the gate region and the active regions. The overlap forms parasitic capacitors C_{GS} and C_{GD}.

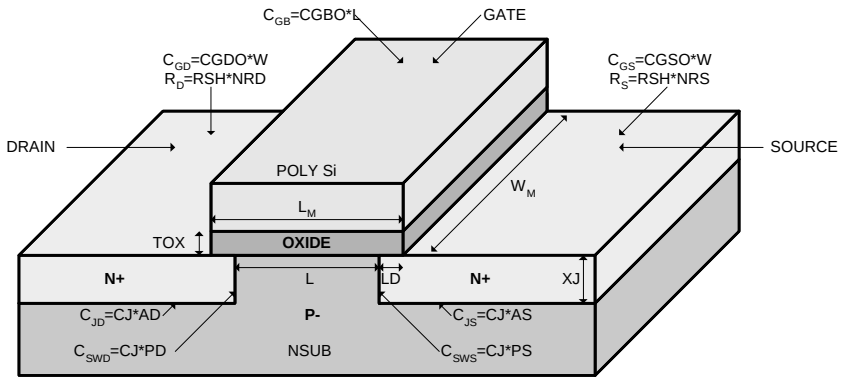


Figure 4-4: Physical structure of a MOSFET

The reverse-biased junctions between the active regions and the bulk form the parasitic capacitors C_{DB} and C_{SB}. The conductivity of the active regions forms the parasitic resistors R_D and R_S. A schematic symbol with the parasitic resistors and capacitors is illustrated in Figure 4-5.

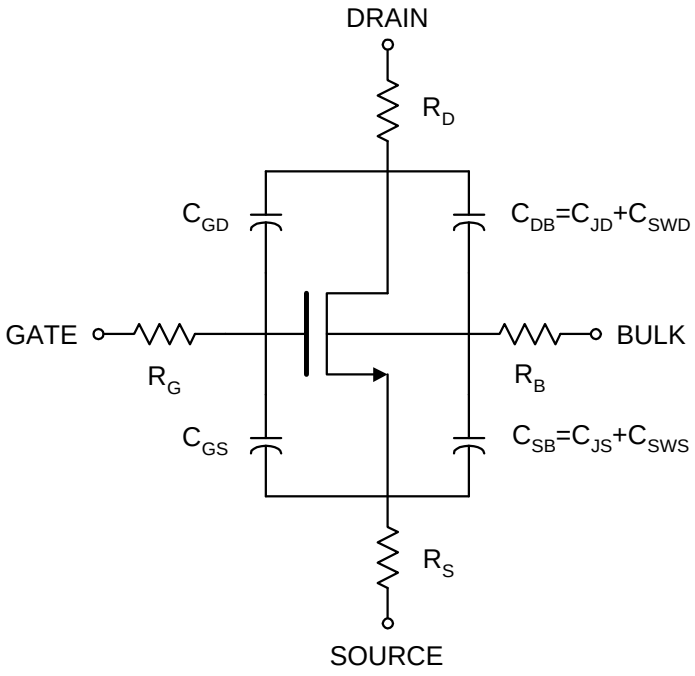


Figure 4-5: MOSFET parasitic resistors and capacitors

Device Characterization

To characterize the MOSFETs so that hand calculations can be done in the future, simulations need to be done to measure KP, V_{T0}, λ, and γ.

λ Measurement

To measure λ you need to do a DC sweep of V_{DS} and plot I_D as shown in Figure 4-6. Each curve represents a different V_{GS} value. Any one of these curves can be used to calculate λ. Make sure that V_{BS} is 0V for this simulation. The formula for calculating λ given two points on the saturation portion of a single curve is:

$$\lambda = \frac{I_{D2} - I_{D1}}{I_{D1} \cdot V_{DS2} - I_{D2} \cdot V_{DS1}}$$

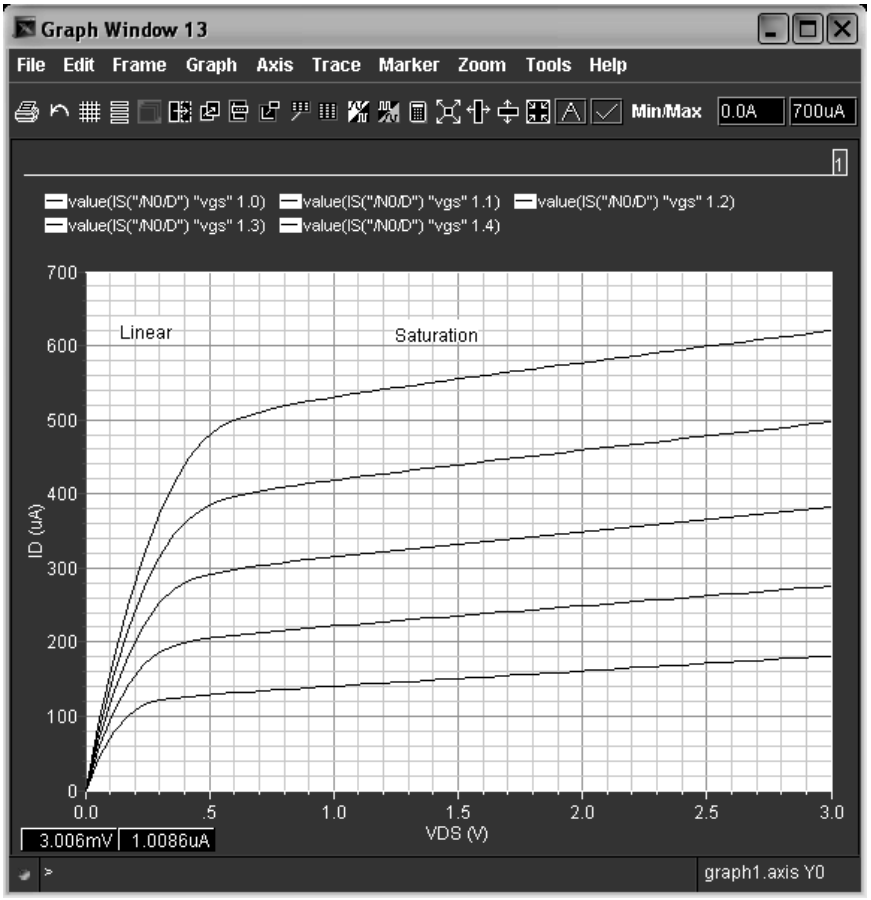


Figure 4-6: NMOS I-V charateristic plot

VT0 Measurement

V_{T0} can also be obtained from Figure 4-6. Using the saturation portion of two curves with equal V_{DS}, V_{T0} can be calculated as

$$V_{T0} = \frac{V_{GS1} - \sqrt{\frac{I_{D1}}{I_{D2}}} \cdot V_{GS2}}{1 - \sqrt{\frac{I_{D1}}{I_{D2}}}}$$

KP Measurement

Knowing λ and V_{T0}, KP can easily be found from the equation for MOSFET drain current in the saturation region. A little algebra gives that KP is

$$KP = \frac{2 \times I_D}{\frac{W}{L} \times (V_{GS} - V_{T0})^2 \times (1 + \lambda \times V_{DS})}$$

γ Measurement

To obtain γ you must first give the transistor a non-zero V_{BS}. Next calculate the new V_T using the same procedure that you used to obtain V_{T0}. γ is then given as

$$\gamma = \frac{V_T - V_{T0}}{\sqrt{\Phi_0 - V_{BS}} - \sqrt{\Phi_0}}$$

Φ_0 is the built-in potential of an open-circuit pn junction and can usually be approximated to be 0.9V.

Simulation

In order to obtain the I_D vs. V_{DS} vs. V_{GS} plot of Figure 4-6, you need to setup your schematic as shown in Figure 4-7. A simple DC sweep of V_{DS} needs to be performed, however to get multiple I-V curves, a parametric analysis needs to be run.

To do a parametric sweep on your V_{GS} voltage source, you need to setup a design variable in Cadence. First, modify the properties of the V_{GS} source. Instead of giving a constant DC voltage, make it a variable by naming it "vgs". In the Analog Environment window, select Variables → Edit. In the "Name" field type "vgs". You can give a value to the variable that Cadence will use for all simulations other than the parametric sweep. Once finished, select "Add" and then "OK".

To get to the parametric analysis simulation, go to the Analog Environment and select Tools → Parametric Analysis. In the "Variable Name" field add "vgs". Sweep from 1.0 to 1.4 with 5 steps. Choose Analysis → Start to run the parametric sweep. Once the simulation is finished, use the calculator to plot I_D.

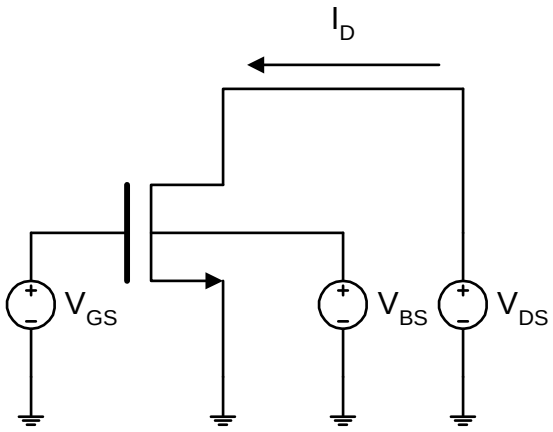


Figure 4-7: Simulation Test Setup

Prelab

No computer work is required for the prelab.

1) Derive the equations for the four electrical parameters given in the Device Characterization portion of the manual.

Lab

1) Use Cadence to produce I_D vs. V_{DS} vs. V_{GS} plots similar to Figure 4-6 for transistors of size 4.2/0.6 and 8.4/1.2.

2) Extract the four electrical parameters for both NMOS and PMOS transistors for both transistor sizes.

3) Compare the extracted parameters to the equivalent parameters given in the model file. Compute the percent difference and explain any discrepancies.

Note: To find the model file used, go to the Analog Environment window. Select Setup → Model Path. Once you know the model path, go to this directory and use a text editor to view the models ami06N.m and ami06P.m.

Lab 5: Current Mirrors

Objective

Design, simulate, layout, and test various current-mirror circuits.

Introduction

Current mirrors are fundamental building blocks of analog integrated circuits. Operational amplifiers, operational transconductance amplifiers, and biasing networks are examples of circuits that are composed of current mirrors. Analog integrated circuit implementation techniques such as current-mode and switched current use current mirrors as the basic circuit element. The design and layout of current mirrors is therefore an important aspect of successful analog circuit design.

In the simplest form, a current mirror is composed of two transistors as shown in Figure 5-1. Transistor M_1 is diode connected and acts as the low-impedance input of the current mirror. The drain of M_2 is the output of the current mirror.

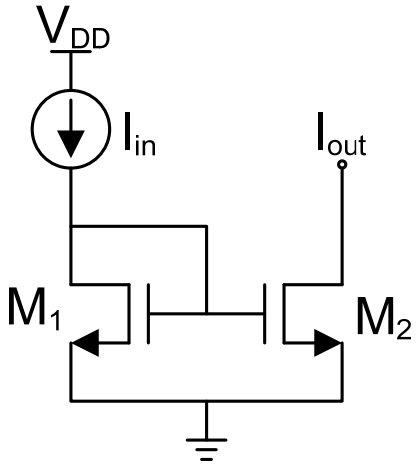


Figure 5-1: Simple current mirror

Since the gate-to-source voltage is the same for both transistors, then, according to the first-order MOSFET model, the drain currents will be equal. This assumes that the transistor sizes are equal as well as the process parameters.

A current mirror is used to mirror the input current into the output branch. A current (I_{in}) entering the diode connected transistor establishes a gate voltage (V_{GS}). The gate voltage causes I_{out} to flow through the output transistor. Notice that the input transistor will show a low small-signal resistance ($1/g_m$) and the output transistor will exhibit a high small-signal resistance (r_o).

If the ratio of the transistors is changed, then the current-mirror acts as a current amplifier. The current gain of the amplifier is given by:

$$A_i = \frac{\left(W_2 / L_2\right)}{\left(W_1 / L_1\right)}$$

The above analysis assumed ideal operation of the current mirrors meaning that the drain currents are independent of V_{DS}; however, due to channel length modulation we know this not to be true. The following equation, which you should be familiar with by now, illustrates the dependence of drain current on V_{DS}.

$$I_D = \frac{1}{2} \cdot KP \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T\right)^2 \cdot \left(1 + \lambda \cdot V_{DS}\right)$$

The excess current due to differences in V_{DS1} and V_{DS2} will cause a difference in I_{D1} and I_{D2}. To reduce "lambda" effects, the drain-to-source voltages of the two transistors need to be kept equal.

Another non-ideality of current mirrors is the limited range of V_{DS2}. Since M_1 remains in saturation for all input currents due to its diode connected configuration, M_2 needs to be kept in saturation to assume proper operation. If V_{DS2} drops too low, M_2 will enter the triode region, and the output current will be much less than what is wanted. The minimum output voltage required for the current mirror is sometimes referred to as the compliance voltage. For the simple current mirror, the compliance voltage is $V_{DS,sat2}$.

The ratio of the input to output currents is also process dependent. Because of this process dependency, good layout techniques such as interdigitized and common-centroid methods are used to layout current mirrors.

As previously mentioned, to obtain good matching between input and output currents, the drain-to-source voltages of M_1 and M_2 must be kept equal. One way to achieve this is by using a cascode current mirror which is pictured in Figure 5-2.

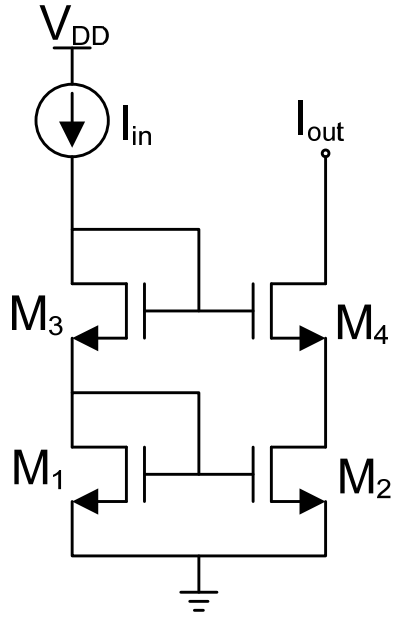


Figure 5-2: Cascode current mirror

Transistors M_1 and M_2 determine the ratio of the input and output currents. M_3 biases M_4 which is used to control the drain voltage of M_2. If designed correctly, V_{DS1} is approximately equal to V_{DS2}. The benefits of the cascode current mirror are better matching of output currents and larger output resistance. The disadvantage is that a larger compliance voltage is needed to keep both M_2 and M_4 in saturation. To find the compliance voltage we will use Figure 5-3.

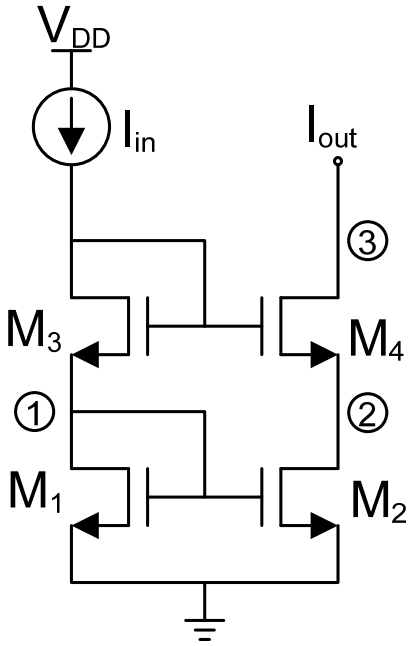


Figure 5-3: Cascode current mirror

Node 1: The voltage here is $V_{GS1} = V_T + V_{DS,sat1}$.

Node 2: For good matching between input and output currents, we want V_{DS1} and V_{DS2} to be equal. Thus, the voltage at node 2 is also $V_T + V_{DS,sat1}$.

Node 3: The minimum compliance voltage will be the minimum voltage to keep M3 and M4 in saturation. This will be $V_T + V_{DS,sat1} + V_{DS,sat2}$.

As you can see, adding the cascode transistor does not just increase the required compliance voltage by one $V_{DS,sat}$, it also increases it by a threshold voltage. If we have 200 mV overdrive voltages on all transistors with threshold voltages of 700 mV, the output voltage will have to be greater than 1.1 V. This makes cascode current mirrors not desirable for modern processes since the required supply voltage is already small.

In order to have the good current matching capabilities of the cascode current mirror, while not having such a large compliance voltage, we can use the low voltage cascode current mirror as pictured in Figure 5-4. If designed correctly, M_1 and M_2 will be biased such that they are at the edge of saturation, thus their $V_{DS} \approx V_{DS,sat}$. If this is the case then the compliance voltage drops to $V_{DS,sat2} + V_{DS,sat4}$. This is one whole threshold voltage less than the regular cascode current mirror of Figure 5-2. M_B will usually have a small W/L ratio, and should have a $V_{DS,sat} = V_{DS,sat1} + V_{DS,sat3}$.

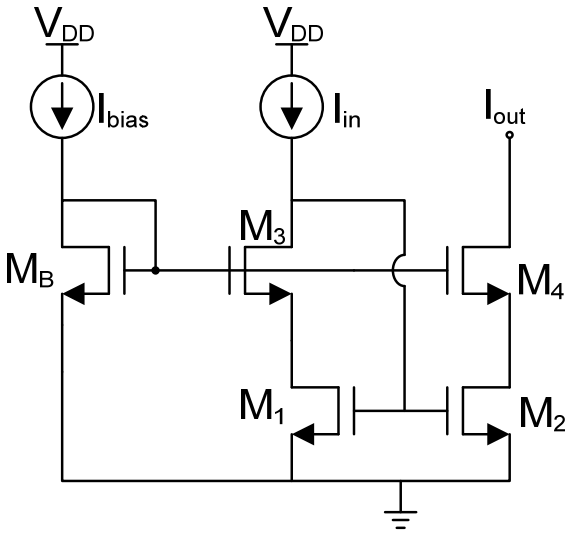


Figure 5-4: Low voltage cascode current mirror

Simulating Current Mirrors

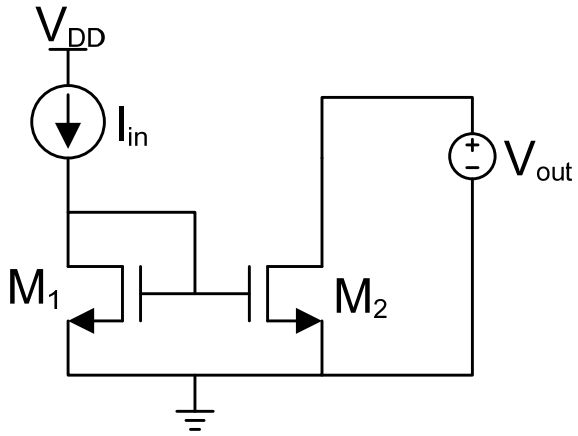


Figure 5-5: Current mirror test configuration

Once a current mirror has been designed (hand calculations), use the test configuration in Figure 5-5. I_{in} is whatever DC current you designed your current mirror to have. V_{out} is a DC source that will be varied in a DC sweep simulation. Plot I_{D2} vs. V_{out}, and you should get a plot which resembles Figure 5-6. The compliance voltage will be the point on the plots where I_{out} begins to change rapidly indicating the output transistor is entering the linear region of operation.

In order to find the output impedance an AC simulation needs to be run. First, give V_{out} a DC voltage greater than $V_{DS,sat}$ (say 1V) with an AC voltage of 1V. The output impedance will be the plot of the inverse of the AC drain current. An example is shown in Figure 5-7. In this example the output impedance is about 60 kΩ at low frequencies and then begins to decrease around 10 GHz.

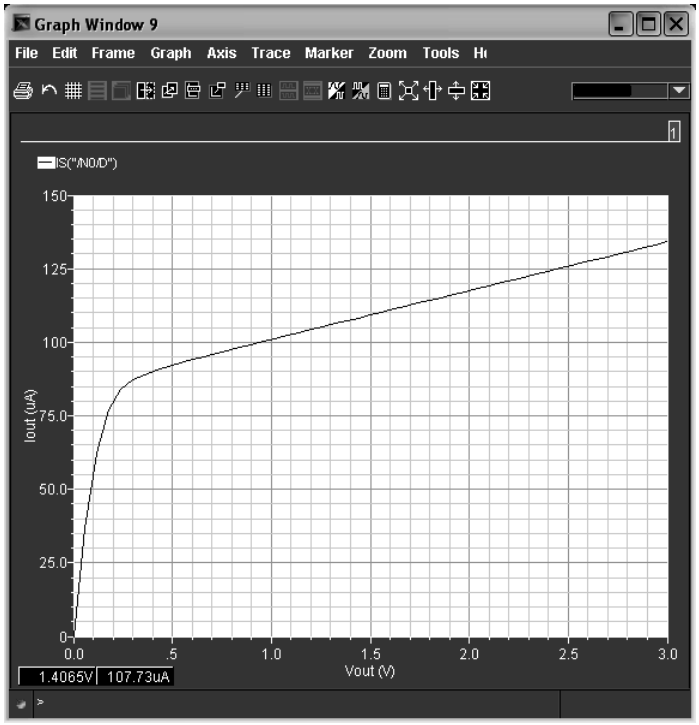


Figure 5-6: Current mirror simulation results

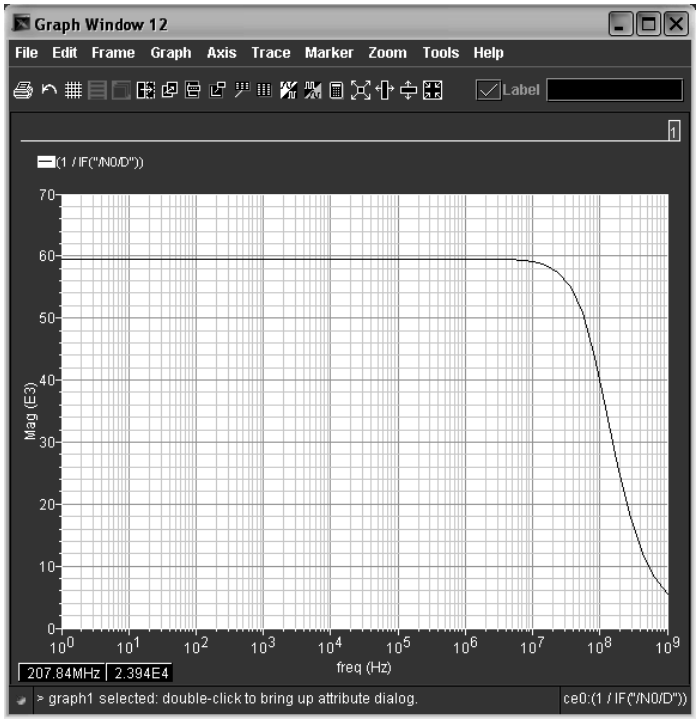


Figure 5-7: Current mirror output impedance

Prelab

The prelab exercise is due at the beginning of the lab period.

1) Make a table which lists the three current mirror topologies described in this lab. Rate each topology using good, medium, or bad for the following design considerations: R_{out}, accuracy, complexity, and compliance voltage.
2) Design a simple 1:1 current mirror that has a compliance voltage of 150 mV to 200 mV. The output current should be 100 μA. Determine W/L for each transistor and what the expected output impedance should be.
3) Design a low-voltage cascode current mirror with a 1:2 input current to output current ratio. The low frequency output impedance should be greater than 2 MΩ. Assume a 50 μA input current.

Lab

1) Simple current mirror
   A) Design in Cadence the simple current mirror from the prelab. If needed, modify the design so that it meets the given specifications.
   B) Generate the plots of Figure 5-6 and Figure 5-7 for this design. Determine the compliance voltage, low frequency output impedance, and comment on the accuracy.
   C) Layout the current mirror. Run post layout simulations. Include plots of both layout and schematic simulations in your lab report.
2) Low-voltage cascode current mirror
   A) Design in Cadence the low-voltage cascode current mirror from the prelab. If needed, modify the design so that it meets the given specifications.
   B) Generate the plots of Figure 5-6 and Figure 5-7 for this design. Determine the compliance voltage, low frequency output impedance, and comment on the accuracy.
   C) Layout the current mirror. Run post layout simulations. Include plots of both layout and schematic simulations in your lab report.
3) Be sure to include in your reports the LVS results showing that the layout matches the schematic.

Lab 6: Inverting Amplifiers

Objective

Design, simulate, and layout various inverting amplifiers.

Introduction

Inverting amplifiers are fundamental building blocks of electronic circuits. These amplifiers are used in a variety of circuit applications such as the gain stage of operational amplifiers and as the NOT gate in digital logic. Due to the utility of inverting amplifiers, learning the process of analyzing and designing these basic building blocks is important to successful circuit design.

Studying inverting amplifiers also gives us insight into basic circuit concepts such as small-signal frequency response and feedback. In this lab, the small-signal model of a generic inverting amplifier is analyzed while a generic design procedure is developed. Next, the lab manual presents advantages and disadvantages of several circuit structures. Finally, the students will design various inverting amplifiers by choosing a circuit structure and developing a design procedure.

The basic inverting amplifier is shown in Figure 6-1. The input signal V_{in} will contain an AC signal component as well as a DC component used to set the operating point:

$$v_{IN} = V_{BIAS} + v_{in}$$

Transistor M_1 is called the driver since the input signal controls the amplifier from this point. An ideal load will have infinite impedance. In the basic inverting amplifier circuit of Figure 6-1, the load is represented by an ideal current source.

The DC operating point of the circuit is determined by I_{BIAS} and V_{BIAS}. These currents and voltages determine the transistor's small-signal parameters and establish the quiescent output voltage.

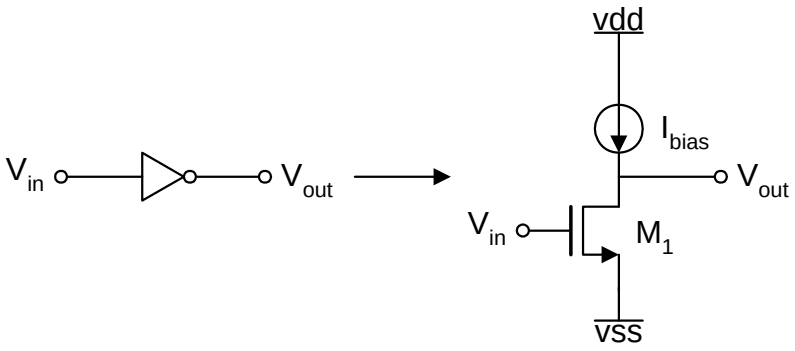


Figure 6-1: Basic inverting amplifier

The small-signal model for an inverting amplifier is given in Figure 6-2. The circuit consists of two connected nodes which will result in two poles and one zero. The resistance R_A represents the voltage source's resistance R_S and any resistance used to establish the DC biasing. The resistance R_B includes the load resistance and the small-signal output resistance of the driving transistor. The capacitance C_A includes source capacitance and the small-signal input capacitance of the transistor. Similarly, C_B represents the load capacitance and the small-signal output capacitance of the transistor. Finally, C_C consists of any external stray capacitance and internal capacitance between the drain and gate of the driving transistor.

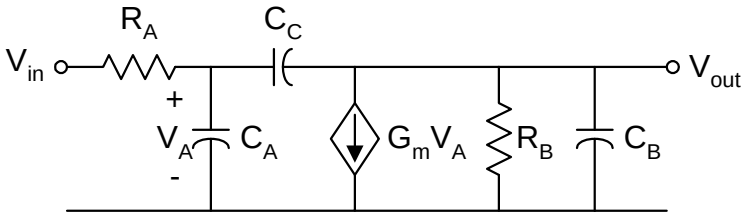


Figure 6-2: Generic inverting amplifier small-signal model

Using node voltage equations or mesh currents, the input-output transfer function for the inverting amplifier can be obtained by with some work. The transfer function for the generic amplifier of Figure 6-2 is given by:

$$H(s) = \frac{\frac{C_C}{R_A}\left(s - \frac{G_m}{C_C}\right)}{\left((C_A + C_C)(C_B + C_C) - C_C^2\right)s^2 + \left(\frac{C_A + C_C}{R_B} + \frac{C_B + C_C}{R_A} + G_m C_C\right)s + \frac{1}{R_A R_B}} \qquad (1)$$

This formula is too complicated to gain any useful insight as to how various resistors and capacitors affect the frequency response of the inverting amplifier. Various assumptions can be made to simplify (1). If we make the assumptions $C_B >> C_A$ and $C_C >> C_A$, then the transfer function can be simplified to:

$$H(s) = \frac{\frac{1}{R_A C_B}\left(s - \frac{G_m}{C_C}\right)}{s^2 + \left(\frac{1}{R_B C_B} + \frac{1}{R_A \frac{C_B C_C}{C_B + C_C}} + \frac{G_m}{C_B}\right)s + \frac{1}{R_A R_B C_B C_C}} \qquad (2)$$

This simplification is useful because C_C is generally a large transistor used to set the gain-bandwidth product, and the total load capacitance is generally larger than any parasitic input capacitances.

Next, we can simplify (2) in two different meaningful ways. The first way assumes R_A is small while the second assumes R_A is large. Using the first assumption

that R_A is small, we have $R_A << R_B$ and $R_A << \frac{1}{G_m}$. With this simplifying assumption, the transfer function in (2) becomes:

$$H(s) = \frac{\frac{1}{R_A C_B}\left(s - \frac{G_m}{C_C}\right)}{s^2 + \left(\frac{1}{R_A \frac{C_B C_C}{C_B + C_C}}\right)s + \frac{1}{R_A R_B C_B C_C}} \tag{3}$$

Also, if we assume the poles are far apart, that is $p_1 << p_2$, then we can use the following simplification when factoring:

$$D(s) = (s + p_1)(s + p_2) = s^2 + (p_1 + p_2)s + p_1 p_2 \approx s^2 + (p_2)s + p_1 p_2$$

The above simplification assumes a dominant pole exists. The dominant pole is the pole which is significantly closer to the origin than all the other poles. The non-dominant poles occur at a much greater frequency than the dominant poles. Using this simplification, the denominator in (3) can be factored as shown in (4). From (4) the poles can easily be determined.

$$H(s) = \frac{\frac{1}{R_A C_B}\left(s - \frac{G_m}{C_C}\right)}{\left(s + \frac{1}{(C_B + C_C)R_B}\right)\left(s + \frac{1}{R_A \frac{C_B C_C}{C_B + C_C}}\right)} \tag{4}$$

Now that the transfer function is in factored form, we can find the DC gain, poles, and zero for the case when C_A is small and R_A is small:

$$A_{V0} = -G_m R_B$$

$$p_1 = \frac{-1}{(C_B + C_C)R_B}$$

$$p_2 = \frac{-1}{R_A \frac{C_B C_C}{C_B + C_C}} \qquad (C_A \text{ is small, } R_A \text{ is small})$$

$$z = \frac{G_m}{C_C}$$

Assuming R_A is large, that is $R_A \approx R_B$ and $R_A >> \frac{1}{G_m}$. With this assumption, the transfer function given by (2) can be factored using the procedure given above:

$$H(s) = \frac{\frac{1}{R_A C_B}\left(s - \frac{G_m}{C_C}\right)}{\left(s + \frac{G_m}{C_B}\right)\left(s + \frac{1}{G_m R_A R_B C_C}\right)} \tag{5}$$

With this transfer function in factored form, we can find the DC gain, poles, and zero for the case when C_A is small and R_A is large:

$$A_{V0} = -G_m R_B$$

$$p_1 = \frac{-1}{G_m R_B C_C R_A} = \frac{-1}{|A_{V0}| C_C R_A}$$

$$p_2 = \frac{-G_m}{C_B} \qquad (C_A \text{ is small, } R_A \text{ is large})$$

$$z = \frac{G_m}{C_C}$$

Notice that the dominant pole has been shifted towards the origin. This is an example of Miller's Effect.

Next the frequency response of the two transfer functions derived above will be examined. For the case when R_A is small, the poles are greatly separated. Usually this system can be represented adequately by a first-order transfer function. The pole-zero diagram is shown in Figure 6-3. Since this system is first-order stability problems are less likely; however, the right-half plane zero will reduce phase margin. If stability becomes a problem, increase C_B relative to C_C.

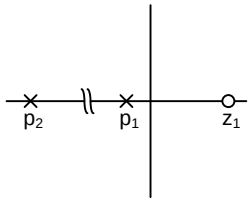


Figure 6-3: Pole-Zero diagram for small R_A

For the case when R_A is large, the system consists of a dominant pole, a non-dominant pole, and a right-half plane zero. Due to these three phase margin reducing components, careful circuit design is required to guarantee stability. The zero reduces phase margin and should be placed as far to the right as possible, while the non-dominant pole should be placed as far to the left as possible. Figure 6-4 illustrates the pole-zero diagram for this system.

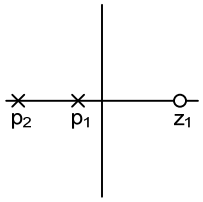


Figure 6-4: Pole-Zero diagram for large R_A

Two other simplifications are shown below. The first simplification assumes $C_A >> C_B$, $C_A >> C_C$, and $R_A \geq R_B$. This situation may occur when the inverter is used to amplify a signal from a capacitive transducer.

$$A_{V0} = -G_m R_B$$

$$p_1 = \frac{-1}{R_A \cdot C_A}$$

$$p_2 = \frac{-1}{R_B(C_B + C_C)} \qquad (C_A \text{ is large}, R_A \text{ is large})$$

$$z = \frac{G_m}{C_C}$$

The second set of equations assumes $C_B >> C_C$, $C_B >> C_A$, and $R_B \geq R_A$. These equations are useful if a wideband inverter is driving a capacitive load.

$$A_{V0} = -G_m R_B$$

$$p_1 = \frac{-1}{R_B \cdot C_B}$$

$$p_2 = \frac{-1}{R_A(C_A + C_C)} \qquad (C_B \text{ is large}, R_B \text{ is large})$$

$$z = \frac{G_m}{C_C}$$

Design Description

This section of the lab will discuss in detail four inverting amplifier configurations. The first inverter uses a current-mirror as the active load. The second is a basic inverter commonly used in CMOS digital logic. The last two amplifiers employ diode connected transistors as loads. The last to amplifiers employ diode connected transistors as loads. Each of these amplifiers has characteristics which makes its use advantageous in certain applications.

Inverter with Current-Mirror Load

The inverter of Figure 6-5 employs an NMOS driver and a PMOS current-mirror as the load. The current-mirror provides a large small-signal output resistance and constant biasing current. The biasing current establishes the operating point for transistor M_1, which in turn determines its small-signal transconductance. This circuit can provide a high output resistance and a large small-signal gain.

A disadvantage of this circuit is the need for a biasing current which requires additional circuitry. However, since this circuit is biased by another circuit, this amplifier can be programmed or tuned to operate at a specific operating point even during the presence of process variations.

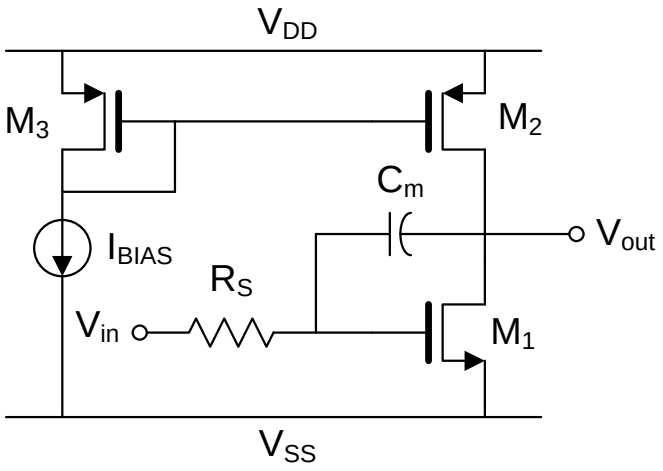


Figure 6-5: Inverting amplifier with current-mirror load

Design Procedure

This design procedure is only an example. To achieve the desired inverter performance another procedure may need to be used.

1) Determine the Miller compensation capacitor C_m from the gain-bandwidth product (GBW) specification. Remember GBW = $A_{V0} \cdot p_1$.
2) To guarantee stability be sure the phase margin is greater than 60º, make sure the non-dominant pole p_2 is at least three times greater than the GBW. Use this information along with the load capacitance to determine g_{m1}.
3) Determine I_{BIAS} to provide the desired DC gain.

4) Using g_{m1} and I_{BIAS}, determine the size for transistor M_1.

5) Use a 1:1 current-mirror sized such that the transconductance is equal to that of the driver transistor.

Digital CMOS Inverter

Figure 6-6 illustrates the basic CMOS inverter. This circuit is commonly used in digital logic circuits. Since both transistors are driven by the input source, the voltage gain will be higher with this circuit than the amplifier with the current-mirror load.

An advantage of this circuit is that it does not need external biasing circuitry. The operating point of this circuit is determined by the ratio of the transistor sizes. Using large transistors will cause G_m to be high. This allows higher frequency operation when driving large capacitive loads.

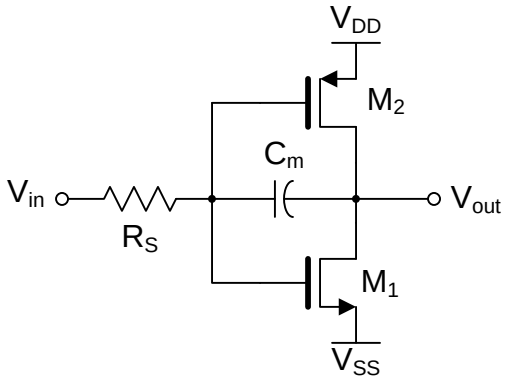


Figure 6-6: Digital CMOS inverting amplifier

Figure 6-7 illustrates the effect of changing the ratio of the transistors. Typically, the transition region will be half the supply voltage. In this case, the products of the transconductance and transistor sizes for the NMOS and PMOS must be equal. If process variations cause K_P or K_N to change, then the transition region will shift.

Figure 6-7 also shows the gain and linearity of the amplifier. The slope of the curve at any point it the gain. The vertical section of the graph is a region of high gain. Since the slope of the curve changes with signal amplitude, the amplifier exhibits high distortion. To obtain low distortion operation, the input voltage must remain small.

Design Procedure

This design procedure is only an example. To achieve the desired performance another procedure may need to be used.

1) First, notice the DC gain is determined by the power supply voltage for symmetrical operation:

$$A_{V0} = G_m R_B = g_{m1} \frac{1}{\lambda I_{BIAS}} = \frac{2}{\lambda (V_{GS} - V_T)} = \frac{2}{\lambda (V_{DD} - V_T)}$$

2) Determine Miller Compensation capacitor C_m from gain-bandwidth product (GBW) specification or dominant pole specification. Remember GBW = A_{V0} p_1.

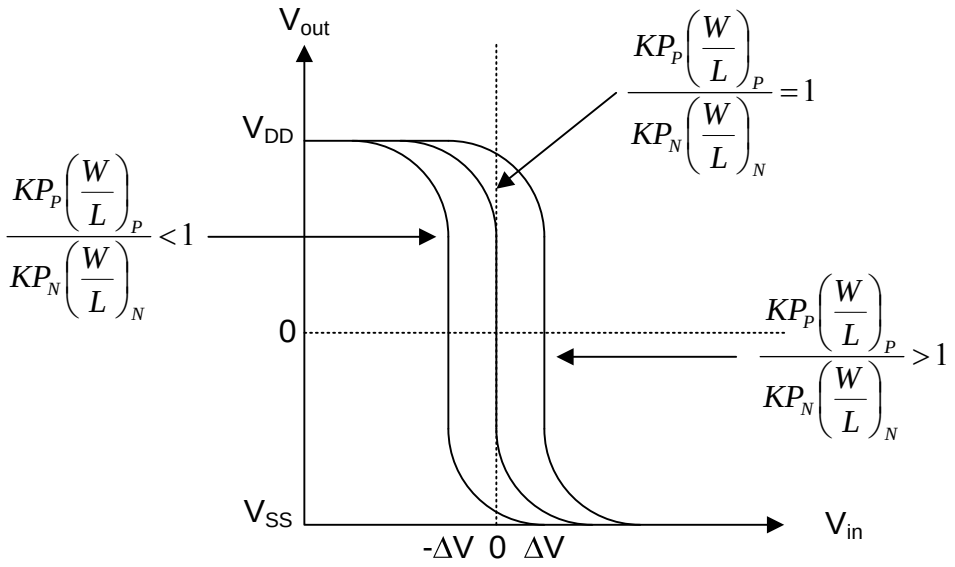


Figure 6-7: Transition regions for various transistor size ratios

3) To guarantee stability be sure the phase margin is greater than 60°. This requires the non-dominant pole p_2 to be at least three times higher in frequency than the gain-bandwidth product ($p_2 > 3$ GBW). Use this information to determine g_{m1}.

4) Remember, for symmetrical operation the transistors must be in the ratio:

$$\frac{KP_N\left(\frac{W}{L}\right)_N}{KP_P\left(\frac{W}{L}\right)_P} = 1$$

5) Using the value for g_{m1} and the above equation, determine the size for transistors M_1 and M_2. Remember, the current through both transistors is the same.

$$KP_{N,P}\left(\frac{W}{L}\right)_{N,P} = \frac{g_{m1,2}}{(V_{DD} - V_T)}$$

PMOS Only Inverter with Self-Biased Load

Figure 6-8 shows a PMOS inverter. This inverter does not require a CMOS process. Due to the diode connected load, the inverter has a low output resistance which in turn gives it a low gain. This inverter however is very linear.

The derivation of the large-signal transfer function is easy. Assume both transistors are the same size and perfectly matched. Since the drain current is the same for both transistors:

$$I = I_{D1} = I_{D2} = \frac{1}{2} K_P \frac{W}{L} (V_{GS1} - V_T)^2$$

and M_2 is diode connected, V_{out} is given by:

$$V_{out} = V_{SS} + V_{GS2}$$

$$V_{out} = V_{SS} + \sqrt{\frac{2I}{K_P \frac{W}{L}}} + V_T$$

The gate to source voltage of M_1 is equal to the input voltage and the equation becomes:

$$V_{out} = V_{SS} + \sqrt{\frac{2\frac{1}{2}K_P \frac{W}{L}(V_{DD} - V_{in} - V_T)^2}{K_P \frac{W}{L}}}$$

$$V_{out} = V_{SS} + V_{DD} - V_{in}$$

$$V_{out} = -V_{in}$$

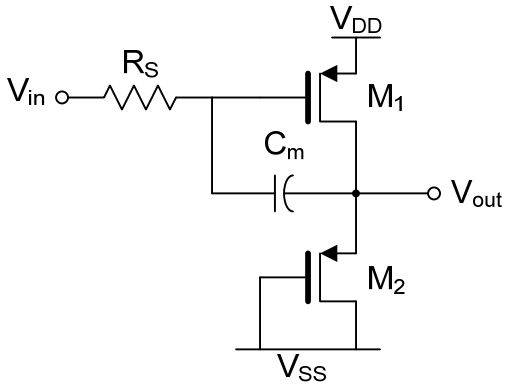


Figure 6-8: PMOS only inverter with self-biased load

Design Procedure

This design procedure is only an example. To achieve the desired inverter performance another procedure may need to be used.

1) First, notice the DC gain is determined by the sizes of the transistors. For a unity-gain buffer, the gain is one.

$$A_{V0} = G_m R_B = -\frac{g_{m1}}{g_{m2}}$$

2) Determine the Miller compensation capacitor C_m from the dominant pole location of the GBW product specification.

3) To guarantee stability, be sure the phase margin is greater than 60º. This requires the non-dominant pole p_2 to be at least three times higher in frequency than the GBW product. Use this information to determine g_{m1} and g_{m2}.

4) Using the value for the transistor transconductance determine the size for transistors M_1 and M_2. Remember, the current through both transistors is the same.

CMOS Inverter with Self-Biased Load

The inverter of Figure 6-9 is similar to the previous inverter except it requires a CMOS process. Matching of transistors is also difficult. Use a design procedure similar to the previous inverter.

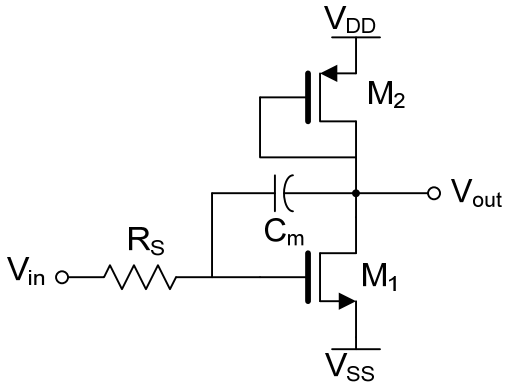


Figure 6-9: CMOS inverter with self biased load

Summary of AC Characteristics

Table 6-1 lists the capacitors and resistors from Figure 6-2 and gives the parameter value for each of the four configurations. This table does not include all possible parasitic capacitance associated with the transistors. The table also does not include stray capacitance associated with circuit layout. Depending on the application, the stray capacitance might be a significant component of the frequency response.

Table 6-1: Relationship between the generic amplifier model and various inverter circuits

	Current-Mirror Load	Digital CMOS	Self-Biased PMOS	Self Biased CMOS
R_A	R_S	R_S	R_S	R_S
R_B	$r_{o1}\|\|r_{o2}\|\|R_L$	$r_{o1}\|\|r_{o2}\|\|R_L$	$r_{o1}\|\|1/g_{m2}\|\|R_L$	$r_{o1}\|\|1/g_{m2}\|\|R_L$
C_A	C_{gs1}	$C_{gs1}+C_{gs2}$	C_{gs1}	C_{gs1}
C_B	$(C_{bd1}\|\|C_{bs1})+$ $(C_{bd2}\|\|C_{bs2})+$ C_L	$(C_{bd1}\|\|C_{bs1})+$ $(C_{bd2}\|\|C_{bs2})+$ C_L	$(C_{bd1}\|\|C_{bs1})+$ $(C_{bd2}\|\|C_{bs2})+$ C_L+C_{gs2}	$(C_{bd1}\|\|C_{bs1})+$ $(C_{bd2}\|\|C_{bs2})+$ C_L+C_{gs2}
C_C	$C_{gd1}+C_m$	$C_{gd1}+C_{gd2}+C_m$	$C_{gd1}+C_m$	$C_{gd1}+C_m$
G_m	g_{m1}	$g_{m1}+g_{m2}$	g_{m1}	g_{m1}

Prelab

The prelab exercises are due at the beginning of the next lab period. No late work is accepted.

1) Create a table ranking the various amplifiers as good, medium, or poor in the following categories: gain, input impedance, output impedance, and linearity. Include the expressions for each design specification (except for linearity).
2) Derive the transfer function for the generic amplifier by applying Miller's Theorem. Compare this transfer function to the one derived in the lab manual. Comment on the utility of Miller's Theorem.
3) Design the following inverting amplifiers:

   A) Current-mirror load inverter with the following specifications:

   GBW = 1 MHz, PM = 60º, A_{V0} = 30 dB, $V_{DD} = V_{SS}$ = 1.5 V, R_S = 100 kΩ, C_L = 30 pF

   B) Digital CMOS inverter with the following specifications:

   GBW = 1 MHz, PM = 60º, A_{V0} = 30 dB, $V_{DD} = V_{SS}$ = 1.5 V, R_S = 100 kΩ, C_L = 30 pF

   C) PMOS inverter with the following specifications

   GBW = 1 MHz, PM = 60º, A_{V0} = 0 dB, $V_{DD} = V_{SS}$ = 1.5 V, R_S = 100 kΩ, C_L = 30 pF

   D) Self-biased CMOS inverter with the following specifications

   GBW = 1 MHz, PM = 60º, A_{V0} = 0 dB, $V_{DD} = V_{SS}$ = 1.5 V, R_S = 100 kΩ, C_L = 30 pF

Lab

1) Simulate the designs from the prelab indicated by the TA. Simulate and perform design iterations until your circuit operates within specifications. These simulation results will be included in the final lab report. After the circuit is operating properly, create a DC input-output characteristic plot and comment on the linear region. Determine the input offset and add a bias source to the circuit to insure $V_{out} = V_{in} = 0$. Create frequency response plots, and determine the GBW, PM, p_1, and A_{V0}.
2) Layout your final design.
3) Repeat simulations from part 1 on the layout. Be sure parasitic capacitances from the layout are included.

Lab 7: Differential Pairs

Objective

Design, simulate, and layout various differential pairs used in different types of differential amplifiers such as operational transconductance amplifiers and operational amplifiers.

Introduction

Differential pairs are the final set of basic circuit elements that will be discussed in this lab course. These circuit elements are used as the input stages of operational amplifiers and operational transconductance amplifiers, common-mode feedback circuits, and analog multipliers. As with the other fundamental building blocks, a good understanding of differential pairs is required for successful analog circuit design.

A differential pair consists of two well-matched, source-coupled transistors as shown in Figure 7-1. An input voltage between the two gate terminals produces an output current in the drain terminals.

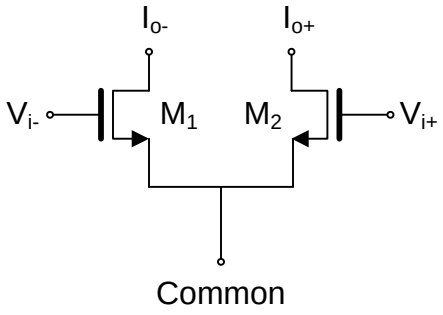


Figure 7-1: Basic differential pair

The most common application for a differential pair is the differential amplifier. Figure 7-2 shows the basic differential amplifier. It consists of a differential pair which is biased by the tail current source I_{tail}. Resistor R_{tail} models the output resistance of a real current source. Load resistors R_{D1} and R_{D2} allow the amplifier to develop an output voltage. The output voltage can be differential or single-ended. A differential output is developed between the two output terminals, while the single-ended output is taken between one output and ground.

The task of the differential amplifier is to amplify the difference between its two input signals. The signals can be decomposed into two components. The first component is called the differential-mode voltage v_{DM} and is given by:

$$v_{DM} = v_1 - v_2$$

The second component is called the common-mode voltage v_{CM} and is given by:

$$v_{CM} = \frac{v_1 + v_2}{2}$$

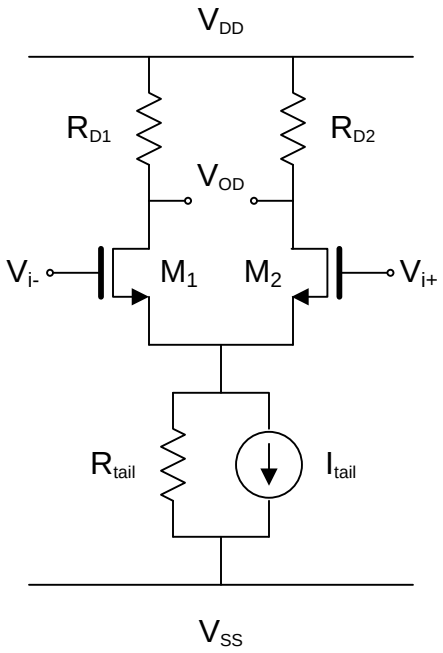


Figure 7-2: Basic differential amplifier

Assuming M_1 and M_2 are in saturation, neglecting channel length modulation, and assuming perfectly matched transistors, the large signal characteristics can be analyzed as follows:

$$v_{DM} = v_{G1} - v_{G2} = v_{GS1} - v_{GS2} = \sqrt{\frac{2I_{D1}}{\beta_1}} - \sqrt{\frac{2I_{D2}}{\beta_2}}$$

$$I_{tail} = I_{D1} + I_{D2}$$

where $\beta = KP \cdot (W/L)$. Assuming that $\beta = \beta_1 = \beta_2$ and combining both equations, two equations describing the drain currents are obtained.

$$I_{D1} = \frac{I_{tail}}{2} + \frac{I_{tail}}{2}\left[\frac{\beta \cdot v_{DM}^2}{I_{tail}} - \frac{\beta \cdot v_{DM}^4}{4 \cdot I_{tail}^2}\right]^{1/2}$$

$$I_{D1} = \frac{I_{tail}}{2} - \frac{I_{tail}}{2}\left[\frac{\beta \cdot v_{DM}^2}{I_{tail}} - \frac{\beta \cdot v_{DM}^4}{4 \cdot I_{tail}^2}\right]^{1/2}$$

These relationships are valid only for

$$|v_{DM}| \le \sqrt{\frac{2 \cdot I_{tail}}{\beta}}$$

and for M_1 and M_2 in saturation. This means that for v_{DM} greater than or equal to the above expression, then only one of the transistors is conducting and the other is off.

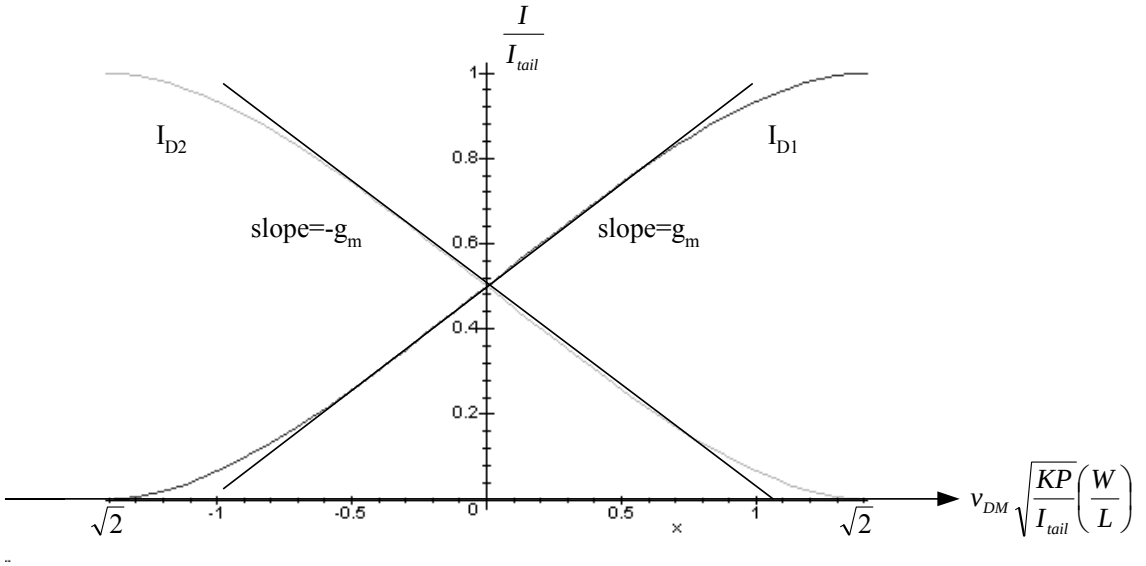


Figure 7-3: Normalized large signal transconductance characteristic of a MOS differential amplifier

The desired behavior of the differential amplifier is to amplify the differential-mode voltage and attenuate the common-mode voltage. The differential gain A_{DM} of an amplifier with a differential output is defined as:

$$A_{DM} = \frac{v_{OD}}{v_{DM}}$$

where v_{OD} is the differential output voltage. For a single-ended differential amplifier, the gain is defined as

$$A_{DM} = \frac{v_{OS}}{v_{DM}}$$

where v_{OS} is the single-ended output voltage. For an amplifier with a differential output, the common-mode to differential-mode gain is defined as:

$$A_{CM} = \frac{v_{OD}}{v_{CM}}$$

and for an amplifier with a single-ended output, the common-mode gain is defined as:

$$A_{CM} = \frac{v_{OS}}{v_{CM}}$$

For a symmetrical amplifier such as the fully-differential amplifier, that is an amplifier with a differential output and a differential input, the common-mode voltage gain will be zero if the differential pair is perfectly matched. Due to mismatches in the differential pair or in the loads, a common-mode input voltage can cause a differential output voltage. A figure of merit for differential amplifiers is the common-mode rejection ratio (CMRR). The CMRR is defined as the ratio of the differential gain and common-mode gain:

$$\mathrm{CMRR} = 20 \cdot \log_{10}\left(\left|\frac{A_{DM}}{A_{CM}}\right|\right)$$

The input common-mode voltage is limited in magnitude. The inputs must not force any of the transistors out of saturation. The limitation on the common-mode voltage creates a common-mode voltage range for the amplifier. When the common-mode voltage increases above the upper limit, the transistors in the differential pair will leave the saturation region and enter the linear region. If the common-mode voltage decreases below the lower limit, then the transistors in the tail current source will be forced out of saturation. The common-mode voltage range can be found by considering the saturation voltages for differential pair transistors and current source transistors. Remember, for a transistor to be in saturation:

$$V_{DS(SAT)} = V_{GS} - V_T = \sqrt{\frac{2I_D}{KP \cdot \frac{W}{L}}}$$

The output voltage range is also limited. For a single-ended amplifier with symmetrical power supplies, the magnitude of the output signal is limited to the supply rail:

$$V_{OS} \le \left|V_{DD}\right|$$

However, for a fully-differential amplifier the output signal can be twice this amplitude. Each output can swing to a supply rail, giving a differential output voltage that is twice as large as either rail. As with all amplifiers, another limit on the output voltage swing is the allowable distortion. An output signal swing which comes within 200 mV of the supply rails may have 10% THD; however, a signal which comes within 500 mV may have only 1% THD in the same circuit. The output voltage range is dictated by the distortion requirement.

The input-output characteristic curves of the differential amplifier are shown in Figure 7-4. The region where the input is approximately zero volts is linear. The size of the linear region is determined by the transistor sizes and $V_{DS(SAT)}$. Decreasing the transistor sizes will decrease the transconductance and usually increase the size of the linear region.

The amplifier also has an input and output impedance. The differential input resistance and the common-mode input resistance are large for MOSFET differential amplifiers. The differential input resistance is the resistance between the two input terminals. The common-mode input resistance is the resistance measured between the two interconnected inputs and ground.

The output impedance can also be measured in two different ways. For fully differential amplifiers, the differential output resistance is the resistance between the two output terminals. For single-ended amplifiers, the common-mode output resistance is the resistance measured between the output and ground.

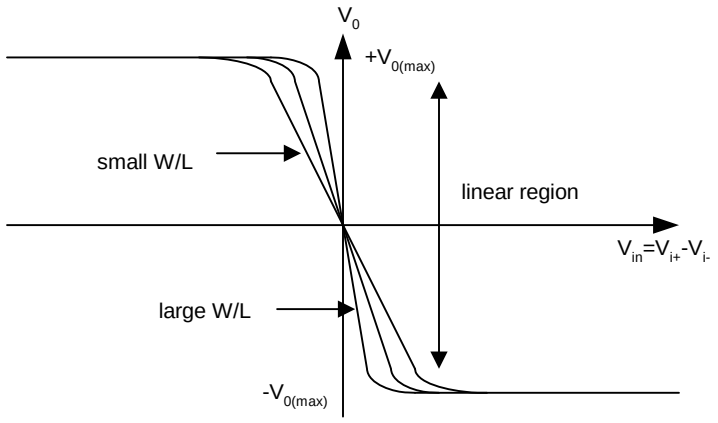


Figure 7-4: Input-output characteristic curves for a differential amplifier

Another figure of merit for the differential amplifier is its power supply rejection ratio (PSRR). This ratio indicates the effect of power supply variations or noise on the output voltage. For full-differential amplifiers with perfect matching in the differential pair and load, the PSRR is infinte. PSRR is given by:

$$\mathrm{PSRR}^{+} = 20 \cdot \log_{10}\left(\left|\frac{A_{dm}}{v_o / v_{DD}}\right|\right)$$

$$\mathrm{PSRR}^{-} = 20 \cdot \log_{10}\left(\left|\frac{A_{dm}}{v_o / v_{SS}}\right|\right)$$

The slew rate is a measure of how quickly the output of the differential amplifier can change in response to an instantaneous rail-to-rail (large-signal) change in the input voltage.

Due to process variations, the differential pair will not be perfectly matched. As a result, for equal input voltages, the drain currents will not be equal. Also, if the load is asymmetrical, then a non-zero output voltage will exist. The voltage at the input which forces the output voltage to zero is called the input offset voltage.

Design Description

This lab consists of the design of two single-ended differential amplifiers. Figure 7-5 illustrates the simple differential amplifier. This circuit consists of a differential pair biased by a simple current mirror. The active load is a PMOS current mirror.

Differential Gain

The differential gain of this circuit is given by:

$$A_{DM} = G_m \cdot R_{out} = -g_{m1,2} \cdot \left(r_{ds2} \parallel r_{ds6}\right)$$

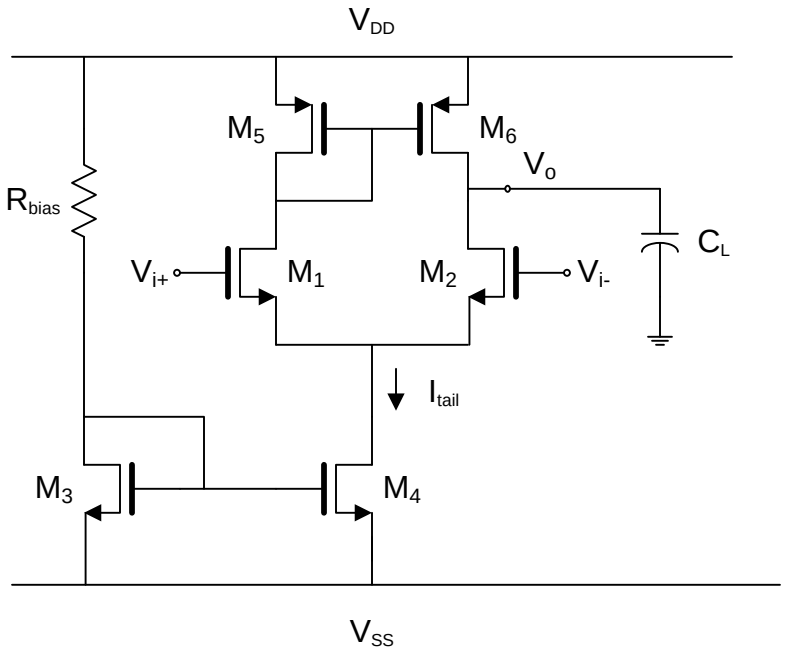


Figure 7-5: Simple differential amplifier

Slew Rate

The biasing current and the amount of load capacitance determine the slew rate. The slew rate is given by:

$$SR = \frac{I_{tail}}{C_L}$$

GBW and Dominant Pole

Since the output node is a high-impedance node, the dominant pole is located at:

$$p_1 = \frac{1}{R_{out} \cdot C_L}$$

The gain-bandwidth product is then given by:

$$GBW = A_{DM} \cdot p_1$$

Input Common-Mode Voltage Range

As mentioned previously, the input common-mode voltage range is the range of input voltages which keep the current-source and active load transistors in saturation. The common-mode voltage range is determined by the sizes of the transistors. To increase the common-mode voltage range, the sizes of the transistors must be increased. The input common-mode voltage range is given by:

$$V_{SS} + \overbrace{\sqrt{\frac{2I_{tail}}{K_N \frac{W}{L}_{3,4}}}}^{V_{DS,sat4}} + \overbrace{\sqrt{\frac{I_{tail}}{K_N \frac{W}{L}_{1,2}}}}^{V_{DS,sat1,2}} + V_{TN} < V_{in(CM)} < V_{DD} - \overbrace{\sqrt{\frac{I_{tail}}{K_P \frac{W}{L}_{5,6}}}}^{V_{DS,sat5}} - V_{TP} + V_{TN}$$

Common Mode Gain

To design for common mode, we can no longer assume that there exists an AC signal ground at the source of M_1 and M_2. This current source must be substituted by a resistor of value equal to the output resistance of the current mirror. To help in the development of the design equations, Figure 7-6 is used. From this figure, the common-mode voltage can be found by:

$$i_d = g_m v_{gs} = g_m (v_{CM} - v_S)$$
$$v_S = 2 i_d r_{o4}$$
$$v_{CM} = i_d \left(\frac{1}{g_m} + 2 r_{o4} \right) \approx 2 i_d r_{o4}$$

Following a similar approach, the output voltage is given by

$$v_{out} \approx -i_d \frac{1}{g_{m6}}$$

The common-mode gain is then given by:

$$A_{cm} = \frac{v_{out}}{v_{CM}} \approx -\frac{1/g_{m6}}{2 r_{o4}} = -\frac{1}{2 g_{m6} r_{o4}}$$

As can be seen from this equation, the CMRR can be improved by increasing the output impedance of the tail current.

$$CMRR \approx 20 \log_{10} \left| \frac{A_{dm}}{A_{cm}} \right| = 20 \log_{10} \left| g_{m1,2} (r_{ds2} \parallel r_{ds6}) 2 g_{m6} r_{o4} \right|$$

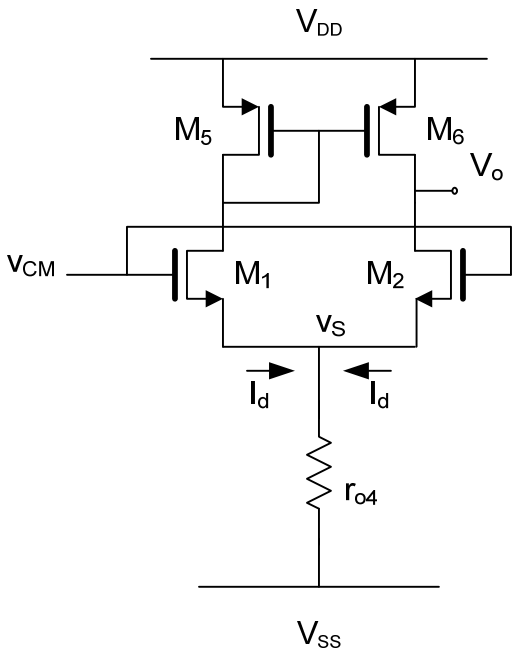


Figure 7-6: Differential amplifier used to determine CMRR

Cascode Differential Amplifier

The second differential amplifier is shown in Figure 7-7. This circuit utilizes low-voltage cascode current mirrors as the current source and active load. Design equations for this structure are the same as the previous structure except that the output impedance of the amplifier and current source are now larger. This will increase differential-mode gain while decreasing common-mode gain, thus a vastly improved CMRR. The main drawback of this circuit is a reduced input common-mode range and output swing

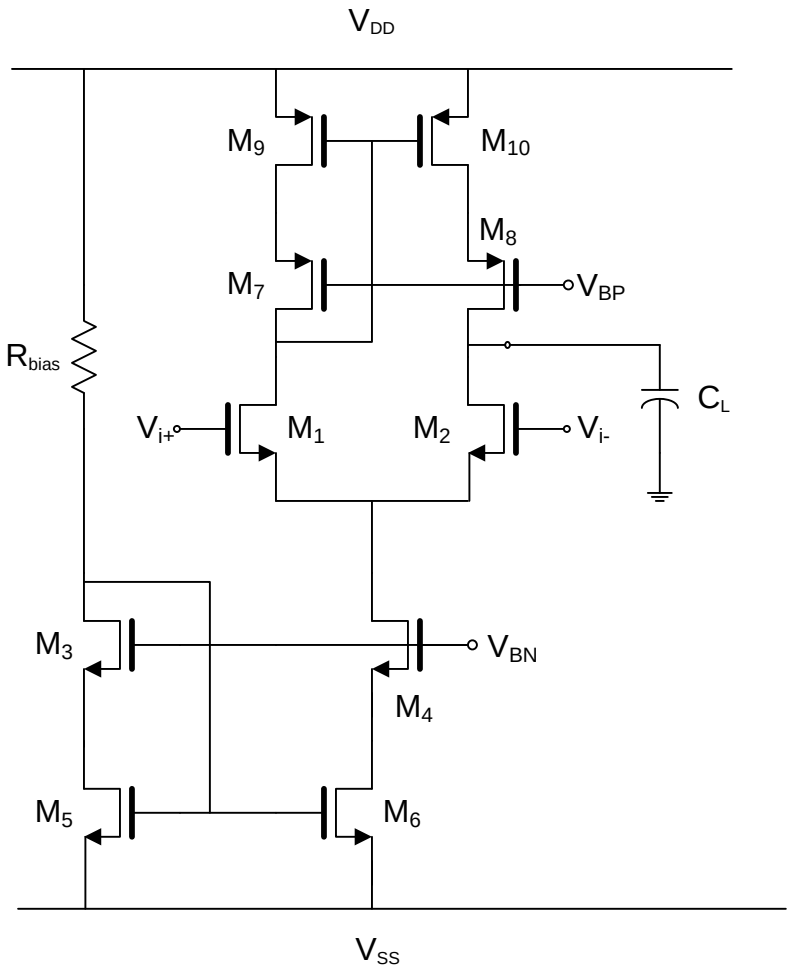


Figure 7-7: Cascode differential amplifier

Prelab

The prelab exercises are due at the beginning of the next lab period. No late work is accepted.

1) Compare the two single-ended differential amplifiers discussed in this lab. Rate the differential gain, common-mode gain, power supply voltage, CMRR, and common-mode input range. Include the expressions for each design specification.

2) Design the simple differential amplifier in Figure 7-5 to obtain the following specifications:

Slew Rate	10 V/μs
Gain-Bandwidth Product	2.5 MHz
Common-Mode Voltage Range	1.75 V
Power Supply	$V_{DD} = -V_{SS} = 1.5$ V
Load Capacitance	10 pF

3) Design the cascode differential amplifier in Figure 7-7 to obtain the following specifications:

Slew Rate	10 V/μs
Gain-Bandwidth Product	2.5 MHz
CMRR	> 80 dB
Power Supply	$V_{DD} = -V_{SS} = 1.5$ V
Load Capacitance	10 pF

Lab

1) Simulate the design from the prelab indicated by the T.A.

   Measure and plot:

   - Common-mode range
   - Differential-mode gain
   - Common-mode gain
   - CMRR
   - GBW
   - Dominant pole p_1
   - Slew rate

   Use any analysis necessary to obtain the most accurate measurements. Include these results in the lab report.

2) Layout the final design. Repeat above measurements. Be sure to include parasitic capacitance in the layout extraction. Include these results in the lab report.

Lab 8: Operational Transconductance Amplifiers

Objectives

Design, simulate, and layout an operational transconductance amplifier.

Introduction

The operational transconductance amplifier (OTA) is a basic building block of electronic systems. The function of a transconductor is to convert an input voltage into an output current. The transconductance amplifier can be configured to amplify or integrate either voltages or currents. The versatility of an OTA allows its use in many electronic systems such as filters, analog-to-digital converters, and oscillators. An OTA is also used as the core amplifier for an operational amplifier (discussed in Lab 9). The operational transconductance amplifier is an essential element of many analog systems.

The symbol for a single-ended OTA is shown in Figure 8-1. The amplifier has two voltage inputs and a single current output. Fully-differential versions are available and are commonly used in integrated circuits.

The output current of an OTA is proportional to the difference between the input voltages. The relationship between the input voltages and output current is given by:

$$I_O = G_m \cdot (V_{i+} - V_{i-}).$$

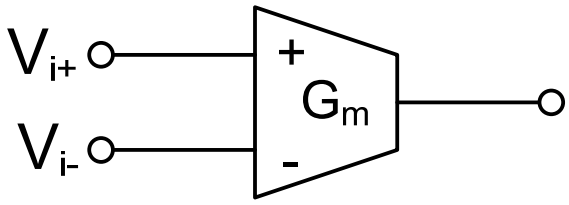


Figure 8-1: OTA symbol

The input-output characteristic for an OTA is shown in Figure 8-2. Notice that this characteristic is similar to the input-output characteristic for the differential amplifier. For a given maximum output current, the width of the OTA's linear region is inversely related to the magnitude of the transconductance; the larger the linear region, the smaller the transconductance.

The input and output resistance must be large in an OTA. Infinite input impedance allows maximum transfer of the source voltage to the input of the OTA. Maximum transfer of output current to the load occurs when the output resistance is infinite.

The circuit diagram for a basic OTA is shown in Figure 8-3. Notice that this is the differential amplifier from Lab 6.

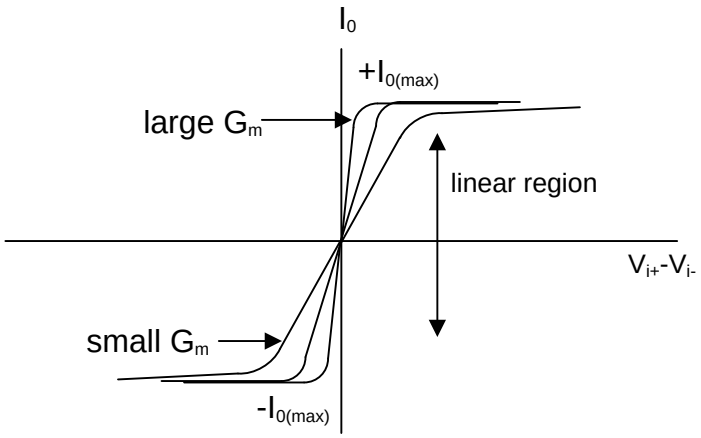


Figure 8-2: Input-output characteristic for an OTA

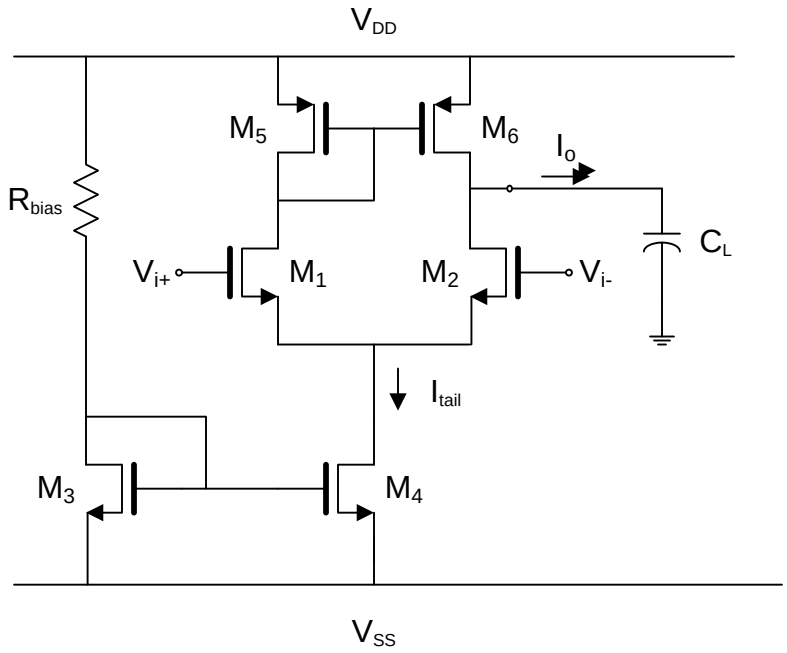


Figure 8-3: Differential amplifier used as an OTA

A quick analysis of this amplifier shows the transconductance is given by:

$$G_m = g_{m1,2}$$

The input resistance is large due to the inputs being at the gate terminals of the MOS differential pair. Notice that the output resistance is also large:

$$R_{out} = r_{ds2} \,||\, r_{ds6}$$

The gain-bandwidth product is given approximately by:

$$GBW = \frac{g_{m1,2}}{C_L}$$

An improvement of the differential amplifier of Figure 8-3 is to use self-biased loads. The circuit in Figure 8-4 is called a symmetric OTA or three current-mirror OTA. This circuit is constructed from all the basic elements discussed in the previous labs. The input stage is a differential pair (Lab 7). The sub-circuits composed of $M_{1,3}$ and $M_{2,4}$ are self-biased inverters (Lab 6). Transistors $M_{3,5}$, $M_{4,6}$, $M_{7,8}$, and $M_{9,10}$ are simple current-mirrors (Lab 5).

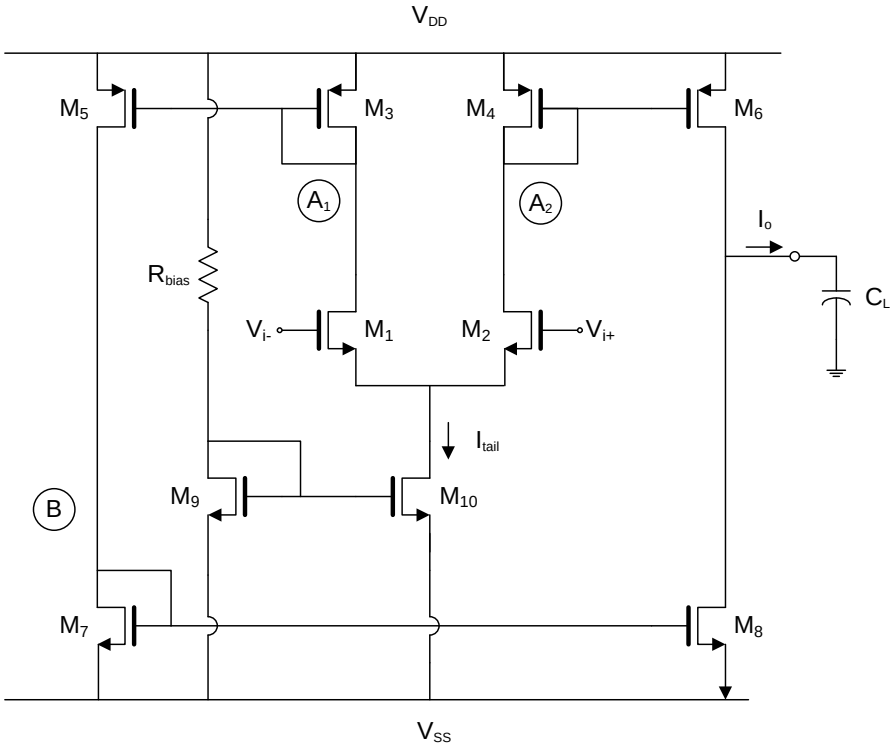


Figure 8-4: Three current-mirror OTA

When designing the symmetrical OTA, transistors $M_1 = M_2$, $M_3 = M_4$, $M_5 = M_6$, and $M_7 = M_8$. This reduces the number of designable parameters to four transistor sizes and the tail current. An analysis of this amplifier shows the transconductance is given by:

$$G_m = \beta \cdot g_{m1,2}$$

where

$$\beta = \frac{g_{m5,6}}{g_{m3,4}}$$

The input resistance is large due to the MOS input stage. The output resistance is approximately given by:

$$R_{out} = r_{ds6} \,||\, r_{ds8}$$

The gain-bandwidth product is given approximately by:

$$GBW = \beta \cdot \frac{g_{m1,2}}{C_L}$$

Analysis shows that the three current-mirror OTA has a larger transconductance, slew rate, and GBW than the OTA of Figure 8-3 when β is greater than unity. These specifications are made larger by increasing β.

Design Description

The design of an OTA begins with a consideration of the design specifications. The typical design considerations for an OTA include transconductance, slew rate, output resistance, GBW, noise, phase margin, power dissipation, and output loading. The transconductance of the symmetric OTA was listed previously and is repeated here for convenience:

$$G_m = \beta \cdot g_{m1,2} = \beta \cdot \sqrt{I_{tail} \cdot K_N \cdot \frac{W}{L}1,2}$$

where

$$\beta = \frac{g_{m5,6}}{g_{m3,4}}$$

In the above equation, notice that the DC current in transistors $M_{5,6}$ is β times larger than the currents in transistors $M_{3,4}$. The transconductance can be set by the tail current source, current mirror ratio, or size of the input transistors. The transconductance is usually the most important parameter, and it is fortunate that it can be determined by several parameters. Automatic tuning circuits sometimes vary the bias current in order to adjust the transconductance to the desired value.

The slew rate of the OTA is given by:

$$SR = \beta \cdot \frac{I_{tail}}{C_L}$$

Notice the slew rate is larger than the slew rate of the differential amplifier. The increased slew rate comes with the disadvantage of an increase in current (power) consumption. The current drawn from the power supply (not including bias current source) is given by:

$$I_{DD} = \frac{1}{2} I_{tail} + \frac{1}{2} I_{tail} + \frac{1}{2} \beta \cdot I_{tail} + \frac{1}{2} \beta \cdot I_{tail} = (\beta + 1) I_{tail}$$

The output resistance was listed above and is repeated below as:

$$R_{out} = r_{ds6} \parallel r_{ds8}$$

The gain-bandwidth product is given by:

$$GBW = A_{V0} \cdot p_1 = (G_m \cdot R_{out}) \left(\frac{1}{R_{out} \cdot C_L} \right) = \frac{G_m}{C_L}$$

Another design consideration is noise. The noise performance is improved when the voltage gain of the first stage is large. The voltage gain of the first stage is given by:

$$A_{V1} = g_{m1,2} \cdot \frac{1}{g_{m3,4}} = \sqrt{\frac{K_N}{K_P} \frac{\frac{W}{L}1,2}{\frac{W}{L}3,4}}$$

The phase margin is a measure of stability for the amplifier. In most cases, the load capacitance is much larger than the capacitance at the other nodes. When this is the case, the operational transconductance amplifier has a dominant pole at the output node and two non-dominant poles at the other two nodes. Due to the extra current mirror in one path to the output, there is a left-half plane zero. For most symmetric OTA designs, the non-dominant poles and zero are much larger than the gain-bandwidth product and degrade the phase margin by less than 10º each. This gives a typical phase margin of greater than 60º. The transfer function of the OTA is given by:

$$H(s) = \frac{\frac{A_{V0} \cdot \rho_1 \rho_2 \rho_3}{z}(s+z)}{(s+\rho_1)(s+\rho_2)(s+\rho_3)}$$

where:

p_1 - is the dominant pole, located at the output node: $p_1 = \frac{1}{R_{out} C_L}$

p_2 - is the non-dominant pole, located at nodes A_1 and A_2:

$$p_2 = \frac{1}{R_A C_A} \approx \frac{g_{m3,4}}{C_A}$$

p_3 - is the non-dominant pole, located at node B: $p_3 = \frac{1}{R_B C_B} \approx \frac{g_{m7}}{C_B}$

z - is the zero due to the pole-zero doublet formed by the $M_{7,8}$ current mirror:

$$z = 2\, p_2$$

The phase margin is thus given by:

$$PM = 180^0 - \tan^{-1}\left(\frac{GBW}{p_1}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right) + \tan^{-1}\left(\frac{GBW}{z}\right) - \tan^{-1}\left(\frac{GBW}{p_3}\right)$$

$$\approx 90^0 - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{z}\right) - \tan^{-1}\left(\frac{GBW}{p_3}\right)$$

The above design description shows that many performance figures are inversely related. For example, increasing slew rate results in an increase in power dissipation.

Prelab

The prelab exercises are due at the beginning of the next lab period. No late work is accepted.

1) Design the three current mirror OTA of Figure 8-4 to obtain the following specifications:

G_m:	500 μA/V
Slew Rate:	SR > 10 V/μs
C_L:	20 pF
Power:	P_D < 1 mW (not including bias current source)
Power Supply:	$V_{DD} = -V_{SS} = 1.5$ V

Lab

1) Simulate the design from the prelab. Measure the transconductance vs. frequency, slew rate, power consumption, voltage gain vs. frequency, dominant pole frequency, phase margin, and gain-bandwidth product. Use any analysis necessary to obtain the most accurate measurements. These simulation results will be included in the final lab report.
2) Create three cell views for your OTA: symbol, schematic, and layout. Layout your final design and use good layout techniques. In your lab report indicate which transistors should be matched. Extract the layout and repeat simulations from part 1. Be sure to include parasitic capacitances in the extraction.

Lab 9: Operational Amplifier

Objective

Design, simulate, layout, and test a three-stage operational amplifier.

Introduction

The operational amplifier (opamp), like the operational transconductance amplifier, is an essential component of analog system design. Integrated circuit design, as well as board level design, heavily uses operational amplifiers. This component is basically a high-gain voltage amplifier. Opamps are used in many analog systems such as filters, regulators, and function generators. This device is also used to create buffers, logarithmic amplifiers, and instrumentation amplifiers. The opamp can also function as a simple comparator. Knowledge of operational amplifier function and design is important in analog design.

The symbol for an operational amplifier is shown in Figure 9-1. The basic device has two inputs and a single output. A fully-differential version of the opamp is often used in high performance integrated circuit designs.

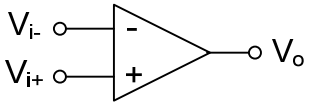


Figure 9-1: Operational amplifier symbol

The operational amplifier functions as a voltage amplifier. The relationship between the input and output voltage is given by:

$$V_o = A_{V0} \cdot (V_{i+} - V_{i-})$$

The amplifier has a high voltage gain ($A_{V0} > 1000$ for CMOS opamps). Due to the high gain, the linear region is very narrow. Figure 9-2 illustrates the typical input-output characteristic for an operational amplifier used with and without feedback. The open-loop (without feedback) plot shows the linear region is only a few millivolts wide. From Figure 9-2, the open loop input-output characteristic is clearly nonlinear.

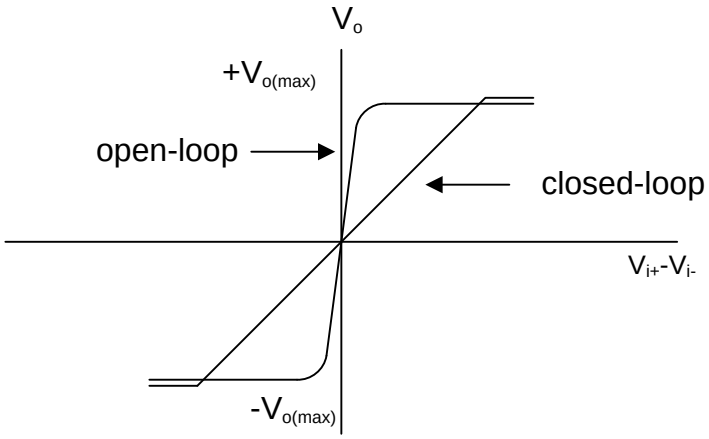


Figure 9-2: Input-output characteristic for an opamp

Due to the high gain and limited linear region, the opamp is commonly used in a negative feedback loop. Figure 9-2 shows also the input-output characteristic when the amplifier is used with feedback. Notice the closed-loop linear region consists of almost the entire input voltage range. The application of feedback reduces the non-linearity, but also reduces the voltage gain.

The simplest operational amplifier is the differential amplifier studied in Lab 7. This amplifier can be improved by adding a second stage. The second stage is an inverting amplifier with a current-source load. The two-stage amplifier shown in Figure 9-3 is referred to as a Miller OTA.

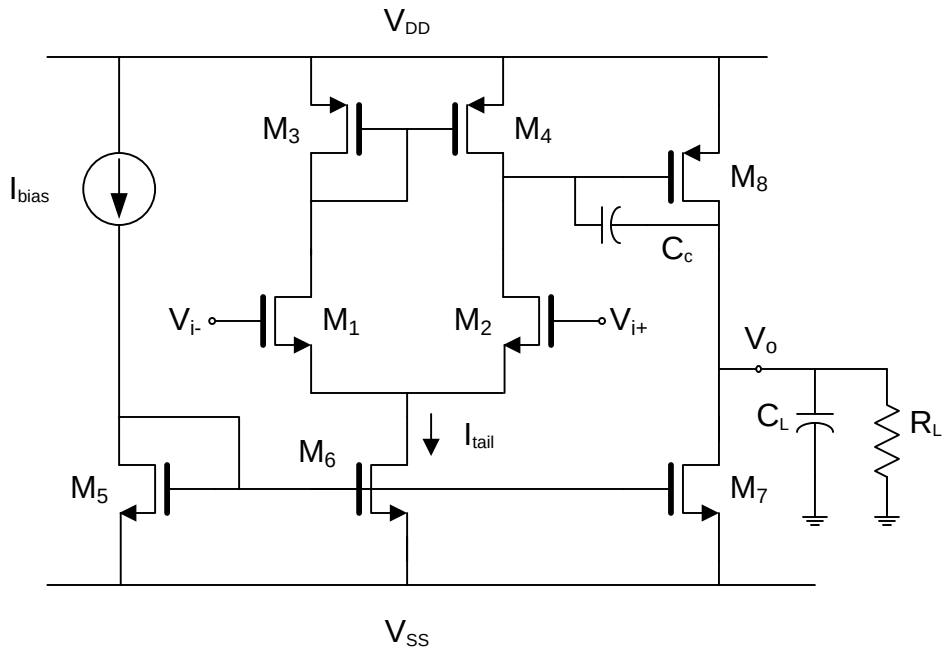


Figure 9-3: Miller OTA

Since the operational amplifier is a voltage amplifier, a high input resistance and low output resistance are desirable characteristics. A high input resistance maximizes the transfer of voltage from the source to the amplifier. Similarly, a low output resistance maximizes the transfer of output voltage from the amplifier to the load. The Miller OTA has a low frequency voltage gain of:

$$A_{V0} = G_m \cdot R_{out}$$

The transconductance is given by:

$$G_m = \frac{g_{m1,2} \cdot g_{m8}}{g_{o2} + g_{o4}}$$

The output resistance of the two-stage opamp is given by:

$$R_{out} = r_{ds7} \parallel r_{ds8}$$

Notice the output resistance is large. This resistance can be reduced by adding a third stage to that amplifier. A complementary push-pull source-follower output stage

can be designed to reduce the open-loop output resistance to a small value. Figure 9-4 illustrates a three-stage opamp.

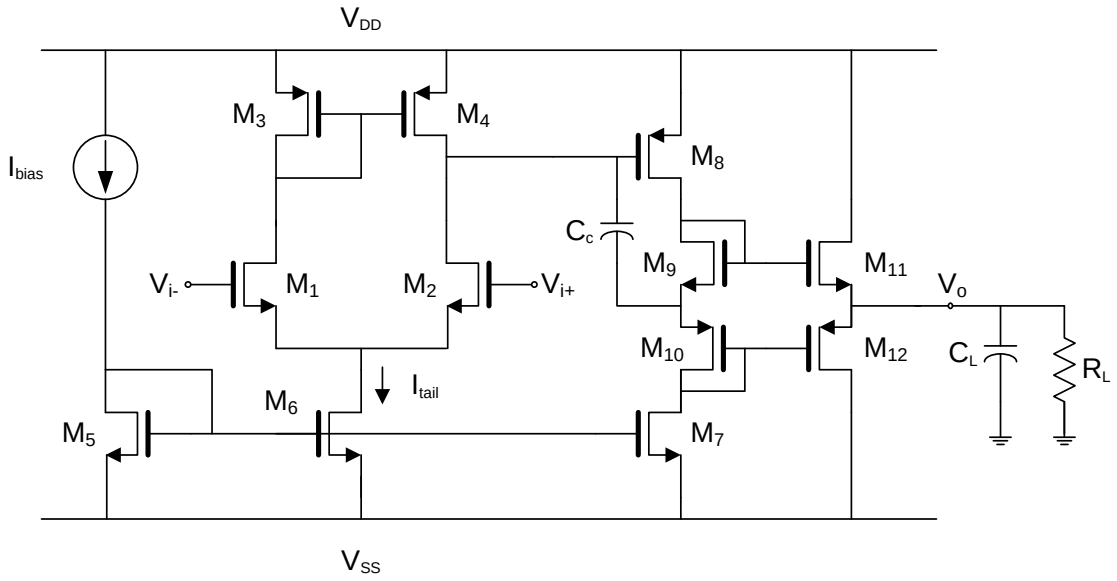


Figure 9-4: Operational amplifier

Design Description

The three-stage operational amplifier can be modeled as a cascade arrangement of three amplifiers. Figure 9-5 illustrates the sequence of amplifiers. The first stage is a differential amplifier. This stage produces an amplified version of the difference in input signals. This stage determines the CMRR, slew rate, and other performance specifications determined by the differential amplifier described in Lab 7.

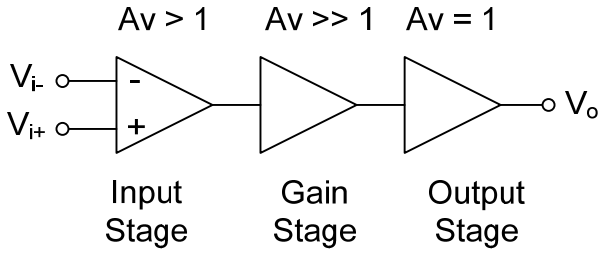


Figure 9-5: Three-stage operational amplifier model

The second stage is an inverting amplifier. The purpose of this stage is to provide a large voltage gain. The gain stage and the input stage create two poles which affect the stability of the system. Usually some form of compensation is required to assure the amplifier is unity-gain stable. Additional gain stages can be employed to increase the gain, but this increases the stability problems and requires complex compensation techniques. Refer to Lab 6 for details on the inverting amplifier performance specifications.

The output stage is essentially a power amplifier. The current gain is usually large and the voltage gain is typically unity. The output stage provides a buffer between the

gain stage and the load and has a small output impedance. Careful biasing is required to keep the output stage operating in the class-AB operating mode.

The frequency response of an operational amplifier will be analyzed with help from a macromodel of the structure. Figure 9-6 shows a macromodel of the opamp. The capacitor C_{in} models the input capacitance of the opamp, which is due mostly from gate-to-source capacitance. The subcircuit consisting of G_{mA}, R_A, and C_A model the gain and frequency response of the input stage. The capacitance C_A includes the input capacitance of the second stage and the output capacitance of the first stage. The components G_{mB}, R_B, and C_B model the second stage. Similarly, the capacitance C_B models the input capacitance of the third stage and output capacitance of the second stage.

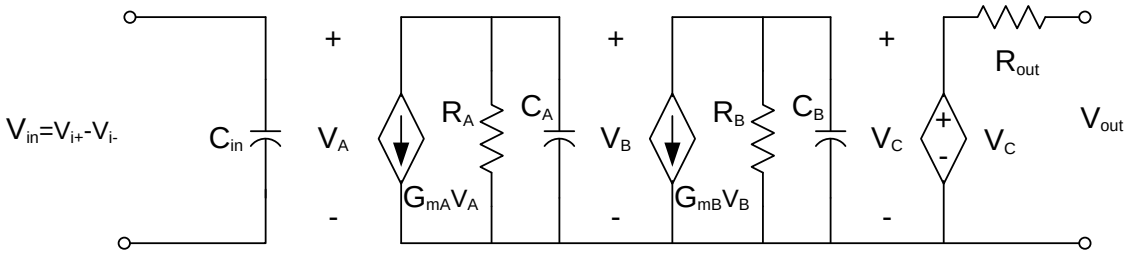


Figure 9-6: Operational amplifier macromodel

The transfer function of the macromodel is given by:

$$H(s) = \frac{A_{Vo} \cdot \rho_1 \rho_2}{(s+\rho_1)(s+\rho_2)} = \frac{\dfrac{G_{mA}G_{mB}}{C_A C_B}}{\left(s + \dfrac{1}{R_A C_A}\right)\left(s + \dfrac{1}{R_B C_B}\right)}$$

This transfer function assumes the source resistance is zero ohms and the load is an open-circuit. Notice the two poles may be close to each other. The capacitors C_A and C_B are dominated by gate-to-source capacitance, and R_A and R_B are the parallel connected small-signal drain-to-source resistance. The pole-zero plot of this transfer function is illustrated in Figure 9-7.

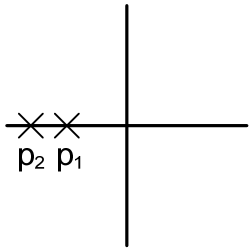


Figure 9-7: Pole-zero diagram for uncompensated opamp

Due to the two poles being located close together, the system is unlikely to be unity-gain stable due to the large DC gain of an operational amplifier. Clearly, some form of compensation is required. The modified macromodel shown in Figure 9-8 uses capacitor C_C to compensate the frequency response of the opamp by splitting the distance between the two poles.

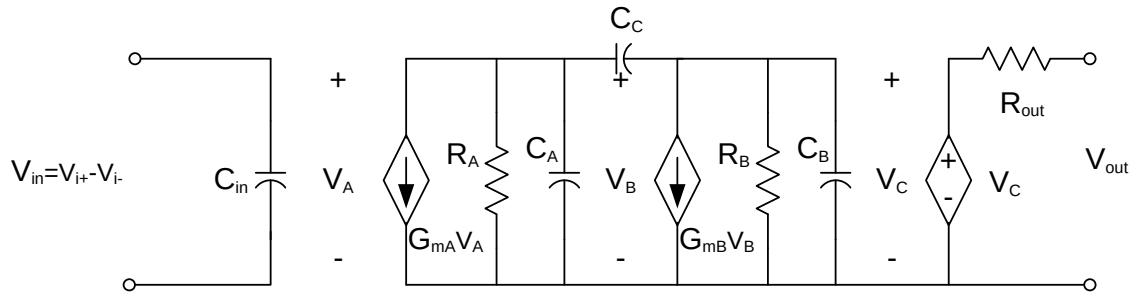


Figure 9-8: Operational amplifier macromodel with compensation capacitor C_C

Assuming R_A is large, that is:

$$R_A \approx R_B \text{ and } R_A >> \frac{1}{G_{mB}}$$

and C_A is small:

$$C_C >> C_A$$

and using the results obtained from the inverting amplifier lab, the transfer function for the operational amplifier with the compensation capacitor is:

$$H_C(s) = \frac{\frac{A_{V0} \cdot \rho_1 \rho_2}{z}(s - z)}{(s + \rho_1)(s + \rho_2)} = \frac{\frac{G_{mA}}{C_B}\left(s - \frac{G_{mB}}{C_C}\right)}{\left(s + \frac{1}{G_{mB} R_A R_B C_C}\right)\left(s + \frac{G_{mB}}{C_A + C_B}\right)}$$

These simplifying assumptions hold because capacitance C_B will include the capacitance of the buffer, and the compensation capacitance C_C can be chosen to be the size of the load capacitor. Also, for the two-stage OTA, capacitance C_B will include the load capacitance C_L.

With the transfer function in factored form, we can find the open-loop DC gain, poles, and zero of the compensated opamp are given by:

$$A_{V0} = G_{mA} G_{mB} R_A R_B$$

$$\rho_1 = \frac{-1}{G_{mB} R_B C_C R_A} = \frac{-1}{|A_{V2}| C_C R_A}$$

$$\rho_2 = \frac{-G_{mB}}{C_A + C_B}$$

$$z = \frac{G_{mB}}{C_C}$$

$$GBW = \frac{G_{mA}}{C_C}$$

Notice the addition of the compensation capacitor C_C caused the poles to separate. One pole moved closer to the origin by a factor of $A_{V2} = G_{mB} \cdot R_B$, while the other pole

moved away from the origin by a factor of A_{V2}. This compensation technique is called "pole splitting". The pole-zero plot of this transfer function is illustrated in Figure 9-9. Also, notice the creation of a zero as a result of the transition path created by the capacitor.

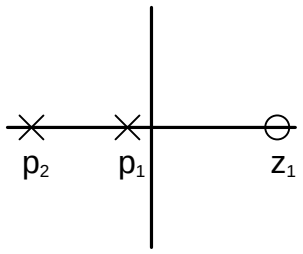


Figure 9-9: Pole-zero plot for a compensated opamp

Using the compensated opamp in a feedback loop produces the following transfer function:

$$A_C(s) = \frac{H_C(s)}{1 + H_C(s)\cdot\beta}$$

$$= \frac{A_0(s-z)}{(s+\rho_1)(s+\rho_2) + A_0\beta(s-z)}$$

$$= \frac{A_0\left(s - \frac{G_{mB}}{C_C}\right)}{s^2 + \left(\frac{1}{G_{mB}R_AR_BC_C} + \frac{G_{mB}}{C_B} + \frac{G_{mA}}{C_B}\beta\right)s + \left(\frac{1}{R_AC_BR_BC_C} + \frac{G_{mA}G_{mB}}{C_BC_C}\beta\right)}$$

where

$$A_0 = \frac{G_{mA}}{C_B}$$

The closed-loop transfer function using the compensated amplifier can be approximated by:

$$A_C(s) = \frac{\frac{G_{mA}}{C_B}\left(s - \frac{G_{mB}}{C_C}\right)}{s^2 + \left(\frac{G_{mB}}{C_B} + \frac{G_{mA}}{C_B}\beta\right)s + \left(\frac{G_{mA}G_{mB}}{C_BC_C}\beta\right)}$$

The effect of the above simplification on the system is to assume the dominant pole is at the origin. Notice that when the system is in open-loop ($\beta = 0$), the transfer function reduces to:

$$A_C(s) = \frac{\frac{G_{mA}}{C_B}\left(s - \frac{G_{mB}}{C_C}\right)}{s\left(s + \frac{G_{mB}}{C_B}\right)}$$

The factor β varies the position of the dominant pole from the origin to the neighborhood of the non-dominant pole. Figure 9-10 illustrates the effect of feedback on the frequency response.

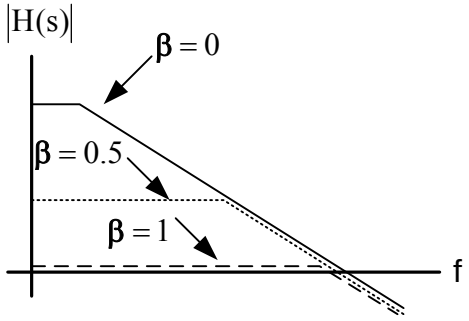


Figure 9-10: Closed-loop frequency response

To assure the feedback system is unity-gain stable (β = 1), the phase margin must be examined. The phase margin is the amount of phase before phase inversion (180º) at the unity gain frequency. The expression for the phase margin is given by:

$$\begin{aligned} PM &= 180^0 - \tan^{-1}\left(\frac{\omega_{0dB}}{p_1}\right) - \tan^{-1}\left(\frac{\omega_{0dB}}{p_2}\right) - \tan^{-1}\left(\frac{\omega_{0dB}}{z}\right) \\ &= 180^0 - \tan^{-1}\left(\frac{GBW}{p_1}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{z}\right) \\ &= 180^0 - \tan^{-1}(A_{V0}) - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{z}\right) \\ &\approx 90^0 - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{z}\right) \end{aligned}$$

The phase margin is improved by moving the non-dominant pole and zero to higher frequencies away from the unity-gain frequency. The phase margin can also be improved by using compensation techniques which place the zero in the left-half plane.

The slew rate is determined by the compensation capacitance and the tail current:

$$SR = \frac{I_{tail}}{C_C}$$

The performance characteristics of the two-stage amplifier are summarized below:

$$A_{V0} = g_{m1,2}\, g_{m8}\left(r_{ds2} \parallel r_{ds4}\right)\left(r_{ds7} \parallel r_{ds8} \parallel R_L\right)$$

$$\rho_1 = \frac{-1}{g_{m8}\left(r_{ds7} \parallel r_{ds8} \parallel R_L\right)C_C\left(r_{ds2} \parallel r_{ds4}\right)}$$

$$\rho_2 = \frac{-g_{m8}}{C_L}$$

$$z = \frac{g_{m8}}{C_C}$$

$$GBW = \frac{g_{m1,2}}{C_C}$$

$$SR = \frac{I_{tail}}{C_C}$$

$$PM \approx 90^0 - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{z}\right)$$

Monte Carlo Analysis

Monte Carlo analysis provides an accurate and powerful method for parametric yield estimation. The principle of Monte Carlo analysis can be defined as the generation of circuit figure-of-merit distributions as a function of statistically varying device model parameters that accurately reflect manufacturing process variations.

With Monte Carlo analysis, you can generate and save statistical information about a circuit's temperature and geometry-dependent performance characteristics. The mathematics supporting this Monte Carlo method proves that the probability distribution of the simulated results will be statistically the same as the actual measurements of a real circuit that has been fabricated.

These are the steps involved in Monte Carlo simulation using Analog Artist:

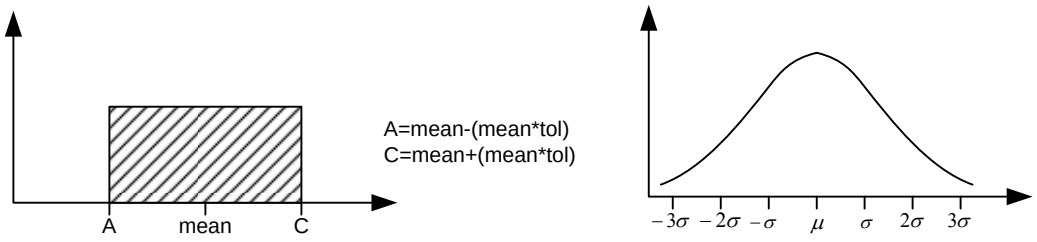
1) Assign statistical parameters to devices in the model file.
2) Setup the simulation environment and run a normal analog simulation.
3) Open Monte Carlo window
4) Define the expressions for Monte Carlo analysis using the calculator.
5) Add expressions to the Monte Carlo window.
6) Define the Monte Carlo simulation parameters.
7) Start the analysis.
8) Use the statistics functions to display and analyze the results.

There are two basic statistical distribution functions that you can apply to device parameters:

- Uniform
- Gaussian

The uniform distribution is defined with a mean value and a tolerance that defines the minimum and maximum values. Statistically, all values between the minimum and maximum values are equally likely to occur. Figure 9-11a shows a plot of a uniform distribution.

The Gaussian distribution is defined with a mean and a standard deviation. Statistically, values about the mean are more likely to occur than values within the tails. Almost all values fall within 3 standard deviations of the mean. Figure 9-11b shows a plot of a Gaussian distribution.



(a) (b)

Figure 9-11: a) Uniform distribution
b) Gaussian distribution

The syntax to include the statistical analysis in the model file is:

UNIFORM(mean,tol,seed)

GAUSS(mean,std_dev,seed)

For example, if you want to vary the threshold voltage by ±15 % using a Gaussian distribution, you would need to calculate what standard deviation to use. Since variations will fall within three standard deviations, the standard deviation needs to be 5 % of the mean. Assuming that the original threshold voltage in the model file is 0.7 V, then the standard deviation will be 0.035 V. Thus in the model file, replace the line:

VTH0=0.7 &

with:

VTH0=GAUSS(0.7,0.035,1) &

The most common analysis modes to perform are:

- Random variations
- Random variations with mismatch

With random variations, the parameters track exactly. All devices that share the same model file share the same model statement in the netlist. With random variations with mismatch, the system creates a separate model statement for each device.

Prelab

The prelab exercises are due at the beginning of the next lab period. No late work is accepted.

1) Design the operational amplifier of Figure 9-4 to obtain the following specifications:

A_{V0}	> 60 dB
CMRR	> 70 dB
GBW	> 1 MHz
PM	> 45º
Output Swing	> 1.5 V
R_{out}	< 1 kΩ
C_L	30 pF
R_L	1 kΩ
P_D	< 1.2 mW

Lab

1) Simulate the design from the prelab. Adjust transistor sizes until all specifications are met. Provide plots of frequency response, CMRR, $PSRR^+$, $PSRR^-$, and transient response. Include the slew rate, phase margin, gain-bandwidth product, and power dissipation in your report.
2) Layout your final design using good layout techniques. Include the "net-lists match" page in your report. Include the plots and data from part 1. Be sure to include parasitic capacitances in your extraction.
3) Run a Monte Carlo simulation on the opamp design. Vary the parameters VTH0 and U0 by 20% with a Gaussian distribution. Be sure to run this simulation with process variations and mismatch. Generate a histogram of the following parameters:
    - GBW
    - p_1
    - PM
    - A_{V0}

    Comment on the impact of process variations and mismatch on each parameter.