ANALOG ELECTRONICS

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – III

Subject Code	14XXX32	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Recall and Explain various BJT parameters, connections and configurations.
- Explain and Demonstrate BJT Amplifier, Hybrid Equivalent and Hybrid π Models.
- Recall and Explain construction and characteristics of JFETs and MOSFETs.
- Explain various types of FET biasing, and Demonstrate use of FET amplifiers.
- Demonstrate and Construct Frequency response of BJT and FET amplifiers at various frequencies.
- Define, Demonstrate and Analyze Power amplifier circuits in different modes of operation.
- Demonstrate and Apply Feedback and Oscillator circuits using FET.

Modules	Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1 **BJT AC Analysis** BJT modeling, r_e transistor model: Common Emitter Configuration, Voltage-Divider Bias, CE Emitter-Bias Configuration (Excluding Pspice Analysis), Emitter Follower Configuration, Determining Current Gain, Effect of R_L and R_S, Cascaded Systems, RC- Coupled BJT Amplifier, Cascode Connection, Darlington Connection. The Hybrid Equivalent Model, Approximate Hybrid Equivalent Circuit-Fixed Bias Configuration, Voltage Divider Configuration, Complete Hybrid Equivalent Model, Hybrid π Model. Relevant problems.	**10 Hours**	**L1, L2**
Module -2		
Field – Effect Transistors Introduction, Construction and Characteristics of JFETs, Transfer Characteristics- Derivation, Applying Schokley's Equation, Depletion Type MOSFET: Basic Construction, Basic Operation and Characteristics, P-Channel Depletion Type MOSFET and Symbols, Enhancement Type MOSFET-Basic Construction, Basic Operation and Characteristics, P-Channel Enhancement Type MOSFET and Symbols, CMOS. Relevant problems. **FET Biasing** Introduction, Fixed-Bias Configuration, Self-Bias Configuration, Voltage-Divider Biasing. Relevant problems.	**10 Hours**	**L1, L2**
Module -3		

FET Amplifiers Introduction, JFET Small Signal Model, JFET AC equivalent Circuit, Fixed- Bias Configuration, Self-Bias Configuration (Excluding Pspice Analysis), Voltage-Divider Configuration, Source Follower Configuration. Relevant problems. **BJT and JFET Frequency Response** General Frequency Considerations, Low Frequency Response- BJT Amplifier (Excluding Pspice Analysis) Low Frequency Response- FET Amplifier (Excluding Pspice Analysis), Miller Effect Capacitance, High Frequency Response- BJT Amplifier, High Frequency Response- FET Amplifier (Excluding Pspice Analysis), Multistage Frequency Effects. Relevant problems.	**10 Hours**	**L1, L2, L3**
Module -4		
Power Amplifiers Introduction: Definitions and Amplifier Types, Series Fed Class A Amplifier, Operation of Amplifier Stage, Transformer Coupled Class A Amplifier, Class B Amplifier Operation, Class B Amplifier Circuits: Transformer Coupled Push-Pull Circuits, Complementary –Symmetry Circuits, Amplifier Distortion, Class C and Class D Amplifier. Relevant Problems.	**10 Hours**	**L1, L2, L3, L4**
Module -5		
Feedback and Oscillator Circuits Feedback Concepts, Feedback Connection Types, Oscillator operation, Phase Shift Oscillator: FET Phase Shift Oscillator, Transistor Phase Shift Oscillator, Wien Bridge Oscillator, Tuned oscillator Circuit: FET and Transistor Colpitts Oscillator, FET and Transistor Hartley Oscillator, Crystal oscillator, Unijunction Oscillator. Relevant Problems.	**10 Hours**	**L2, L3**

Course outcomes:

After studying this course, students will be able to:

- Acquire knowledge of
  - Working principles, characteristics and basic applications of BJT and FET.
  - Single stage, cascaded and feedback amplifier configurations.
  - Frequency response characteristics of BJT and FET.
  - Power amplifier classifications such as Class A, Class B, etc.
- Analyse the performance of
  - r_e transistor model, π model.
  - FET amplifier in CS configuration.
  - Power Amplifiers and Oscillator circuits.
- Interpretation of performance characteristics of transistors amplifiers, frequency Response and Oscillators.
- Apply the knowledge gained in the design of transistorized circuits, amplifiers and Oscillators.

Graduate Attributes (as per NBA):

- Engineering Knowledge.
- Problem Analysis.
- Design / development of solutions (partly).
- Interpretation of data.

Question paper pattern:

- The question paper will have ten questions.

- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Robert L. Boylestad and Louis Nashelsky, "Electronics devices and Circuit theory", Pearson, 11th Edition, 2015, ISBN:9789332542600.

Reference Books:

1. I. J. Nagrath, "Electronics: Analog and Digital", PHI.
2. David A. Bell, "Electronic Devices and Circuits", Oxford University Press.

DIGITAL ELECTRONICS
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – III

Subject Code	14XXX33	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Describe, Illustrate and Analyze Combinational Logic circuits, Simplification of Algebraic Equations using Karnaugh Maps and Quine McClusky Techniques.
- Define and Describe Decoders, Encoders, Digital multiplexers, Adders and Subtractors, Binary comparators, Latches and Master-Slave Flip-Flops.
- Describe, Demonstrate, Analyze and Design of Mealy and Moore Models, Synchronous Sequential Circuits, State diagrams and Registers and Counters.

Modules	Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1 **Combinational Logic Design** Boolean Laws and Theorems, Sum-of-product and Product-of-sum Form, Karnaugh Map, Karnaugh Map with 'Don't Care' Conditions, Five Variable Karnaugh Map, Quine-McCluskey Minimisation Procedure: Reduction Techniques, Map Entered Variable Method. Relevant Problems.	**10 Hours**	**L2, L3, L4**
Module -2		
Logic Circuit Design: Arithmetic Operation Combinational Circuit, Binary Adder, Binary Substractor, Binary Parallel Adder, The Look-Ahead-Carry Binary Adders, Binary Multipliers, Binary Dividers, Comparator. Relevant Problems. **Logic Circuit Design: Data Processing** Introduction, Decoders: One-to-Two Line Decoder, Two-to-Four Line Decoder, Three-to-Eight Line Decoder, Encoders: Four-to-Two Line Encoder, Four-to-Two Line Priority Encoders, Multiplexers: Two-to-One Multiplexer, Four-to-One Multiplexer, Eight-to-One Multiplexer, Cascading of Multiplexers: Construction of Four-to-One Multiplexer, Eight-to-One Multiplexer using Two-to-One Multiplexer, Cascading of Multiplexers using Enable, Demultiplexers: One-to-Two Line Demultiplexer, One-to-Four Line Demultiplexer, Casacading of Demultiplexers: Construction of One-to-Four Line Demultiplexers using One-to-Two Line Demultiplexers, Cascading of Demultiplexers using Enable. Relevant Problems.	**10 Hours**	**L1, L2**
Module -3		

Flip-Flops Introduction, Basic Bistable Element, SR Latch: SR Latch using NOR Gates, Gated SR Latch using NOR Gates, SR Latch using NAND Gates, Gated SR Latch using NAND Gate, Characteristic of SR Latch, State Transition Diagram of SR Latch, Excitation Table of SR Latch, Triggering of Latches, D-Flip-Flop, JK Flip-Flop, T Flip-Flop, Race Around Condition, Master Slave Flip-Flop, Edge-Triggered Flip-Flop, Conversion of Flip-Flops: SR Flip-Flop to JK Flip-Flop. Relevant Problems.	**10 Hours**	**L1, L2**
Module -4		
Design of Sequential Circuits Introduction, Notations, Moore and Mealy Sequential Circuits, Analysis of Asynchronous Sequential Circuits: Fundamental Mode Asynchronous Sequential Circuit without Latches, Pulse Mode Asynchronous Sequential Circuit with Latches. Relevant Problems.	**10 Hours**	**L2, L3, L6**
Module -5		
Registers Introduction, Registers: Four Bit Latch, Shift Register, Serial In Serial Out Shift Register: Left-Shift Serial-In Serial-Out Register with D Flip-Flop, Serial-In Parallel-Out Shift Register, Parallel-In Serial-Out Shift Register: PISO Left-Shift Register, Ring Counter, Johnson Counter. Relevant Problems. **Counters** Introduction, Synchronous Counter, Modulus-4 Synchronus Up Counter, Modulus-4 Synchronus Down Counter, Modulus-4 Synchronus Up/Down Counter, Modulus-8 Synchronus Up Counter, Modulus-8 Synchronus Down Counter, Modulus-8 Synchronus Up/ Down Counter. Relevant Problems.	**10 Hours**	**L2, L3, L6**

Course outcomes:

After studying this course, students will be able to:

- Acquire knowledge of
  - Combinational Logic.
  - Simplification Techniques using Karnaugh Maps, Quine McClusky Technique.
  - Operation of Decoders, Encoders, Multiplexers, Adders and Subtractors.
  - Working of Latches, Flip-Flops,
  - Designing Registers, Counters.
  - Mealy, Moore Models and State Diagrams
- Analyse the performance of
  - Simplification Techniques using Karnaugh Maps, Quine McClusky Technique.
  - Synchronous Sequential Circuits.
- Interpretation of performance characteristics of Mealy and Moore Models.
- Apply the knowledge gained in the design of Counters, Registers and etc.

Graduate Attributes (as per NBA):

- Engineering Knowledge.
- Problem Analysis.
- Design / development of solutions (partly).
- Interpretation of data.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. D. P. Kothari and J. S Dhillon, "Digital Circuits and Design", Pearson, 2016, ISBN:9789332543539.

Reference Books:

1. Donald D. Givone, "Digital Principles and Design", McGraw Hill.
2. Charles H Roth, Jr., "Fundamentals of logic design", Cengage Learning.

ELECTRONIC INSTRUMENTATION

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – III

Subject Code	14XXX33	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Define and Describe accuracy and precision, types of errors, statistical and probability analysis.
- Describe basic functional concepts of various analog and digital measuring instruments.
- Describe basic concepts of microprocessor based instruments.
- Describe and Discuss functioning and types of oscilloscopes and signal generators, AC and DC bridges.
- Recognize and Describe significance and working of different types of transducers.

Modules	Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1 **Measurement and Error:** Definitions, Accuracy and Precision, Significant Figures, Types of Error, Statistical Analysis, Probability of Errors, Limiting Errors. Relevant problems. **Ammeters:** DC Ammeter, Multirange Ammeter, The Ayrton Shunt or Universal Shunt, Requirements of Shunt, Extending of Ammeter Ranges, RF Ammeter (Thermocouple), Limitations of Thermocouple, Effect of Frequency on Calibration, Measurements of Very Large Currents by Thermocouples. Relevant problems. **(Text 2)** **Voltmeters and Multimeters:** Introduction, Basic Meter as a DC Voltmeter, DC Voltmeter, Multirange Voltmeter, Extending Voltmeter Ranges, Loading, Transistor Voltmeter, Differential Voltmeter, Average Responding Voltmeter, Peak responding Voltmeter, True RMS Voltmeter, Considerations in Choosing an Analog Voltmeter, Multimeter. Relevant problems. **(Text 2)**	**10 Hours**	**L1, L2**
Module -2		
Digital Voltmeters: Introduction, RAMP technique, Dual Slope Integrating Type DVM, Integrating Type DVM, Most Commonly used principles of ADC, Successive Approximations, Continuous Balance DVM, $3\frac{1}{2}$-Digit, Resolution and Sensitivity of Digital Meters, General Specifications of DVM, Microprocessor based Ramp type DVM. Relevant Problems. **(Text 2)**	**10 Hours**	**L1, L2**

Digital Instruments: Introduction, Digital Multimeters, Digital Frequency Meter, Digital Measurement of Time, Universal Counter, Decade Counter, Electronic Counter, Digital Tachometer, Digital pH Meter, Digital Phase Meter, Digital Capacitance Meter, Microprocessor based Instruments. Relevant Problems. **(Text 2)**		
Module -3		
Oscilloscopes: Introduction, Basic principles, CRT features, Block diagram of Oscilloscope, Simple CRO, Vertical Amplifier, Horizontal Deflecting System, Sweep or Time Base Generator, Storage Oscilloscope, Digital Readout Oscilloscope, Measurement of Frequency by Lissajous Method, Probes for CRO, Digital Storage Oscilloscope. **(Text 2)** **Signal Generators:** Introduction, Fixed and Variable AF Oscillator, Standard Signal Generator, Laboratory Type Signal Generator, AF sine and Square Wave Generator, Function Generator, Square and Pulse Generator, Sweep Generator. **(Text 2)**	**10 Hours**	**L1, L2**
Module -4		
Measuring Instruments: Output Power Meters, Field Strength Meter, Stroboscope, Phase Meter, Vector Impedance Meter, Q Meter, Megger, Analog pH Meter, Telemetry. Relevant Problems. **(Text 2)** **Bridges:** Introduction, Wheatstone's bridge, Kelvin's Bridge; AC bridges, Capacitance Comparison Bridge, Inductance Comparison Bridge, Maxwell's bridge, Wein's bridge, Wagner's earth connection, Relevant Problems. **(Text 2)**	**10 Hours**	**L1, L2**
Module -5		
Transducers: Introduction, Electrical transducers, Selecting a transducer, Resistive transducer, Resistive position transducer, Strain gauges, Resistance thermometer, Thermistor, Inductive transducer, Differential output transducers, LVDT, Piezoelectric transducer, Photoelectric transducer, Photovoltaic transducer, Semiconductor photo diode and transistor, Temperature transducers-RTD. Relevant Problems. **(Text 2)**	**10 Hours**	**L1, L2**
Course outcomes: After studying this course, students will be able to: • Acquire knowledge of o Difference between accuracy and precision o Functioning of various types of analog and digital measuring instruments. o Different types of quantization, resolution and sensitivity in digital instruments such as frequency meters, tachometers, pH meters etc. o Microprocessor based instrumentation o Functioning of various types of Oscilloscopes and signal generators. o Different types of transducers in various applications.		

- Analyse the performance of
  - AC and DC bridges.
- Interpretation of performance characteristics of analog and digital measuring instruments.
- Understand the importance of life-long learning in the field of electronic instrumentation.

Graduate Attributes (as per NBA)

- Engineering Knowledge.
- Problem Analysis (partly).
- Life-long learning.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. A. D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1st Edition, 2015, ISBN:9789332556065.
2. H. S. Kalsi, "Electronic Instrumentation", McGraw Hill, 3rd Edition, 2012, ISBN:9780070702066.

Reference Books:

1. A. K. Sawhney, "Electronics and Electrical Measurements", Dhanpat Rai & Sons.
2. David A. Bell, "Electronic Instrumentation and Measurements", Oxford University Press.

MICROPROCESSORS AND MICROCONTROLLERS

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – III

Subject Code	14XXX35	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50	Exam Hours	03

CREDITS – 04

Course objectives: This course enables students to:

- Recall and Describe basics of Digital Computer, Microprocessors, Microcomputers and Microcontrollers.
- Discuss fundamentals of 8086 microprocessor architecture, pin diagram, etc.
- Discuss and Describe architecture of 8051 microcontroller, memory and I/O organization and addressing modes.
- Recall and Describe 8051 Instruction set, Timers and counters, serial communication.
- Demonstrate and Develop 8051 interfacing and applications.

Modules	Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1 **Microprocessor Introduction:** Digital Computer, Microprocessors, Microcomputers and Microcontrollers **(section 0.3, 1.1 of Text 1)**. **8086 Microprocessor**: Architecture – General Purpose Registers, Pointers, Segment Registers, Advantages of Segment Registers, PSW, Pin diagram in Minimum Mode **(Text 2)**.	**10 Hours**	**L1, L2**
Module -2		
8051 Microcontroller: Architecture, Registers, Pin diagram, I/O ports functions, Memory organization, External Memory (ROM & RAM) interfacing, Addressing Modes **(Text 1)**.	**10 Hours**	**L1, L2**
Module -3		
8051 Instruction Set: Data Transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Bit manipulation instructions, Stack and Subroutine instructions, Assembler directives, Assembly language program examples **(Text 1)**.	**10 Hours**	**L1, L2**
Module -4		
8051 Timers and Counters – Operation and Assembly language programming **(Text 1)**. **8051 Serial Communication**- Basics of Serial Data Communication, RS-232 standard, 9 pin RS232 signals, Assembly language programming for 8051 serial data transmission and reception, 8051 Interrupts and 8051 Assembly language Interrupts programming **(Text 1)**.	**10 Hours**	**L1, L2**

Module -5		
8051 Interfacing and Applications: Interfacing 8051 to simple switches and LEDs, LCD, ADC-0804 and Stepper motor and 8051 Assembly language Interfacing programming **(Text 1)**.	**10 Hours**	**L3, L4**

Course outcomes:

After studying this course, students will be able to:

- Acquire knowledge of
  - Architecture of 16 bit 8086 microprocessor.
  - Architecture, registers of 8051 microcontroller.
  - Instruction set of 8051 microcontroller.
  - Functioning of 8051 timers, counters and serial I/O.
  - 8051 interfacing and its applications.
- Apply the knowledge gained in the design of microprocessor and microcontroller based systems.
- Acquire competency in using tools such as assembler/ compiler.

Graduate Attributes (as per NBA)

- Engineering Knowledge.
- Design/ development of solutions.

Modern tool usage.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay, "The 8051 Microcontroller and Embedded Systems – using assembly and C", Pearson, 2nd Edition, 2006, ISBN:9788131710265.
2. Yu-cheng Liu and Glenn A. Gibson, "Microcomputer Systems - The 8086/8088 Family Architecture, Programming and Design", Pearson, 2nd Edition 2015, ISBN:9789332550087.

Reference Books:

1. Douglas Hall, "Microprocessors and Interfacing – Programming & Hardware", McGraw Hill.
2. Kenneth J. Ayala, "The 8051 Microcontroller Architecture, Programming & Applications", Thomson Learning.
3. Krishna Kant, "Microprocessors and Microcontrollers: Architecture, Programming, and System Design", PHI.

OOPs with C++ (Elective)

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – III

Subject Code	14XXX361	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40	Exam Hours	03

CREDITS – 03

Course objectives: This course enables students to:

- Describe the fundamental concepts of object-oriented Programming (OOP) and basics of C++ programming.
- Define and Describe Arrays, structure, union and pointers.
- Define and Describe Classes, objects, constructors, destructors, inheritance and polymorphism, Template and exception handling.

Modules	Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1 Fundamentals of OOPs , Basics of C++	**08 Hours**	**L1, L2**
Module -2		
Functions, Arrays, Structure, Union , Bit fields	**08 Hours**	**L1, L2**
Module -3		
Pointers, Classes and objects,	**08 Hours**	**L1, L2**
Module -4		
Constructors and Destructors, Inheritance,	**08 Hours**	**L1, L2**
Module -5		
Polymorphism, Template and exception handling	**08 Hours**	**L1, L2**

Course outcomes:

After studying this course, students will be able to:

- Acquire knowledge of
  - C++ basics and fundamental concepts of OOPs.
  - OOPs features such as classes, objects, inheritance and polymorphism.
  - Arrays, structures, union, bit fields and pointers.
  - Template and exception handling.
- Apply the knowledge gained in the
  - Understanding of Java and other object oriented programming languages.
  - Development of wide range of object oriented software packages.
- Acquire competency in using OOPs in different platforms.
- Understand the importance of life-long learning in the field of OOPs.

Graduate Attributes (as per NBA)

- Engineering Knowledge.
- Problem Analysis.
- Design/Development of solutions.
- Modern Tool Usage.
- Life-long learning.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.

- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Rakesh Shukla, "Object Oriented Programming in C++", Wiley India, 2013, ISBN: 9788126516582.
2. Herbert Schildt, "The Complete Reference C++", McGraw Hill, 4th Edition, 2003, ISBN:978007053532465.

Reference Books:

1. Stanley B.Lippmann and Josee Lajore, "C++ Primer", Pearson.
2. K. R. Venugopal, Rajkumar Buyya, and T. Ravi Shankar, "Mastering C++", McGraw Hill.

OPERATING SYSTEMS (Elective)

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – III

Subject Code	14XXX362	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40	Exam Hours	03

CREDITS – 03

Course objectives: This course enables students to:

- Define and Describe operating systems, Computer System architecture, Operating System structure, Operating System operations and services.
- Explain Process concept, Process scheduling, Operations on processes, Inter-process communication, Multi-Threaded Programming and Process management as a whole.
- Define and Discuss the Critical section problem, Peterson's solution, Synchronization hardware, Semaphores, Process synchronization and deadlocks in general.
- Define and Describe swapping, contiguous memory allocation, paging; tructure of page table, Segmentation Memory management of an Operating System.

Modules	Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1 **Introduction to Operating Systems, System structures:** What operating systems do; Computer System organization; Computer System architecture; Operating System structure; Operating System operations; Process management; Memory management; Storage management; Protection and security; Distributed system; Special-purpose systems; Computing environments. Operating System Services; User - Operating System interface; System calls; Types of system calls; System programs; Operating System design and implementation; Operating System structure; Virtual machines; Operating System generation; System boot.	**08 Hours**	**L1, L2**
Module -2		
Process Management: Process concept; Process scheduling; Operations on processes; Inter-process communication. Multi-Threaded Programming: Overview; Multithreading models; Thread Libraries; Threading issues. Process Scheduling: Basic concepts; Scheduling criteria; Scheduling algorithms; Multiple-Processor scheduling; Thread scheduling.	**08 Hours**	**L1, L2**
Module -3		
Process Synchronization: Synchronization: The Critical section problem; Peterson's solution; Synchronization hardware; Semaphores; Classical problems of	**08 Hours**	**L1, L2**

synchronization; Monitors.		
Module -4		
Deadlocks: Deadlocks: System model; Deadlock characterization; Methods for handling deadlocks; Deadlock prevention; Deadlock avoidance; Deadlock detection and recovery from deadlock.	**08 Hours**	**L1, L2**
Module -5		
Memory Management: Memory Management Strategies: Background; Swapping; Contiguous memory allocation; Paging; Structure of page table; Segmentation; Virtual Memory Management: Background.	**08 Hours**	**L1, L2**

Course outcomes:

After studying this course, students will be able to:

- Acquire knowledge of Operating system
  - Structure, operations and services.
  - Process and memory management.
  - Process scheduling, process synchronization and deadlock.
  - Virtual memory management.
- Apply the knowledge gained in the design of operating systems.
- Acquire competency in understanding different Operating Systems.
- Understand the importance of life-long learning in the field of Operating Systems.

Graduate Attributes (as per NBA)

- Engineering Knowledge.
- Design/Development of solutions.
- Life-long learning.

Question paper pattern:

- The question paper will have ten questions.
- Each full Question consists of 16 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Abraham Silberschatz, Peter Baer Galvin and Greg Gagne, "Operating System Principle", Wiley India, 8th Edition, 2009, ISBN:9788126520510.

Reference Books:

1. D.M Dhamdhere, "Operating systems - A concept based Approach", McGraw Hill.
2. P.C.P. Bhatt, "Introduction to Operating Systems: Concepts and Practice", PHI.
3. Harvey M Deital, "Operating systems", Pearson.

COMPUTER ORGANISATION (Elective)

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – III

Subject Code	14XXX363	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40	Exam Hours	03

CREDITS – 03

Course objectives: This course enables students to:

- Recall and Describe basic structure of computers, machine instructions and programs.
- Recall and Describe different addressing modes, output operations, Stacks and Queues, Subroutines and Additional Instructions, IEEE standard for Floating point Numbers.
- Write and Describe accessing I/O Devices, Interrupts, Direct Memory Access, Busses, Interface Circuits, and Standard I/O Devices.
- Describe Semiconductor RAM Memories, Read Only Memories, Cache Memories, Performance Considerations and Virtual Memories.
- Recall and Describe execution of a Complete Instruction, Multiple Bus Organization, Microprogrammed Control and Hardwired Control.

Modules	Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1 **Basic Structure of Computers:** Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance – Processor Clock, Basic Performance Equation. **Machine Instructions and Programs:** Numbers, Arithmetic Operations and Characters, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing.	**08 Hours**	**L1, L2**
Module -2		
Machine Instructions and Programs (Continued): Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions. IEEE standard for Floating point Numbers (6.7.1 of Chapter 6)	**08 Hours**	**L1, L2**
Module -3		
Input/output Organization: Accessing I/O Devices, Interrupts, Direct Memory Access, Busses, Interface Circuits, Standard I/O Devices.	**08 Hours**	**L1, L2**
Module -4		
Memory System: Some Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Cache Memories, Performance Considerations, Virtual Memories.	**08 Hours**	**L1, L2**
Module -5		

Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Microprogrammed Control, Hardwired Control.	**08 Hours**	**L1, L2**

Course outcomes:

After studying this course, students will be able to:

- Acquire knowledge of
  - The basic structure of computers & machine instructions and programs.
  - Addressing Modes, Assembly Language,
  - Stacks, Queues and Subroutines.
  - Input/output Organization such as accessing I/O Devices, Interrupts.
  - Memory system basic Concepts, Semiconductor RAM Memories, Static memories, Asynchronous DRAMS, Read Only Memories, Cache Memories and Virtual Memories.
  - Some Fundamental Concepts of Basic Processing Unit, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control and Microprogrammed Control.
- Apply the knowledge gained in the design of Computer.
- Acquire competency in understanding computer organisation.
- Understand the importance of life-long learning in the field of computer organisation.

Graduate Attributes (as per NBA)

- Engineering Knowledge.
- Problem Analysis.
- Life-long learning.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, “Computer Organization”, McGraw Hill, 5th Edition, 2015, ISBN:9781259005275.

Reference Books:

1. David A. Patterson, John L. Hennessy, “Computer Organization and Design – The Hardware / Software Interface ARM”, Elsevier.
2. William Stallings, “Computer Organization & Architecture”, Pearson.
3. Vincent P. Heuring & Harry F. Jordan, “Computer Systems Design and Architecture”, Pearson.

DESIGN AND ANALYSIS OF ALGORITHMS (Elective)

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – III

Subject Code	14XXX364	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40	Exam Hours	03

CREDITS – 03

Course objectives: This course enables students to:

- Describe and Analyze non-recursive and recursive algorithms.
- Recall and Describe binary search, merge Sort and quick sort.
- Explain asymptotic performance of algorithms.
- Describe and Analyze greedy method and dynamic programming.
- Explain decrease-and-conquer approaches and space-time tradeoffs.

Modules	Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module-1 **Introduction:** Notion of Algorithm, Review of Asymptotic Notations, Mathematical Analysis of Non-Recursive and Recursive Algorithms **Brute Force Approaches:** Introduction, Selection Sort and Bubble Sort, Sequential Search and Brute Force String Matching.	**08 Hours**	**L1, L2, L4**
Module -2		
Divide and Conquer: General Method, Defective Chess Board, Binary Search, Merge Sort, Quick Sort and its performance.	**08 Hours**	**L1, L2**
Module -3		
The Greedy Method: The General Method, Knapsack Problem, Job Sequencing with Deadlines, Minimum-Cost Spanning Trees: Prim's Algorithm, Kruskal's Algorithm; Single Source Shortest Paths.	**08 Hours**	**L1, L2**
Module -4		
Dynamic Programming: The General Method, Warshall's Algorithm, Floyd's Algorithm for the All-Pairs Shortest Paths Problem, Single-Source Shortest Paths: General Weights, 0/1 Knapsack, The Traveling Salesperson problem.	**08 Hours**	**L1, L2, L3**
Module -5		
Decrease-and-Conquer Approaches: Introduction, Insertion Sort, Depth First Search and Breadth First Search, Topological Sorting, **Space-Time Tradeoffs:** Introduction, Sorting by Counting, Input Enhancement in String Matching.	**08 Hours**	**L1, L2, L3**

Course outcomes:

After studying this course, students will be able to:

- Acquire knowledge of

- Algorithms using inductive proofs and invariants.
- Worst-case running times of algorithms using asymptotic analysis.
- Dynamic-programming paradigm.
- Greedy algorithms and its sustainability.
- Major graph algorithms and analyses.

- Apply the knowledge gained in the design of Algorithm.
- Acquire competency in using different Algorithms.
- Understand the importance of research in the field of Algorithms.

Graduate Attributes (as per NBA)

- Engineering Knowledge.
- Problem Analysis.
- Design/Development of solutions.
- Life-long learning.

Question paper pattern:

- The question paper will have ten questions.
- Each full Question consists of 16 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Anany Levitin, "Introduction to the Design & Analysis of Algorithms", Pearson, 2nd Edition, 2007, ISBN:9780321358288 (Listed topics only from the Chapters 1, 2, 3, 5, 7 and 8).
2. Ellis Horowitz, Sartaj Sahni, Sanguthevar Rajasekaran, "Fundamentals of Computer Algorithms", Universities Press, 2nd Edition, 2007, ISBN: 9788173716126 (Listed topics only from the Chapters 3, 4, 5).

Reference Books:

1. Thomas H. Cormen, Charles E. Leiserson, Ronal L. Rivest, Clifford Stein, "Introduction to Algorithms", PHI.
2. R. C. T. Lee, S. S. Tseng, R. C. Chang & Y. T. T Sai, "Introduction to the Design and Analysis of Algorithms A Strategic Approach", McGraw Hill.

ANALOG ELECTRONICS LABORATORY

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – III

Laboratory Code	14XXL37	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory	Exam Marks	80
		Exam Hours	03

CREDITS – 02

Course objectives: This laboratory course enables students to get practical experience in design, assembly and evaluation/testing of

- Rectifiers and Voltage Regulators.
- BJT characteristics and Amplifiers.
- JFET Characteristics and Amplifiers.
- MOSFET Characteristics.
- Power Amplifiers.
- RC-Phase shift, Hartley, Colpitt's and Crystal Oscillators.

Laboratory Experiments: **NOTE: The experiments are to be carried using discrete components only.**	**Revised Bloom's Taxonomy (RBT) Level**
1. To design and set up the following rectifiers with and without filters: (a) Full Wave Rectifier (b) Bridge Rectifier To determine ripple factor and conversion efficiency.	**L5, L6**
2. To plot load regulation characteristics using zener diode and calculate the percentage load regulation.	**L2, L3, L4**
3. To plot the input and output characteristics of a NPN transistor in common emitter configuration and calculate the dynamic input resistance, dynamic output resistance and common emitter current gain.	**L2, L3, L4**
4. To design and set up the common emitter amplifier under voltage divider bias with and without feedback and determine the gain-bandwidth product from its frequency response.	**L5, L6**
5. To design and setup common collector amplifier (Emitter Follower) using voltage divider bias and to determine gain-bandwidth product from its frequency response.	**L5, L6**
6. To plot the input and output characteristics of a JFET and calculate its parameters, namely; drain dynamic resistance, mutual conductance and amplification factor.	**L2, L3, L4**
7. To design, setup and plot the frequency response of Common Source JFET amplifier, and obtain the bandwidth.	**L5, L6**
8. To plot the input and output characteristics of n-channel MOSFET and calculate its parameters, namely; drain dynamic resistance, mutual conductance and amplification factor.	**L2, L3, L4**

9. To set up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency.	**L2, L3, L4**
10. To design and setup the RC-Phase shift Oscillator using BJT, and calculate the frequency of output waveform.	**L5, L6**
11. To design and setup the following tuned oscillator circuits using BJT, and determine the frequency of oscillation. (a) Hartley Oscillator (b) Colpitts Oscillator	**L5, L6**
12. To design and setup the crystal oscillator and determine the frequency of oscillation.	**L5, L6**

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Design and Test rectifiers and voltage regulators.
- Compute the parameters from the characteristics of BJT, JFET and MOSFET devices.
- Design, Test and Evaluate BJT amplifiers in CE and CC configurations.
- Design and Test JFET amplifiers.
- Design and Test a power amplifier.
- Design and Test various types of oscillators.

Graduate Attributes (as per NBA)

- Engineering Knowledge.
- Problem Analysis.
- Design/Development of solutions.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Students are allowed to pick one experiment from the lot.
3. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
4. Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

Reference Book:

1. K. A. Navas, "Electronics Lab Manual", Volume I, PHI, 5th Edition, 2015, ISBN:9788120351424

DIGITAL ELECTRONICS and INTERFACING LABORATORY

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER - III

Laboratory Code	14XXL38	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory	Exam Marks	50
		Exam Hours	03

CREDITS – 02

Course objectives: This laboratory course enables students to get practical experience:

- in design, realisation and verification of
  - Demorgan's Theorem.
  - Full/Parallel Adders and Subtractors.
  - Multiplexer using logic gates
  - Demux and Decoder
  - Flip-Flops, Shift registers and Counters
- in interfacing microcontroller to
  - Toggle Switch and LEDs
  - LCD
  - Stepper Motor
  - Light dependant resistor (LDR) , a relay and buzzer.

Laboratory Experiments: **NOTE:** Use discrete components to test and verify the logic gates. Multisim may be used for designing the gates along with the above.	**Revised Bloom's Taxonomy (RBT) Level**
1. To verify (a) Demorgan's Theorem for 2 variables (b) The sum-of product and product-of-sum expressions using universal gates.	**L1, L2, L3**
2. To design and implement (a) Full Adder using basic logic gates. (b) Full subtractor using basic logic gates.	**L5, L6**
3. To design and implement 4-bit Parallel Adder/ subtractor using IC 7483.	**L5, L6**
4. To realize (a) 4:1 Multiplexer using gates (b) 3-variable function using IC 74151(8:1 MUX) (c) 1:8 Demux and 3:8 Decoder using IC74138	**L2, L3**
5. To realise the following flip-flops using NAND Gates. (a) Clocked SR Flip-Flop (b) JK Flip-Flop	**L2, L3**
6. To realize the following shift registers using IC7474 (a) SISO (b) SIPO (c)PISO (d) PIPO	**L2, L3**
7. To realize the Ring Counter and Johnson Counter using IC7476	**L2, L3**
8. To realize the Mod-N Counter using IC7490	**L2, L3**
9. To Interface 8051 to a toggle Switch and 8 LEDs to light up LEDs alternatively when the Switch is ON (in Assembly	**L4, L5, L6**

language).	
10. To Interface 8051 to LCD to display a message (in C Language).	**L4, L5, L6**
11. To Interface 8051 to Stepper Motor to rotate the motor for a given number of steps (C language programming).	**L4, L5, L6**
12. Interface a Light dependant resistor (LDR), a relay and buzzer to make a light operated switch (in Assembly language).	**L4, L5, L6**

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Demonstrate the truth table of various logic gates.
- Design, Test and Evaluate various combinational circuits such as adders, subtractors, multipliers, comparators, parity generators, multiplexers and de-Multiplexers.
- Construct flips-flops, counters and shift registers.
- Develop and Test interfacing of 8051 Microcontroller to various devices.

Graduate Attributes (as per NBA)

- Engineering Knowledge.
- Problem Analysis.
- Design/Development of solutions.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Students are allowed to pick one experiment from the lot.
3. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
4. Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

Reference Book (For 1 to 6 experiments):

1. K. A. Navas, "Electronics Lab Manual", Volume I, PHI, 5th Edition, 2015, ISBN:9788120351424.