M. Tech. DEGREE

VLSI SYSTEMS

SYLLABUS

FOR

CREDIT BASED CURRICULUM

(2009 -2010)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY

TIRUCHIRAPPALLI – 620 015, INDIA.

CURRICULUM

I-SEMESTER

CODE	COURSE OF STUDY	L- T- P- C
MA617	Graph Theory and Discrete Optimization	3 - 0 - 0 – 3
EC651	Analog VLSI	3 - 0 - 0 – 3
EC653	Basics of VLSI	3 – 0 - 0 – 3
EC655	Digital System Design	3 – 0 - 0 – 3
	Elective I	3 – 0 - 0 – 3
	Elective II	3 – 0 - 0 – 3
EC657	HDL Programming Laboratory	0 – 0 - 3 – 2
		18 - 0 - 3 – 20

II-SEMESTER

EC652	VLSI System Testing	3 - 0 - 0 – 3
EC654	Electronic Design Automation Tools	3 - 0 - 0 – 3
EC656	Designing with ASICs	3 - 0 – 0 – 3
	Elective III	3 - 0 – 0 – 3
	Elective IV	3 - 0 – 0 – 3
	Elective V	3 - 0 – 0 – 3
EC658	Analog IC Design Laboratory	0 - 0 – 3 – 2
EC660	ASIC – CAD Laboratory	0 - 0 – 3 – 2
		18 – 0 – 6 –22

III-SEMESTER

EC697	Project – Phase I	**0 - 0– 24 – 12**

IV-SEMESTER

EC698	Project - Phase II	**0 - 0 –24 – 12**

ELECTIVES

I-SEMESTER

EC659	Modeling and Synthesis with Verilog HDL	3 - 0 - 0 – 3
EC661	Digital Signal Processing structures for VLSI	3 - 0 - 0 – 3
EC605	High Speed Communication Networks	3 – 0 - 0 – 3
EC615	Digital Image Processing	3 – 0 – 0 – 3

II-SEMESTER

EC612	Architecture of DSPs	3 – 0 – 0 – 3
EC662	FPGA - based System Design	3 - 0 - 0 – 3
EC664	VHDL Analysis and Design of Digital Systems	3 - 0 - 0 – 3
EC666	Low Power VLSI circuits	3 - 0 - 0 – 3
EC668	VLSI Digital Signal Processing Systems	3 - 0 - 0 – 3
EC670	Asynchronous System Design	3 - 0 - 0 – 3

ADDITIONAL ELECTIVES APPROVED BY BoS

EC663	VLSI Technology	3 - 0 - 0 – 3
EC665	Advanced Computer Architecture	3 - 0 - 0 – 3
EC672	Advanced Digital Design	3 - 0 - 0 – 3
EC674	Physical Design Automation	3 - 0 - 0 – 3
EC676	Mixed - Signal Circuit Design	3 - 0 - 0 – 3

MA617 Graph Theory And Discrete Optimization (3 – 0 - 0) 3

Basic definitions, Degree of vertices, Complement of a graph. Self complementary gr

aph, Some eccentricity properties of graphs. Tree, spanning tree. Directed graphs standard definitions; strongly, weakly, unilaterally connected digraphs, deadlock communication network. Matrix representation of graph and digraphs. Some properties(proof not expected).

Eulerian graphs and standard results relating to characterization. Hamiltonian graph-standard theorems (Dirac theorem, Chavathal theorem, closure of graph).Non Hamiltonian graph with maximum number of edges. Self-centered graphs and related simple theorems. Chromatic number; Vertex and edge(only properties and examples)-application to colouring. Planar graphs, Euler's formula, maximum number of edges in a planar graph. Five colour theorem.

DFS-BFS algorithm ,shortest path algorithm, min-spanning tree and max-spanning tree algorithm, planarity algorithm. matching theory, maximal matching ,algorithms for maximal matching. Perfect matching(only properties and applications to regular graphs).

Flows in graphs, Ranking of participants in tournaments, simple properties and theorems on strongly connected tournaments. Application of Eulerian digraphs. PERT-CPM. Complexity of algorithms; P-NP-NPC-NP hard problems and examples.

Linear- Integer Linear programming, Conversion of TSP, maxflow, Knapsack scheduling ,shortest path problems for Linear programming types - branch bound method to solve Knapsack problems- critical path and linear programming conversion- Floor shop scheduling problem- Personal assignment problem.
Dynamic programming- TSP- compartment problems- Best investment problems.

Text Books:

1. *C.Papadimitriou & K.Steiglitz,Combinatorial Optimization, Prentice Hall, 1982.*
2. *H.Gerez, Algorithms for VLSI Design Automation, John Wiley, 1999.*

Reference Books:

1. *B.Korte & J.Vygen, Combinatorial Optimization, Springer-Verlag, 2000.*
2. *W.J.COOK ETAL: Combinatorial Optimization, John Wiley, 1997.*
3. *G.L.NEMHAUSER & L.A.WOLSEY: Integer and Combinatorial Optimization, John Wiley,1999.*

EC651 Analog VLSI (3 – 0 - 0) 3

Advanced MOS modeling, BJT modeling , CS, CD and CG amplifiers. Current mirrors – active loads. High input impedance current mirrors. BJT gain stages.

CMOS operational amplifiers- compensation. Comparators. Sample and hold circuits

MOS, CMOS and Bi CMOS S/H circuits. Switched capacitor filters, operation, analysis and applications.

Nyquist rate. D/A converters. A/D converters.

Over sampling techniques, filter design.

Text Books:

1. *D.A.John & K.Martin, Analog Integrated Circuit Design, Wiley , 1997.*
2. *B.Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2000*

Reference Books:

1. *P.E. Allen & D.R. Holberg, CMOS Analog Circuit Design, Oxford University Press, 2002*
2. M. Ismail & T.Fiez, Analog VLSI, McGraw Hill, 1994
3. Gregolian & temes, Analog MOS integrated Circuits , John Wiley , 1986.

EC653 Basics of VLSI (3 – 0 - 0) 3

Introduction to CMOS circuits: MOS transistors, CMOS combinational logic gates, multiplexers, latches and flip-flops. CMOS fabrication and layout. VLSI design flow.

MOS transistor theory: Ideal I-V and C-V characteristics, non ideal I-V effects, DC transfer characteristics. Switch level RC delay models.

CMOS technologies. Layout design rules. CMOS process enhancement. Technology related CAD issues.

Circuit characterization and performance estimation: Delay estimation. Logical effort and transistor sizing. Power dissipation. Interconnect design margin. Reliability. Scaling.

Combinational circuit design: Static CMOS, Ratioed circuits, Cascode voltage switch logic, Dynamic circuits, Pass transistor circuits. More circuit families. Comparison of circuit families.

Text Books:

1. *N.H.E.Weste etal, CMOS VLSI Design (3/e), Pearson, 2005*
2. Pucknell & Eshraghian: Basic VLSI Design , (3/e), PHI, 1996.

Reference Books:

1. Weste : Principle of CMOS VLSI design, Addition Wesley, 1994
2. M. Conway : Introduction to VLSI Systems, Addition Wesley, 1980.
3. A.Mukherjie :Introduction to NMOS and CMOS Systems Design, Prentice Hall, 1986.

EC655 Digital System Design (3 – 0 - 0) 3

Programmable logic devices (PLDs). Programmable gate arrays. Xilinx series FPGAs and CPLDs. Altera series CPLDs and FPGAs.

FPGA- based system design. FPGA fabrics. Combinational network delay. Power and energy optimization sequential machine design styles. Rules for clocking. Performance analysis.

Sequencing static circuits. Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.

Datapath and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context-addressable memory.

Basics of Testing: Fault models. Combinational logic and fault simulation: Preliminaries, Logic simulation, Fault simulation essentials. Test generation for combinational circuits: Test generation basics, structural test generation & non- structural test generation, test generation systems. Test generation: Synchronous circuits and Asynchronous circuits

Text Books:

1. *N.H.E.Weste etal, CMOS VLSI Design (3/e), Pearson, 2005*
2. *W.Wolf, FPGA- based System Design, Pearson, 2004*

Reference Books:

1. *N. Jha & S.D. Gupta, Testing of Digital Systems, Cambridge, 2003.*
2. R.F.Tinder: Engineering Digital Design, (2/e), Academic Press, 2000

EC652 VLSI System Testing (3 – 0 - 0) 3

Combinational ATPG. Current sensing based testing. Classification of sequential ATPG methods. Fault collapsing and simulation

Universal test sets. Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

CMOS testing: Testing of static and dynamic circuits. Fault diagnosis: Fault models for diagnosis, Cause-effect diagnosis, Effect-cause diagnosis.

Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives.

Built-in self-test: Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

Text Books:

1. *N. Jha & S.D. Gupta, Testing of Digital Systems, Cambridge, 2003.*
2. *M. Abramovici etal, Digital System Testing and Testable Design, Computer Science Press, 1990*

Reference Books:

1. *P.K.LALA: Digital Circuit Testing and Testability, Academic Press, 1999.*
2. *P.K.LALA: Self checking and Fault-tolerant Digital Design, Academic Press, 1999.*
3. *M.L.BUSHNELL & V.D.AGARWAL: Essentials of Electronic Testing for Digital, Memory and Mixed signal VLSI circuits, Kluwer, 2000.*

EC654 Electronic Design Automation Tools (3 – 0 - 0) 3

An overview of OS commands. System settings and configuration. Introduction to Unix commands. Writing Shell scripts. VLSI design automation tools.An overview of the features of practical CAD tools. Modelsim, Leonardo spectrum, ISE 8.1i, Quartus II, VLSI backend tools.

Synthesis and simulation using HDLs-Logic synthesis using verilog and VHDL. Memory and FSM synthesis. Performance driven synthesis, Simulation- Types of simulation. Static timing analysis. Formal verification. Switch level and transistor level simulation.

Circuit simulation using Spice - circuit description. AC, DC and transient analysis. Advanced spice commands and analysis. Models for diodes, transistors and opamp. Digital building blocks. A/D, D/A and sample and hold circuits. Design and analysis of mixed signal circuits.

Mixed signal circuit modeling and analysis using VHDL –AMS,

System design using systemC- SystemC models of computation. Classical hardware modeling in system C. Functional modeling. Parametrized modules and channels. Test benches. Tracing and debugging.

Text Books:

1. *M.J.S.Smith, Application Specific Integrated Circuits,Pearson,2002*
2. *M.H.Rashid, Spice for Circuits and Electronics using Pspice. (2/e), PHI.*

Reference Books:

1. *T. Grdtker et al , System Design with SystemC, Kluwer, 2004.*
2. *P.J. Ashenden et al , The System Designer's Guide to VHDL-AMS, Elsevier, 2005*

EC656 Designing with ASICs (3 – 0 - 0) 3

Types of ASICs. ASIC design flow. Programmable ASICs. Antifuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects.

An overview of advanced FPGAs and programmable SOCs **:** Architecture and configuration of Spartan and Virtex FPGAs . Apex and Cyclone FPGAs. Virtex PRO kits and Nios kits. OMAP. ASIC physical design issues. **s**ystem partitioning, interconnect delay models and measurement of delay.

ASIC floor planning, placement and routing.

Design issues in SOC. Design methodologies. Processes and flows. Embedded software development for SOC. Techniques for SOC testing. Configurable SOC. Hardware/software codesign.

High performance algorithms for ASICs/ SOCs. SOC case studies- DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. Case Studies: Digital camera, Bluetooth radio/modem, SDRAM and USB controllers.

Text Books:

1. *M.J.S. Smith : Application Specific Integrated Circuits,,Pearson,2003.*
2. *H.Gerez, Algorithms for VLSI Design Automation, John Wiley, 1999.*

Reference Books:

1. *K.K.Parhi, VLSI Digital Signal Processing Systems, John-Wiley, 1999.*

EC659 Modeling and Synthesis with Verilog HDL (3 – 0 - 0) 3

Hardware modeling with the verilog HDL. Encapsulation, modeling primitives, different types of description.

Logic system, data types and operators for modeling in verilog HDL. Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection.

Behavioral descriptions in verilog HDL. Synthesis of combinational logic.

HDL-based synthesis- technology-independent design, styles for synthesis of combinational and sequential logic, synthesis of finite state machines, synthesis of gated clocks, design partitions and hierarchical structures.

Synthesis of language constructs, nets, register variables, expressions and operators, assignments and compiler directives. Switch-level models in verilog. Design examples in verilog.

Text Books:

1. *M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.*
2. *S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.*

Reference Books:

1. *M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.*

EC661 Digital Signal Processing Structures for VLSI (3 – 0 - 0)3

An overview of DSP concepts-Linear system theory, DFT, FFT, realization of digital filters. Typical DSP algorithms, DSP applications. Data flow graph representation of DSP algorithm.

Loop bound and iteration bound Retiming and its applications.

Algorithms for fast convolution. Algorithmic strength reduction in filters and transforms. DCT and inverse DCT. Parallel FIR filters. Pipelining of FIR filters. Parallel processing. Pipelining and parallel processing for low power.

Pipeline interleaving in digital filters. Pipelining and parallel processing for IIR filters.Low power IIR filter design using pipelining and parallel processing, Pipelined adaptive digital filters.

Round off noise and its computation. State variable description of digital filters, Round off noise computation using state variable description. Scaling using slow-down, retiming and pipelining.

Text Book:

1. *K.K.Parhi, VLSI Digital Signal Processing Systems, John-Wiley, 1999.*

Reference Books:

1. *U. Meyer – Baese , Digital Signal Processing with FPGAs, Springer, 2004*

EC662 FPGA - based System Design (3 – 0 - 0) 3

Multirate signal processing- Decimation and Interpolation. Spectrum of decimated and interpolated signals, Polyphase decomposition of FIR filters and its applications to multirate DSP. Sampling rate converters, Sub-band encoder.

Filter banks-uniform filter bank. direct and DFT approaches. Introduction to ADSL Modem. Discrete multitone modulation and its realization using DFT. QMF. Short time Fourier Transform Computation of DWT using filter banks. Implementation and verification on FPGAs.

DDFS- ROM LUT approach. Spurious signals, jitter. Computation of special functions using CORDIC. Vector and rotation mode of CORDIC. CORDIC architectures. Implementation and verification on FPGAs.

Block diagram of a software radio. Digital downconverters and demodulators Universal modulator and demodulator using CORDIC. Incoherent demodulation - digital approach for I and Q generation, special sampling schemes. CIC filters. Residue number system and high speed filters using RNS. Down conversion using discrete Hilbert transform. Undersampling receivers, Coherent demodulation schemes.

Speech coding- speech apparatus. Models of vocal tract. Speech coding using linear prediction. CELP coder. An overview of waveform coding. Vocoders. Vocoder attributes. Block diagrams of encoders and decoders of G723.1, G726, G727, G728 and G729.

Text Books:

1. *J. H. Reed, Software Radio, Pearson, 2002.*
2. *U. Meyer – Baese , Digital Signal Processing with FPGAs, Springer, 2004*

Reference Books:

1. *Tsui, Digital Techniques for Wideband receivers, Artech House,2001.*
2. *S. K. Mitra, Digital Signal processing, McGrawHill, 1998*

EC664 VHDL Analysis and Design of Digital Systems (3 – 0 -0) 3

An overview of design procedures for system design using CAD tools. Design verification tools. Examples using commercial PC based VLSI CAD tools. Design methodology based on VHDL. Basic concepts and structural descriptions in VHDL.

Characterizing hardware languages, objects and classes, signal assignments, concurrent and sequential assignments. Structural specification of hardware.

Design organization, parameterization and high level utilities, definition and usage of subprograms, packaging parts and utilities, design parameterization, design configuration, design libraries. Utilities for high-level descriptions.

Data flow and behavioral description in VHDL- multiplexing and data selection, state machine description, open collector gates, three state bussing, general dataflow circuit, updating basic utilities. Behavioral description of hardware.

CPU modelling for discrete design- Parwan CPU, behavioral description, bussing structure, data flow, test bench, A more realistic Parwan. Interface design and modeling, VHDL as a modeling language.

Text Books:

1. *Z.Navabi, VHDL Analysis and Modeling of Digital Systems, (2/e), McGraw Hill, 1998.*
2. *Perry, VHDL (3/e), McGraw Hill.2002*

EC666 Low Power VLSI Circuits (3 – 0 - 0) 3

Evolution of CMOS technology. 0.25 μm and 0.1 μm technologies. Shallow trench isolation. Lightly-doped drain. Buried channel. BiCMOS and SOI CMOS technologies. Second order effects and capacitance of MOS devices.

CMOS inverters, static logic circuits of CMOS, pass transistor, BiCMOS, SOI CMOS and low power CMOS techniques.

Basic concepts of dynamic logic circuits. Various problems associated with dynamic logic circuits. Differential, BiCMOS and low voltage dynamic logic circuits.

Different types of memory circuits.

Adder circuits. Multipliers, advanced structures. PLA. PLL. Processing unit.

Text Books:

1. *J.B.Kuo & J.H.Lou, Low-voltage CMOS VLSI Circuits, Wiley., 1999.*
2. A.Bellaowar & M.I.Elmasry: Low power Digital VLSI Design, Circuits and Systems, Kluwer,1996.

EC668 VLSI Digital Signal Processing Systems (3 – 0 - 0) 3

Transformations for retiming. Folding and unfolding DSP programs.

Bit level arithmetic structures- parallel multipliers, interleaved floor plan and bit plan based digital filters. Bit serial multipliers. Bit serial filter design and implementation . Canonic signed digit arithmetic, Distributed arithmetic.

Redundant arithmetic, redundant number representations , carry free radix 2 addition and subtraction . Hybrid radix 4 addition. Radix 2 hybrid redundant multiplication architectures , data format conversion. Redundant to nonredundant converter. Numerical strength reduction.

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining. Implementation of wave-pipelined systems. Asynchronous pipelining.

Scaling versus power consumption. Power analysis, power reduction techniques, power estimation techniques. Low power IIR filter design .Low power CMOS lattice IIR filter.

Text Book:

1. *K.K. Parhi : VLSI Digital Signal Processing systems, John Wiley, 1999.*

EC670 Asynchronous System Design (3 – 0 - 0) 3

Fundamentals: Handshake protocols, Muller C-element, Muller pipeline, Circuit implementation styles, theory. Static data-flow structures: Pipelines and rings, Building blocks, examples

Performance: A quantitative view of performance, quantifying performance, Dependency graphic analysis. Handshake circuit implementation: Fork, join, and merge, Functional blocks, mutual exclusion, arbitration and metastability.

Speed-independent control circuits: Signal Transition graphs, Basic Synthesis Procedure, Implementation using state-holding gates, Summary of the synthesis Process, Design examples using Petrify. Advanced 4-phase bundled data protocols and circuits: Channels and protocols, Static type checking, More advanced latch control circuits.

High-level languages and tools: Concurrency and message passing in CSP, Tangram program examples, Tangram syntax-directed compilation, Martin's translation process, Using VHDL for Asynchronous Design. An Introduction to Balsa: Basic concepts, Tool set and design flow, Ancillary Balsa Tools

The Balsa language: Data types, Control flow and commands, Binary/Unary operators, Program structure. Building library Components: Parameterized descriptions, Recursive definitions. A simple DMA controller: Global Registers, Channel Registers, DMA control structure, The Balsa description.

Principles of Asynchronous Circuit Design - Jens Sparso, Steve Furber, Kluver Academic Publishers.

Text Books:

1. *Asynchronous Circuit Design- Chris. J. Myers, John Wiley & Sons,2001.*
2. *Handshake Circuits An Asynchronous architecture for VLSI programming – Kees Van Berkel Cambridge University Press, 2004*

Reference Book:

1. *Principles of Asynchronous Circuit Design-Jens Sparso, Steve Furber, Kluver Academic Publishers, 2001.*

EC663 VLSI Technology (3 – 0 - 0) 3

Electron grade silicon. Crystal growth. Wafer preparation. Vapour phase and molecular beam epitaxy. SOI. Epitaxial evaluation. Oxidation techniques, systems and properties. Oxidation defects.

Optical, electron, X-ray and ion lithography methods. Plasma properties, size, control, etch mechanism, etch techniques and equipments.

Deposition process and methods. Diffusion in solids. Diffusion equation and diffusion mechanisms.

Ion implantation and metalisation. Process simulation of ion implementation, diffusion, oxidation, epitaxy, lithography, etching and deposition. NMOS, CMOS, MOS memory and bipolar IC technologies. IC fabrication.

Analytical and assembly techniques. Packaging of VLSI devices.

Text Books:

1. *S.M.Sze, VLSI Technology (2/e) , McGraw Hill, 1988*
2. *W. Wolf, Modern VLSI Design, (3/e), Pearson,2002*

EC665 Advanced Computer Architecture (3 – 0 - 0) 3

Multiprocessors and multi-computers. Multi-vector and SIMD computers. PRAM and VLSI Models. Conditions of parallelism. Program partitioning and scheduling. Program flow mechanisms. Parallel processing applications. Speed up performance law.

Advanced processor technology. Superscalar and vector processors. Memory hierarchy technology. Virtual memory technology. Cache memory organization. Shared memory organization.

Linear pipeline processors. Non linear pipeline processors. Instruction pipeline design. Arithmetic design. Superscalar and super pipeline design. Multiprocessor system interconnects. Message passing mechanisms.

Vector Processing principle. Multivector multiprocessors. .Compound Vector processing. Principles of multithreading. Fine grain multicomputers. Scalable and multithread architectures. Dataflow and hybrid architectures.

Parallel programming models. Parallel languages and compilers. Parallel programming environments. Synchronization and multiprocessing modes. Message passing program development. Mapping programs onto multicomputers. Multiprocessor UNIX design goals. MACH/OS kernel architecture. OSF/1 architecture and applications.

Text Books:

1. *K. Hwang, Advanced Computer Architecture , TMH, 2001.*
2. *W. Stallings, Computer Organization and Architecture, McMillan, 1990 .*

Reference Book:

1. *M.J. Quinn, Designing Efficient Algorithms for Parallel Computer, McGraw Hill, 1994.*

EC670 Advanced Digital Design (3 – 0 - 3) 3

Different types of graphs. Combinational optimization- Graph optimization problems and algorithms. Boolean functions, statisfiability and cover. Abstract models, state diagrams. Data flow and sequencing graphs , compilation and behavioural optimization.

Architectural synthesis - Circuit specifications for architectural synthesis . Temporal domain , spatial domain , hierarchical models. Synchronization problems . Area and performance estimation. Strategies for architectural optimization, Data path synthesis of pipelined circuits.

Scheduling algorithms-Scheduling with and without constraints. Scheduling algorithms for extended sequencing models. Scheduling pipelined circuits.

Resource sharing and binding. Sharing and binding for resource dominated circuits and general circuits. Concurrent binding and scheduling. Resource sharing and binding for non-scheduled sequencing graphs.

Sequential logic optimization-sequential circuit optimization using state based models and network models. Implicit finite state machine. Traversal methods. Testability considerations for synchronous circuits.

Text Book:

1. *G.De Micheli, Synthesis and optimization of Digital circuits, McGraw Hill,1994 .*

EC672 Physical Design Automation (3 – 0 - 0) 3

VLSI design automation tools- algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools.

Layout compaction, placement and routing. Design rules, symbolic layout. Applications of compaction. Formulation methods. Algorithms for constrained graph compaction. Circuit representation. Wire length estimation. Placement algorithms. Partitioning algorithms.

Floor planning and routing- floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.

Simulation and logic synthesis- gate level and switch level modeling and simulation. Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.

High-level synthesis- hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment and scheduling. Scheduling algorithms. Aspects of assignment. High level transformations.

Text Books:

1. *S.H. Gerez, A lgorithms for VLSI Design Automation, John Wiley ,1998.*
2. *N.A.Sherwani , Algorithms for VLSI Physical Design Automation, (3/e), Kluwer,1999.*

Reference Books:

1. *S.M. Sait , H. Youssef, VLSI Physical Design Automation, World scientific, 1999.*
2. *M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996.*

EC674 Mixed - Signal Circuit Design (3 – 0 - 0) 3

Concepts of Mixed-Signal Design and Performance Measures. Fundamentals of Data Converters. Nyquist Rate Converters and Over sampling Converters.

Design methodology for mixed signal IC design using gm/Id concept.

Design of Current mirrors. References. Comparators and Operational Amplifiers.

CMOS Digital Circuits Design: Design of MOSFET Switches and Switched-Capacitor Circuits, Layout Considerations.

Design of frequency and Q tunable continuous time filters.

Text Books:

1. *R. Jacob Baker, Harry W. Li, David E. Boyce, CMOS, Circuit Design, Layout, and Simulation, Wiley-IEEE Press, 1998*
2. *David A. Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 1997.*