GITAM UNIVERSITY

(Declared as Deemed to be University U/S 3 of UGC Act, 1956)

REGULATIONS & SYLLABUS
OF

M.Tech. (VLSI Design)

(w.e.f 2012 -13 admitted batch)

Gandhi Nagar Campus, Rushikonda
VISAKHAPATNAM – 530 045
Website: www.gitam.edu

SYLLABUS

M.Tech (VLSI Design)

Programme Code: EPRVD 200801

I Semester

Course Code	Name of the Course	Credits	Hours per Week	Continuous Evaluation	Semester End Examination	Total Marks
EPRVD101	Digital System Design	4	4L	40	60	100
EPRVD102	Digital IC Design	4	4L	40	60	100
EPRVD103	Analog IC Design	4	4L	40	60	100
EPRVD121-124	Elective – I	4	4L	40	60	100
EPRVD131-133	Elective - II	4	4L	40	60	100
EPRVD111	VLSI Circuit Design Laboratory	2	6P	100	-	100
EPRVD112	FPGA Design Laboratory	2	3P	100	-	100
	Total	24	25	400	300	700

Elective - I	
EPRVD121	Semiconductor Devices
EPRVD122	Digital Signal Processing
EPRVD123	Operation and Modeling of MOS Transistor
EPRVD124	Modeling and Design with HDLs

Elective - II	
EPRVD131	VLSI Technology
EPRVD132	DSP Processors and Architectures
EPRVD133	Computer Organization

II semester

Course Code	Name of the Course	Credits	Hours per Week	Continuous Evaluation	Semester End Examination	Total Marks
EPRVD201	VLSI CAD	4	4L	40	60	100
EPRVD202	Digital Systems Testing and Testability	4	4L	40	60	100
EPRVD221-224	Elective –III	4	4L	40	60	100
EPRVD231-235	Elective – IV	4	4L	40	60	100
EPRVD241-245	Elective – V	4	4L	40	60	100
EPRVD211	Technical Seminar	2	2L	100	--	100
EPRVD212	Advanced VLSI Design Laboratory	2	6P	100	-	100
EPRVD213	Comprehensive Viva Voce	2	--	--	100	100
	Total	26	25	400	400	800

Elective – III	
EPRVD221	RF IC Design
EPRVD222	Analog System Design
EPRVD223	VLSI Digital Signal Processing
EPRVD224	Digital Systems Engineering

Elective – IV	
EPRVD231	Advanced Digital IC Design
EPRVD232	Low Power VLSI Design
EPRVD233	Data Converters
EPRVD234	Statistical Digital Signal Processing
EPRVD235	Active Filter Design

Elective – V	
EPRVD241	Advanced Computer Architecture
EPRVD242	Computer Arithmetic
EPRVD243	Logic Synthesis and Verification
EPRVD244	VLSI Physical Design Automation
EPRVD245	Advanced Digital Signal Processing

M.Tech (VLSI Design)

III Semester

Course Code	Name of the Course	Credits	Continuous Evaluation	Semester End Examination	Total Marks
EPRVD311	Project Work	8	50	50	100
	Total	8	50	50	100

IV Semester

Course Code	Name of the Course	Credits	Continuous Evaluation	Semester End Examination	Total Marks
EPRVD411	Project work	16	50	50	100
	Total	16	50	50	100

Total Credits 74

M.Tech (VLSI Design) I Semester

Digital System Design

Course Code: **EPRVD101** Credits: **4** Hours: **4 per week**
Category: **Core**

UNIT I
Review of Logic Design Fundamentals: Combinational Logic / Boolean Algebra and Algebraic Simplification Karnaugh Maps / Designing with NAND and NOR Gates / Hazards in Combinational Circuits / Flip-Flops and Latches / Mealy Sequential Circuit Design / Design of a Moore Sequential Circuit / Equivalent States and Reduction of State Tables / Sequential Circuit Timing / Tristate Logic and Busses

UNIT II
Introduction to VHDL: Computer-Aided Design / Hardware Description Languages / VHDL Description of Combinational Circuits / VHDL Modules / Sequential Statements and VHDL Processes / Modeling Flip-Flops Using VHDL Processes / Processes Using Wait Statements / Two Types of VHDL Delays: Transport and Inertial Delays / Compilation, Simulation, and Synthesis of VHDL Code / VHDL Data Types and Operators / Simple Synthesis Examples / VHDL Models for Multiplexers / VHDL Libraries / Modeling Registers and Counters Using VHDL Processes / Behavioral and Structural VHDL / Variables, Signals, and Constants / Arrays / Loops in VHDL / Assert and Report Statements

UNIT III
Introduction to Programmable Logic Devices: Brief Overview of Programmable Logic Devices / Simple Programmable Logic Devices (SPLDs) / Complex Programmable Logic Devices (CPLDs) / Field-Programmable Gate Arrays (FPGAs) Design Examples: BCD to 7-Segment Display Decoder / A BCD Adder / 32-Bit Adders / Traffic Light Controller / State Graphs for Control Circuits / Scoreboard and Controller / Synchronization and Debouncing / A Shift-and-Add Multiplier / Array Multiplier / A Signed Integer/Fraction Multiplier / Keypad Scanner / Binary Dividers

UNIT IV
SM Charts and Microprogramming: State Machine Charts / Derivation of SM Charts / realization of SM Charts / Implementation of the Dice Game / Microprogramming / Linked State Machines

UNIT V
Designing with Field Programmable Gate Arrays: Implementing Functions in FPGAs / Implementing Functions Using Shannon's Decomposition / Carry Chains in FPGAs / Cascade Chains in FPGAs / Examples of Logic Blocks in Commercial FPGAs / Dedicated Memory in FPGAs / Dedicated Multipliers in FPGAs / Cost of Programmability / FPGAs and One-Hot State Assignment / FPGA Capacity: Maximum Gates Versus Usable Gates / Design Translation (Synthesis) / Mapping, Placement, and Routing

Text Books :

1. Charles Roth, Lizy Kurian John, Principles of Digital System Design using VHDL, Cengage Learning, 2009.

Reference Books:

1. John F. Wakerly, Digital Design Principles and Practices, Pearson Education, 2002..
2. Digital Systems Design using VHDL by Charles Roth, Cengage Learning, 1998.
3. Michael Ciletti, Advanced Digital Design using Verilog HDL, Prentice Hall Publications, 2006
4. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte) 1994.
5. S.Trimberger, Field Programmable Gate Array Technology, Kluwer Academic Publications ,1994.
6. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
7. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubications, 1992.
8. S.Brown, R.Francis, J.Rose, Z.Vransic, Fundamentals of Digital Logic with Verilog Design, Kluwer Pubishers, 1992.
9. FPGA Based system Design, Wayve Woldf, Pearson Education

M.Tech (VLSI Design) I Semester

Digital IC Design

Course Code: **EPRVD102** Credits: **4** Hours: **4 per week**
Category: **Core**

UNIT-I
Introduction: Historical Perspective, Issues in Digital Integrated Circuit Design, Quality Metrics of a Digital Design - Cost of an Integrated Circuit, Functionality and Robustness, Performance, Power and Energy Consumption – The Manufacturing Process - Introduction, Manufacturing CMOS Integrated Circuits, The Silicon Wafer, Photolithography, Some Recurring Process Steps Simplified CMOS Process Flow, Design Rules — The Contract between Designer and Process Engineer

UNIT-II
Devices: Introduction, The Diode, A First Glance at the Diode — The Depletion Region, Static Behavior, Dynamic, or Transient, Behavior, The Actual Diode—Secondary Effects, The SPICE Diode Model, The MOS(FET) Transistor, A First Glance at the Device, The MOS Transistor under Static Conditions, Dynamic Behavior, The Actual MOS Transistor—Some Secondary Effects, SPICE Models for the MOS Transistor – **Wire:** Introduction, A First Glance, Interconnect Parameters — Capacitance, Resistance, and Inductance, Capacitance, Resistance, Inductance

UNIT-III
The CMOS Inverter: Introduction, The Static CMOS Inverter — An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Switching Threshold, Noise Margins, Robustness Revisited, Performance of CMOS Inverter: The Dynamic Behavior, Computing the Capacitances, Propagation Delay: First-Order Analysis, Propagation Delay from a Design Perspective, Power, Energy, and Energy-Delay, Dynamic Power Consumption, Static Consumption, Perspective: Technology Scaling and its Impact on the Inverter Metrics

UNIT-IV
Designing Combinational Logic Gates in CMOS: Introduction, Static CMOS Design, Complementary CMOS, Ratioed Logic, Pass-Transistor Logic, Dynamic CMOS Design, Dynamic Logic: Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Perspectives, How to Choose a Logic Style, Designing Logic for Reduced Supply Voltages

UNIT-V
Designing Sequential Logic Circuits: Introduction, Timing Metrics for Sequential Circuits, Classification of Memory Elements, Static Latches and Registers, The Bistability Principle, Multiplexer-Based Latches Master-Slave Edge-Triggered Register, Low-Voltage Static Latches, Static SR Flip-Flops—Writing Data by Pure Force, Dynamic Latches and Registers, Dynamic Transmission-Gate Edge-triggered Registers C2MOS—A Clock-Skew Insensitive Approach, True Single-Phase Clocked Register (TSPCR), Pipelining: An approach to optimize sequential circuits, Latch- vs. Register-Based Pipelines, NORA-CMOS—A Logic Style for Pipelined Structures, Non-Bistable Sequential Circuits, The Schmitt Trigger, Monostable Sequential Circuits, Astable Circuits, Perspective: Choosing a Clocking Strategy

Text Books :

1. Jan M. Rabaey Anantha Chandrakasan, & Borivoje Nikolic, Digital Integrated Circuits – A design perspective, Second Edition, PHI, 2003

Reference Books:

1. S. M. Kang & Y. Leblebici, CMOS Digital Integrated Circuits, Third Edition, McGraw Hill, 2003.
2. Jackson & Hodges, Analysis and Design of Digital Integrated circuits. 3rd Ed. TMH Publication, 2005.
3. Ken Martin, Digital Integrated Circuit Design, Oxford Publications, 2001.
4. Sedra and Smith, Microelectronic Circuits 5/e, Oxford Publications, 2005.

M.Tech (VLSI Design) I Semester

Analog IC Design

Course Code: **EPRVD103** Credits:**4** Hours: **4 per week**
Category: **Core**

UNIT I

Basic MOS Device Physics: General Considerations, MOSFET as a Switch, MOSFET Structure, MOS Symbols, MOS I/V Characteristics, Threshold Voltage, Derivation of I/V Characteristics, Second-Order Effects, MOS Device Models, MOS Device Layout, MOS Device Capacitances, MOS Small-Signal Model, MOS SPICE models, NMOS versus PMOS Devices, Long-Channel versus Short-Channel Devices.

UNIT II

Single-Stage Amplifiers, Basic Concepts , Common-Source Stage, Common-Source Stage with Resistive Load ,CS Stage with Diode-Connected Load, CS Stage with Current-Source Load, CS Stage with Triode Load, CS Stage with Source Degeneration, Source Follower, Common-Gate Stage, Cascode Stage, Folded Cascode, Choice of Device Models.

UNIT III

Differential Amplifiers, Single-Ended and Differential Operation. Basic Differential Pair, Qualitative Analysis, Quantitative Analysis, Common-Mode Response, Differential Pair with MOS Loads, Gilbert Cell, **Passive and Active Current Mirrors,** Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors, Large-Signal Analysis, Small-Signal Analysis, Common-Mode Properties

UNIT IV

Frequency Response of Amplifiers, General Considerations, Miller Effect, Association of Poles with Nodes, Common-Source Stage, Source Followers, Common-Gate Stage, Cascode Stage, Differential Pair **Feedback** General Considerations, Properties of Feedback Circuits, Types of Amplifiers, Feedback Topologies, Voltage-Voltage Feedback, Current-Voltage Feedback, Voltage-Current Feedback, Current-Current Feedback, Effect of Loading, Two-Port Network Models, Loading in Voltage-Voltage Feedback, Loading in Current-Voltage Feedback, Loading in Voltage-Current Feedback, Loading in Current-Current Feedback, Summary of Loading Effects, Effect of Feedback on Noise

UNIT V

Operational Amplifiers, General Considerations , Performance Parameters, One-Stage Op Amps, Two-Stage Op Amps , Gain Boosting , Comparison , Common-Mode Feedback . Input Range Limitations, Slew Rate, Power Supply Rejection. **Stability and Frequency Compensation** General Considerations, Multipole Systems, Phase Margin, Frequency Compensation, Compensation of Two-Stage Op Amps, Slewing in Two-Stage Op Amps, Other Compensation Techniques.

Text Books:

1. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2001.

Reference Books:

1. P. R. Gray & R. G. Meyer, Analysis and Design of Analog Integrated Circuits, Fifth Edition, John Wiley, 2010.
2. R. Gregorian and Temes, Analog MOS Intgrated Circuits for Signal Processing, Wiley, 1986.
3. Ken Martin, Analog Integrated Circuit Design, Wiley Publications, 2002.
4. Sedra and Smith, Microelectronic Circuits 5/e, Oxford Publications, 2001
5. B.Razavi, Fundamentals of Microelectronics, Wiley Publications, 2008

M.Tech (VLSI Design) I Semester

Semiconductor Devices

Course Code: **EPRVD121** Credits: **4** Hours: **4 per week**
Category: **Elective - I**

UNIT I

Review of Electronics in Solids. Electronics in Semiconductors: Introduction, Bandstructure of semiconductors, Holes in semiconductors, bandstructures of some semiconductors, Mobile carriers, Doping, Carriers in doped semiconductors, **Carrier Dynamics in Semiconductors**: Introduction, Scattering in semiconductors, Velocity electric field relations in semiconductors, Very high field transport, carrier transport by diffusion, charge injection and quasi Fermi levels, carrier generation and recombination, Continuity equation.

UNIT II

Junctions in Semiconductors: Device demands, Unbiased p-n junction, p-n junction under bias, real diode, high voltage effects in diodes, modulation and switching ac response. Spice model**. Semiconductor Junctions with metal and insulators:** Metals as conductors, Schottky barrier diode, Ohmic contacts, Insulator-semiconductor junctions.

UNIT III

Bipolar Junction Transistors: Introduction, Bipolar transistor, static characteristics of bipolar transistors, bjt static performance parameters, secondary effects in real devices, a charge control analysis, bipolar transistor as an inverter, high frequency behavior of bjt. Spice model. Bipolar transistors: A Technology roadmap.

UNIT IV

Field Effect Transistors(MOSFET): Introduction, MOSFET, structure and fabrication, metal-oxide semiconductor capacitor, capacitance voltage characteristics of the mos structure, metal oxide semiconductor field effect transistor, important issues in real mosfets,

UNIT V

Field Effect Transistors (JFET, MESFET): Introduction, JFET, MESFET, Current voltage characteristics, effects in real devices, high frequency high speed issues. **Semiconductor Optoelectronics:** Introduction, Optical absorption in a semiconductor, photo current in a p-n diode, P-I-N photodetector, Light emission, semiconductor laser-basic principles.

Text Books:

1. Jasprit Singh, Semiconductor Devices, Basic Principles, Wiley Student Edition, 2001
2. Ben G. Streetman, Solid State Electronic Devices, Sixth Edition, Prentice Hall India, 2009.

Reference Books:

1. Yuan Taur, Tak.H.Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 1998
2. Donald Neamen, Semiconductors Physics and Devices, Tata Mc Graw Hill, 2003
3. Tyagi, Introduction to Semiconductor Materials and Devices, Wiley Publications, 2002.
4. Semiconductor Devices, Basic Principles Jasprit Singh, Wiley Publications, 2001
5. S.M. Sze (Ed), Physics of Semiconductor Devices, 2nd Edition, Wiley Publications, 1998
6. Analysis and Design of Analog Integrated Circuits 4/e, Paul R. Gray, Paul J. Hurst, Robert G Meyer, 2001, Wiley Publications
7. Physics of Semiconductor Devices 3/e S. M. Sze, Wiley Publications, 2007.

M.Tech (VLSI Design) I Semester

Digital Signal Processing

Course Code: **EPRVD122** Credits: **4** Hours: **4 per week**
Category: **Elective - I**

UNIT-I

Discrete-Time Signals And Systems - Discrete-Time Signals, Discrete-Time Systems, Analysis of Discrete-Time Linear Time-Invariant systems, Discrete-Time Systems Described by Difference Equations, Implementation of Discrete-Time Systems

UNIT-II

Frequency Analysis Of Signals And Systems: The z-Transform, Properties of the z-Transform, Analysis of Linear Time Invariant Systems in the z-Domain, Frequency Analysis of Continuous-Time Signals, Frequency Analysis of Discrete-Time Signals, Frequency-Domain Characteristics of Linear Time-Invariant Systems, Frequency Response of LTI Systems

UNIT-III

The Discrete Fourier Transform: Its Properties And Applications - Frequency Domain Sampling: The Discrete Fourier Transform, Properties of the DFT, Linear Filtering Methods Based on the DFT, Frequency Analysis of Signals Using the DFT, The Discrete Cosine Transform, Efficient Computation of the DFT: FFT Algorithms Applications of FFT Algorithms

UNIT-IV

Implementation Of Discrete-Time Systems: Structures for the Realization of Discrete-Time Systems, Structures for FIR Systems, Structures for IIR Systems, Representation of Numbers, Quantization of Filter Coefficients, Round-Off Effects in Digital Filters, Quantization Effects in the Computation of the DFT

UNIT-V

Design Of Digital Filers: General Considerations, Design of FIR Filters, Design of IIR Filters From Analog Filters Frequency Transformations

Text Books:

1. Digital Signal Processing : Principles, Algorithms and Applications - Proakis, J.Gard and D.G.Manolakis, Fourth Edn.,,PHI, 1996.

Reference Books:

1. Discrete Time Signal Processing – A.V. Oppenheim and R.W. Schaffer, PHI, 1989.
2. Fundamentals of Digital Signal Processing – Robert J. Schilling & Sandra L. Harris, Thomson, 2005
3. Digital Signal Processing – S. Salivahanan et al., TMH, 2000.
4. Digital Signal Processing – Thomas J. Cavicchi, WSE, John Wiley, 2004.
5. Digital Signal Processing by A.V.Opperheim & R.W.Schafer, PHI Publications

M.Tech (VLSI Design) Ist Semester

Operation and Modeling of MOS Transistor

Course Code: **EPRVD123** Credits: **4** Hours: **4 per week**
Category: **Elective-I**

UNIT-I

Semiconductors, Junctions, and Mosfet Overview: Introduction, Semiconductors, Conduction Contact Potentials, Thepn Junction, Overview of the MOS Transistors, Fabrication Processes and Device Features. **The Two Terminal MOS Structure:** Introduction, The Flat-Band Voltage, Potential Balance and Charge Balance, Effect of Gate - Body Voltage on Surface Condition, Accumulation and Depletion, Inversion, Small - Signal Capacitance, Summary of Properties of the Regions of Inversion

UNIT-II

The Three Terminal MOS Structure: Introduction, Contacting the Inversion Layer, The Body Effect, Regions of Inversion, "CB Control" Point of View. **The Four - Terminal MOS Transistor** Introduction, Transistor Regions of Operation, Complete All - Region Model, Simplified All - Region Models, Models Based on Quasi - Fermi Potentials, Regions of Inversion in Terms of Terminal Voltages, Strong Inversion, Complete Strong -Inversion Model, Weak Inversion Special Conditions in Weak Inversion , Moderate Inversion and Single - Piece Models, Source - Referenced vs. Body - Referenced Modeling, Effective Mobility, Effect of Extrinsic Source and Drain Series Resistances, Temperature Effects, Breakdown, The p-Channel MOS Transistor

UNIT-III

Small Dimension Effects: Introduction, Carrier Velocity Saturation, Channel Length Modulation, Charge Sharing, Drain - Induced Barrier Lowering, Punchthrough, Combining Several Small - Dimension Effects Into One Model - A Strong Inversion Example, Hot Carrier Effects; Impact Ionization, Velocity Overshoot and Ballistic Operation, Polysilicon Depletion, Quantum Mechanical Effects, DC Gate Current, Junction Leakage; Band - to - Band Tunneling; GIDL, Leakage Currents – Examples, The Quest for Ever - Smaller Devices.

UNIT-IV

The MOS Transistor In Dynamic Operation - Large Signal Modeling: Introduction, Quasi - Static Operation, Terminal Currents in Quasi - Static Operation, Evaluation of Intrinsic Chargers in Quasi - Static Operation, Transit Time Under DC Conditions, Limitations of the Quasi - Static Model, Non - Quasi - Static Modeling, Extrinsic Parasitics,

UNIT-V

Small - Signal Modeling for Low and Medium Frequencies: Introduction, A Low - Frequency Small - Signal Model for the Intrinsic Part, A Medium - Frequency Small - Signal Model for the Intrinsic Part, Including the Extrinsic Part, Noise, All - Region Models. **High Frequency Small - Signals Models:** Introduction, A Complete Quasi - Static Model, y- Parameter Models, Non - Quasi - Static Models, High - Frequency Noise, Consideration In MOSFet Modeling for RF Applications

Text Books :

1. Yannis Tsividis and Colin McAndrew , Operation and Modeling of the MOS Transistor, Third Edition, Oxford University Press, 2011

Reference Books:

1. Taur and Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press.
2. Donald Neamen, Semiconductors Physics and Devices, Tata Mc Graw Hill, 2003
3. Tyagi, Introduction to Semiconductor Materials and Devices, Wiley Publications, 2002.
4. Semiconductor Devices, Basic Principles Jasprit Singh, Wiley Publications, 2001
5. S.M. Sze (Ed), Physics of Semiconductor Devices, 2nd Edition, Wiley Publications, 1998
6. Analysis and Design of Analog Integrated Circuits 4/e, Paul R. Gray, Paul J. Hurst, Robert G Meyer, 2001, Wiley Publications

Physics of Semiconductor Devices 3/e S. M. Sze, Wiley Publications, 2007.

M.Tech (VLSI Design) I Semester

Modeling and Design with HDLs

Course Code: **EPRVD124** Credits: **4** Hours: **4 per week**
Category: **Elective - I**

Unit-I
Basic Concepts:Lexical Conventions. Data Types. System Tasks and Compiler Directives.**Modules and Ports:** Modules. Ports. Hierarchical Names. **Gate-Level Modeling:** Gate Types. Gate Delays.

Unit-II
Dataflow Modeling: Continuous Assignments. Delays. Expressions, Operators, and Operands. Operator Types. Examples.

Unit-II
Behavioral Modeling: Structured Procedures. Procedural Assignments. Timing Controls. Conditional Statements. Multiway Branching. Loops. Sequential and Parallel Blocks. Generate Blocks. Examples.

Unit-III
Tasks and Functions: Difference between Tasks and Functions. Tasks. Functions. **Procedural Continuous Assignments.** Overriding Parameters. Conditional Compilation and Execution. Time Scales. Useful System Tasks. **Timing and Delays:** Types of Delay Models. Path Delay Modeling. Timing Checks. Delay Back-Annotation.

Unit- IV
Switch Level Modeling: Switching-Modeling Elements. Examples. **User-Defined Primitives**: UDP basics. Combinational UDPs. Sequential UDPs. UDP Table Shorthand Symbols. Guidelines for UDP Design.

Unit-V
Writing testbenches: Basic testbenches, Testbench structure, Constrained random stimulus generation, Object-oriented programming, Assertion-based verification. **SystemVerilog simulation**: Event-driven simulation, SystemVerilog simulation Races, Delay models, Simulator tools**. SystemVerilog synthesis:** RTL synthesis: Non-synthesizable SystemVerilog, Constraints, Attributes, Area and structural constraints Synthesis for FPGAs, Behavioral synthesis, Verifying synthesis results

Text Books

1. Samir Palnitkar, Verilog HDL 2/e, Pearson Education,
2. Mark Zowilski, Digital System Design with SystemVerilog, Pearson Education, 2010

Reference Books

1. J.Bhasker, Verilog HDL Primer, Pearson Education
2. J.Bhasker, Verilog Synthesis Primer, B.S.Publications.
3. M.Ciletti, Advanced Digital Design with Verilog HDL,Second Edition Pearson Education.

M.Tech (VLSI Design) I Semester

VLSI Technology

Course Code: **EPRVD131** Credits: **4** **H**ours: **4 per week**
Category: **Elective - II**

UNIT I
Introduction : Semiconductor materials, Semiconductor Devices, Semiconductor process technology, Basic fabrication steps. Crystal Growth : Silicon Crystal Growth from melt, Silicon Float-Zone Process, GaAs Crystal Growth Techniques, Material Characterization.

UNIT II
Silicon Oxidation : Thermal oxidation, Impurity Redistribution during oxidation, masking properties of silicon dioxide, oxide quality, oxide thickness characterization. Photolithography: Optical lithography, Next-Generation lithographic.

UNIT III
Etching : Wet chemical etching, Dry etching. Diffusion : Basic Diffusion Process, Extrinsic Diffusion, Lateral Diffusion.

UNIT IV
Ion Implantation : Range of Implanted ions, Implant Damage and annealing, Implantation-related Process. Film Deposition : Epitaxial growth techniques, Structures and defects in epitaxial layers, Dielectric deposition, Polysilicon deposition, Metallization.

UNIT V
Process Integration : Passive Components, Bipolar Technology, MOSFET technology, MESFET technology, MEMS technology. IC Manufacturing : Electrical testing, Packaging.

Text Books:

1. Gary S. May, Simon M. Sze, Fundamentals of Semiconductor Fabrication, John Wiley Inc., 2004.

Reference Books:

1. C.Y. Chang and S.M.Sze (Ed), ULSI Technology, McGraw Hill Companies Inc, 1996.
2. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983.
3. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988
4. The Science and Engineering of Microelectronic Fabrication, Stephen Cambell, Oxford University Press, 2001.

M.Tech (VLSI Design) I Semester

DSP Processors and Architectures

Course Code: **EPRVD132** Credits: **4** Hours: **4 per week**
Category: **Elective - II**

UNIT-I

Review of Digital signal processing. ,the sampling process,Discrte time sequences, discrete fourier transform and FFT, Linear time –invariant systems, digital filters, decimation and Interpolation,analysys and design tool for DSP systems. **Computational accuracy IN DSP Implementations:** number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D conversion errors, DSP computational errors.D/A conversion errors, compensating filter.

UNIT-II

Architectures for Programmable DSP Devices : basic architectural features,DSP computational building blocks. Bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing. **Programmable Digital Signal Processors:** Introduction. Commercial Digital Signal Processing Devices. The Architecture of TMS320C54xx Digital Signal Processors. Addressing Modes of the TMS320C54xx Processors. Memory Spaces of TMS320C54xx Processors. Program Control. TMS320C54xx Instructions and Programming. On-Chip Peripherals. Interrupts. Pipeline Operation of the TMS320C54xx Processors

UNIT-III

Implementation of Basic DSP Algorithms: Introduction. The Q-notation. FIR Filters. IIR Filters. Interpolation Filters. Decimation Filters. PID Controller. Adaptive Filters. 2-D Signal Processing. **Implemenation of FFT Algortihms:** Introduction. An FFT Algorithm for DFT Computation. A Butterfly Computation. Overflow and Scaling. Bit-Reversed Index Generation. An 8-point FFT Implementation of TMS320C54xx. Computation of Signal Spectrum

UNIT-IV

Interfacing Memory and Parallel IO Peripherals to Programmable DSP Devices: Introduction. Memory Space Organization of the TMS320C54xx Devices. Memory and I/O Signals of the TMS320C54xx Devices. Memory Interface. Parallel I/O. Programmed I/O. Interrupts and I/O. Direct Memory Access (DMA).

UNIT-V

Interfacing Serial Converters to a Programmable DSP Device: Introduction. Synchronous Serial Interface between the DSP and an AIC. A Multi-channel Buffered Serial Port (McBSP). The McBSP Programming. A CODEC Interface Circuit. CODEC Programming. A CODEC-DSP Interface Example. **Applications:** Introduction. A DSP System. DSP Based Biotelemetry System. A Speech Processing System. An Image Processing System. A Position Control System for a Hard Disk Drive. DSP Based Power Meter

Text Books:

1. Digital Signal Processing- Avtar Singh and S. Srinivasan, Thompson Publications, 2004.

Reference Books:

1. Digital signal processors, Archtecture, programming and applications- B. venkata ramani and M. Bhaskar, TMH, 2004.
2. Sen. M. Kuo, Real-Time Digital Signal Processing: Implementations and Applications 2/e, Wiley Publications, 2006
3. Rulph Chassaing, Digital Signal Processing with C6713 and C6416 DSK, 2/e Wiley Publications, 2005
4. DSP processor fundamentals,Archtecture & Features-Lapsley et al. S. Chand & Co.2000

M.Tech (VLSI Design) I Semester

Computer Organization

Course Code: **EPRVD133** Credits: **4** Hours: **4 per week**
Category: **Elective - II**

UNIT-I
Instruction Set Architecture: Memory Locations and Addresses, Memory Operations, Instructions and Instruction Sequencing, Addressing Modes, Assembly Language, Stacks, Subroutines, Additional Instructions, Dealing with 32-Bit Immediate Values, CISC Instruction Sets, RISC and CISC Styles, Example Programs, Encoding of Machine Instructions

UNIT-II
Basic Input/Output: Accessing I/O Devices, Interrupts**. Software:** The Assembly Process, Loading and Executing Object Programs, Linker, Libraries, Compiler, Debugger, High Level Language for IO Tasks, Interaction between Assembly and C Language, The Operating System

Unit-III
Basic Processing Unit: Some Fundamental Concepts, Instruction Execution, Hardware Components, Instruction Fetch and Execution Steps, Control Signals, Hardwired Control, CISC-Style Processors. **Pipelining:** Basic Concept—The Ideal Case, Pipeline Organization, Pipelining Issues, Data Dependencies, Memory Delays, Branch Delays, Resource Limitations, Performance Evaluation, Superscalar Operation, Pipelining in CISC Processors

Unit-IV
Input/Output Organization: Bus Structure, Bus Operation, Arbitration, Interface Circuits, Interconnection Standards. **The Memory System:** Basic Concepts, Semiconductor RAM Memories, Read-only Memories, Direct Memory Access, Memory Hierarchy, Cache Memories, Performance Considerations, Virtual Memory, Memory Management Requirements, Secondary Storage

Unit-V
Arithmetic: Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Unsigned Numbers, Multiplication of Signed Numbers, Fast Multiplication. Integer Division, Floating-Point Numbers and Operations**. Parallel Processing and Performance**: Hardware Multithreading, Vector (SIMD) Processing, Shared-Memory Multiprocessors, Cache Coherence, Message-Passing Multicomputers, Parallel Programming for Multiprocessors, Performance Modeling

Text Books

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Naraig Manjikian, Computer Organization and Embedded Systems Sixth Edition, Mc Graw Hill Publications, 2010

Reference Books

1. Patterson, Hennessy, Computer Organization and Design, Fourth Edition, Elsevier Publications
2. Computer Architecture and Parallel Processing- Kaui Hwang and A. Briggs International Edition Mcgraw hill
3. Advanced Computer Architecture, Dezso Sima,terence Fountain ,peter Kacsuk Pearson Education

M.Tech (VLSI Design) I Semester

VLSI Circuit Design Laboratory

Course Code: **EPRVD111** Credits: **2** Hours : **6 per week**

This laboratory course shall be carried out in two 3-Hour sessions per week. Experiments shall be carried out using Tanner/Mentor Graphics/Cadence/Xilinx Tools

Session – I: Digital IC Design Laboratory

1. Introduction to SPICE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis)
2. Modeling of Diodes, MOS transistors, Bipolar Transistors etc using SPICE.
3. An Overview of Tanner EDA Tool/MicroWind/Electric/ Magic/LTSpice
4. I-V Curves of NMOS and PMOS Transistors
5. DC Characteristics of CMOS Inverters (VTC, Noise Margin)
6. Dynamic Characteristics of CMOS Inverters (Propagation Delay, Power Dissipation)
7. Schematic Entry/Simulation/ Layout of CMOS Combinational Circuits
8. Schematic Entry/Simulation/ Layout of CMOS Sequential Circuits
9. High Speed and Low Power Design of CMOS Circuits

Session-II: Analog IC Design Laboratory

Experiments shall be carried out using Tanner/Mentor Graphics/Cadence Tools

1. Study of MOS Characteristics and Characterization
2. Design and Simulation of Single Stage Amplifiers (Common Source, Source Follower, Common Gate Amplifier)
3. Design and Simulation of Single Stage Amplifiers (Cascode Amplifier, Folded Cascode Amplifier)
4. Design and Simulation of a Differential Amplifier (with Resistive Load, Current Source Biasing)
5. Design and Simulation of Basic Current Mirror, Cascode Current Mirror
6. Analysis of Frequency response of various amplifiers (Common Source, Source Follower, Cascode, Differential Amplifier
7. Design/Simulation/Layout of Telescopic Operational Amplifier/ Folded Cascode Operational Amplifier

M.Tech (VLSI Design) I Semester

FPGA Design Laboratory

Course Code: **EPRVD112** Credits: **2** Hours : **3 per week**

Modeling and Functional Simulation of the following digital circuits (with Xilinx/ ModelSim tools) using VHDL/Verilog Hardware Description Languages

1. Part – I Combinational Logic: Basic Gates, Multiplexer, Comparator, Adder/ Substractor, Multipliers, Decoders, Address decoders, parity generator, ALU

2. Part – II Sequential Logic: D-Latch, D-Flip Flop, JK-Flip Flop, Registers, Ripple Counters, Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial), Cyclic Encoder / Decoder.

3. Part – III Memories and State Machines: Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Arithmetic Multipliers using FSMs

4. Part-IV: FPGA System Design: Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation of UART/Mini Processors on FPGA/CPLD

M.Tech (VLSI Design) II Semester

VLSI CAD

Course Code: **EPRVD201** Credits: **4** Hours: **4 per week**
Category: **Core**

Unit - I

Algorithmic Graph Theory and Computational Complexity – Terminology, Data Structures for the Representation of Graphs, Computational Complexity, Examples of Graph Algorithms, Depth-first Search, Breadth-first Search, Dijkstra's Shortest-path Algorithm, Prim's Algorithm for Minimum Spanning Trees - **Tractable and Intractable Problems**, Combinatorial Optimization Problems, Decision Problems, Complexity Classes, NP-completeness and NP-hardness

Unit - II

Simulation - General Remarks on VLSI Simulation, Gate-level Modeling and Simulation, Signal Modeling, Gate Modeling, Delay Modeling, Connectivity Modeling, Compiler-driven Simulation Event-driven Simulation, Switch-level Modeling and Simulation, Connectivity and Signal Modeling, Simulation Mechanisms,

Unit - III

Logic Synthesis and Verification , Introduction to Combinational Logic Synthesis, Basic Issues and Terminology, A Practical Example, Binary-decision Diagrams, ROBDD Principles, ROBDD Implementation and Construction, ROBDD Manipulation, Variable Ordering, Applications to Verification, Applications to Combinatorial Optimization, Two-level Logic Synthesis, Problem Definition and Analysis, A Heuristic Based on ROBDDs, **High-level Synthesis**, Hardware Models for High-level Synthesis, Hardware for Computations, Data Storage, and Interconnection, Data, Control, and Clocks, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some Aspects of the Assignment Problem, High-level Transformations

Unit - IV

Layout Compaction, Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint-graph Compaction, A Longest-path Algorithm for DAGs, The Longest Path in Graphs with Cycles, The Liao- Wong Algorithm, The Bellman-Ford Algorithm, Discussion: Shortest Paths, Longest Paths and Time Complexity, Other Issues **Placement and Partitioning**, Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithms, Constructive Placement, Iterative Improvement, Partitioning, The Kernighan-Lin Partitioning Algorithm.

Unit - III

Floorplanning, Floorplanning Concepts, Terminology and Floorplan Representation, Optimization Problems in Floorplanning, Shape Functions and Floorplan Sizing **Routing**, Types of Local Routing Problems, Area Routing, Channel Routing, Channel Routing Models, The Vertical Constraint Graph, Horizontal Constraints and the Left-edge Algorithm Channel Routing Algorithms, Introduction to Global Routing, Standard-cell Layout, Building-block Layout and Channel Ordering, Algorithms for Global Routing, Problem Definition and Discussion, Efficient Rectilinear Steiner-tree Construction, Local Transformations for Global Routing

Text Books

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.

Reference Books

1. Majid Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996.
2. Naveed Sherwani, Algorithms for VLSI Physical Design Automation, 3rd ed., Kluwer Academic Pub., 1999
3. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993.
4. Modern VLSI Design: Systems on silicon – Wayne Wolf, Pearson Education Asia, 2nd Edition, 1998

M.Tech (VLSI Design) II Semester

Digital Systems Testing and Testability

Course Code: **EPRVD202** **Credits: 4** **Hours: 4 per week**
Category: **Core**

UNIT-I
Introduction: Introduction, Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing. **VLSI Testing Process and Test Equipment:** How to test chips. **Test Economics and Product Quality:** Test Economics, Yield. **Fault Modeling:** Defects, Errors and Functional Versus Structural Testing, Levels of Fault Models, Glossary of Fault Models, Single Stuck-at Fault. **LOGIC AND FAULT SIMULATION:** Simulation for Design Verification, Simulation for Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-Value Simulation, Algorithms for Fault Simulation,Statistical Methods for Fault Simulation

UNIT-II
Combinational Circuit Test Generation: Algorithms and Representations, Redundancy Identification (RID), Testing as a Global Problem, Definitions, Significant Combinational ATPG Algorithms

UNIT-III
Sequential Circuit Test Generation: ATPG for Single-Clock Synchronous Circuits, Time-Frame Expansion Method, Simulation-Based Sequential Circuit ATPG.

UNIT-IV
Memory Test: Memory Density and Defect Trends, Faults, Memory Test Levels, March Test Notation, Fault Modeling, Memory Testing **Digital DFT and Scan Design:** Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-V
Built-In Self Test: The Economic Case for BIST, Random Logic BIST, Memory BIST, Delay Fault BIST. **Boundary Scan Standard**: Motivation, System Configuration with Boundary Scan, Boundary Scan Description Language

Text Books

1. M. L. Bushnel and V. D. Agarwal, Essentials of Testing for Digital, Memory and Mixed – Signal VLSI Circuits, Boston: Kluwer Academic Publishers, 2000

Reference Books

1. M. Abramovici, M. A. Breuer, and A. D. Friedman, Digital Systems Testing and Testable Design, Piscataway, New Jersey: IEEE Press, 1994. Revised printing.
2. Niraj Jha, Sandeep Gupta, Test of Digital Systems, Cambridge University Press, 2003.
3. Robert J. Feugate, Steven. M. McIntyre, Introduction to VLSI Testing, Prentice Hall Publications, 1988
4. Ed. Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, VLSI Test Principles and Architectures, Elsevier Publications.
5. Alexander Miczo, Digital Logic Testing and Simulation, Second Edition, John Wiley and Sons, 2003.

M.Tech (VLSI Design) II Semester

RF IC Design

Course Code: **EPRVD221** Credits: **4** Hours: **4 per week**
Category: **Elective - III**

UNIT-I
Basic Concepts in RF Design: General Considerations, Effects of Nonlinearity, Noise, Sensitivity and Dynamic Range, Passive Impedance Transformation, Scattering Parameters, Analysis of Nonlinear Dynamic Systems, Volterra Series. **Communication Concepts**: General Considerations, Analog Modulation, Digital Modulation, Spectral Regrowth, Mobile RF Communications, Multiple Access Techniques, Wireless Standards, Differential Phase Shift Keying.

UNIT-II
Transceiver Architectures: General Considerations, Receiver Architectures, Transmitter Architectures, OOK Transceivers.

UNIT-III
Low-Noise Amplifiers: General Considerations, Problem of Input Matching, LNA Topologies, Gain Switching, Band Switching, High-IP2 LNAs, Nonlinearity Calculations.

UNIT-IV
Mixers: General Considerations, Passive Down conversion Mixers, Active Down conversion Mixers, Improved Mixer Topologies, Upconversion Mixers. **Passive Devices:** General Considerations, Inductors, Transformers, Transmission Lines, T-Line Structures, Varactors, Constant Capacitors.

UNIT-V
Oscillators: Performance Parameters, Basic Principles, Cross-Coupled Oscillator, Three-Point Oscillators, Voltage-Controlled Oscillators, LC VCOs with Wide Tuning Range, Phase Noise, Design Procedure, Low-Noise VCOs, LO Interface, Mathematical Model of VCOs, Quadrature Oscillators. **Phase-Locked Loops:** Basic Concepts, Type-I PLLs, Type-II PLLs, PFD/CP Nonidealities, Phase Noise in PLLs, Loop Bandwidth, Design Procedure. Overview of integer and fractional Frequency synthesizers, power amplifiers. Transceiver design example.

Text Books :

1. Behzad Razavi, RF Microelectronics, Second Edition, Pearson Education, 2011.

Reference Books:

1. Leung, Bosco, VLSI for Wirless Communication, Second Edition, Springer 2011.
2. Thomas Lee, Design of CMOS Radio Frequency Integrated Circuits, Cambridge University Press, 2002.

M.Tech (VLSI Design) II Semester

Analog System Design

Course Code: **EPRVD222** Credits: **4** Hours: **4 per week**
Category: **Elective - III**

Unit- I
Noise Analysis and Modeling: Statistical Characteristics of Noise, Noise Spectrum, Amplitude Distribution, Correlated and Uncorrelated Sources, Types of Noise, Thermal Noise, Flicker Noise, Representation of Noise in Circuits, Noise in Single-Stage Amplifiers, Common-Source Stage, Common-Gate Stage, Source Followers, Cascode Stage, Noise in Differential Pairs, Noise in Op-Amps, Noise Bandwidth.

Unit-II
Active and Passive Filter Design (Elementary Treatment): General Considerations, Filter Characteristics, Classification of Filters, Filter Transfer Function, Problem of Sensitivity, First-Order Filters, Second-Order Filters, Special Cases, RLC Realizations, Active Filters, Sallen and Key Filter, Integrator-Based Biquads, Biquads Using Simulated Inductors, Approximation of Filter Response, Butterworth Response, Chebyshev Response. **Comparators:** Characterization of a Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators, High-Speed Comparators

Unit-III
Introduction to Switched-Capacitor Circuits General Considerations, Sampling Switches, MOSFETS as Switches , Speed Considerations, Precision Considerations , Charge Injection Cancellation, Switched-Capacitor Amplifiers , Unity-Gain Sampler/Buffer, Noninverting Amplifier, Precision Multiply-by-Two Circuit, Switched-Capacitor Integrator, Switched-Capacitor Common-Mode Feedback

Unit –IV
Bandgap References: General Considerations, Supply-Independent Biasing, Temperature-Independent References, PTAT Current Generation, Constant-Gm Biasing, Speed and Noise Issues, Case Study. **Nonlinearity and Mismatch:** Nonlinearity, Mismatch

Unit-V
OSCILLATORS General Considerations , Ring Oscillators, LC Oscillators , Crossed-Coupled Oscillator Colpitts Oscillator, One-Port Oscillators, Voltage-Controlled Oscillators, Tuning in Ring Oscillators, Tuning in LC Oscillators, Mathematical Model of VCOs. **Phase-Locked Loops** Simple PLL , Phase Detector, Basic PLL Topology, Dynamics of Simple PLL, Charge-Pump PLLs, Problem of Lock Acquisition, Phase/Frequency Detector and Charge Pump, Basic Charge-Pump PLL, Nonideal Effects in PLLs , PFD/CP Nonidealities, Jitter in PLLs , Delay-Locked Loops, Applications, Frequency Multiplication and Synthesis, Skew Reduction, Jitter Reduction

Text Books

1. B. Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw Hill Publications, 2002
2. Allen Holberg, CMOS Analog Circuit Design, Oxford Publications, 2002
3. B.Razavi, Fundamentals of Microelectronics, Wiley Publications, 2008

Reference Books:

1. Baker, Li, Boyce, CMOS Mixed Circuit Design, Wiley Publications, 2002
2. Baker, Li, Boyce, CMOS Circuit Design Layout and Simulation, IEEE Press, 2000
3. David A Johns, Ken Martin, Analog Integrated Circuit Design, Wiley Publications, 2003

M.Tech (VLSI Design) II Semester

VLSI Digital Signal Processing

Course Code: **EPRVD223** Credits: **4** Hours: **4 per week**
Category: **Elective - III**

UNIT-I

Introduction to DSP Systems: Typical DSP algorithms, Representation of DSP algorithms. **Iteration Bound:** Introduction, Data flow graph representations, Loop Bound and Iteration bound, Algorithms for computing iteration bound, iteration bound of multirate dataflow graphs. **Pipelining and Parallel Processing:** Introduction, pipelining of fir digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT-II

Retiming: Introduction, Definition and Properties, Solving systems of inequalities, retiming techniques. **Unfolding:** Introduction, An algorithm for unfolding, properties of unfolding, critical path, unfolding and retiming, applications of unfolding.

UNIT-III

Folding: Introduction, folding transformation, register minimization techniques, register minimization in folded architectures, folding of multirate systems. **Systolic Architecture Design:** Introduction, Systolic array design methodology, FIR systolic arrays, selection of scheduling vector, matrix-matrix multiplication and 2-D systolic array design. Systolic arrays for state representations containing delays.

UNIT-IV

Fast Convolution: Introduction, Cook-Toom algorithm, Winograd algorithm, Iterated convolution, Cyclic convolution. **Algorithmic strength reduction in Filters and Transforms:** Introduction, Parallel FIR filters, Discrete Cosine Transform and IDCT. **Pipelined and Parallel Recursive Filters:** Introduction, Pipeline interleaving in digital filters, Pipelining in first order IIR fiters, Pipelining in higher order IIR filters, Parallel processing for IIR filters.

UNIT-V

Bit-Level Arithmetic Architectures: Introduction, Parallel Multipliers, Interleaved floorplan and bitplane based digital filters, Bit serial multipliers, bit serial filter design and implementation. **Numerical strength reduction:** Introduction, subexpression elimination, multiple constant multiplication, sub-expression sharing in digital filters. **Low Power Design:** Introduction, Theoretical background, scaling vs. power consumption, power analysis, power reduction techniques, power estimation approaches.

Text Books

1. Keshab Parhi, VLSI Digital Signal Processing, Wiley Student Edition, 1999.

Reference Books

1. Lan Wanhammer, DSP Integrated Circuits, Academic Press
2. George A. Constantinides, Peter Y.K. Cheung, Wayne Luk, Synthesis and Optimization of DSP Algorithms, Kluwer Academic Publishers.
3. Digital Signal Processing : Principles, Algorithms and Applications - Proakis, J.Gard and D.G.Manolakis, Fourth Edn.,,PHI, 1996

M.Tech (VLSI Design) II Semester

Digital Systems Engineering

Course Code: **EPRVD224** Credits: **4** Hours: **4 per week**
Category: **Elective - III**

UNIT-I
Introduction: Engineering view of a digital system, Technology Trends and Digital Systems Engineering, Packaging of Digital Systems: A typical digital system, On chip wiring, Integrated Circuit Packages, Printed Circuit Boards, Chassis and Cabinets, Backplanes and Mother Boards, Wire and Cable, Connectors, **Modeling and Analysis of Wires:** Geometry and Electrical Properties, Electrical Models of Wires, Simple Transmission Lines, Special Transmission Lines, Wire Cost Models

UNIT-II
Power Distribution: The Power Supply Network, Local Regulation, Logic Loads and On chip supply distribution, Power Supply Isolation, Bypass capacitors, Example power distribution system. **Noise in Digital Systems:** Noise Sources in a digital system, Power supply noise, Crosstalk, Intersymbol Interference, Managing Noise.

UNIT-III
Signalling Conventions: A Comparison of two transmission systems, considerations in a transmission system design, Signalling modes for transmission lines, signaling over lumped transmission media, Signal Encoding. **Advanced Signalling Conventions:** Signalling over RC Interconnect, Driving lossy LC lines, Simultaneous bidirectional signaling, AC and N of M Balanced Signalling, Examples.

UNIT-IV
Timing Conventions: A comparison of two timing conventions, considerations in timing design, timing fundamentals, Encoding timing: Signals and Events, Open Loop Synchronous timing, Closed loop timing, clock distribution. **Synchronization:** A Comparision of two synchronization strategies, synchronization fundamentals, synchronizer design, asynchronous design,

UNIT-V
Signalling Circuits: Terminations, transmitter circuits, receiver circuits, ESD Protection, An example signaling system. **Timing Circuits:** Delay line circuits, Voltage controller oscillators, Phase comparators, loop filters, Clock aligners.

Text Books :

1. William J. Dally and John Poulton, Digital Systems Engineering, Cambridge University Press,

Reference Books:

1. S. M. Kang & Y. Leblebici, CMOS Digital Integrated Circuits, Third Edition, McGraw Hill, 2003.
2. Jackson & Hodges, Analysis and Design of Digital Integrated circuits. 3rd Ed. TMH Publication, 2005.
3. Jan M Rabaey, Digital Integrated Circuits, Second Edition, Prentice Hall Publications.
4. Ken Martin, Digital Integrated Circuit Design, Oxford Publications, 2001.

M.Tech (VLSI Design) II Semester

Advanced Digital IC Design

Course Code: **EPRVD231** Credits: **4** Hours: **4 per week**
Category: **Elective - IV**

UNIT-I

Implementation Strategies for Digital ICs: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective—The Implementation Platform of the Future

UNIT-II

The Wire: Introduction, A First Glance, Interconnect Parameters — Capacitance, Resistance, and Inductance, Electrical Wire Models, SPICE Wire Models**. Coping with Interconnect:** Introduction, Capacitive Parasitics, Capacitance and Reliability—Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability—Ohmic Voltage Drop, Electromigration, Resistance and Performance—RC Delay

UNIT-III

Timing Issues in Digital Circuits: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Synchronizers and Arbiters, Synchronizers—Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL

UNIT-IV

Designing Arithmetic Building Blocks: Introduction, Datapaths in Digital Processor Architectures, The Adder, The Binary Adder: Definitions, The Full Adder: Circuit Design Considerations, The Binary Adder: Logic Design Considerations, The Multiplier, The Multiplier: Definitions, Partial-Product Generation, Partial Product Accumulation, Final Addition, Multiplier Summary, The Shifter, Barrel Shifter, Logarithmic Shifter

UNIT-V

Designing Memory and Array Structures: Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Nonvolatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References, Drivers/Buffers, Timing and Control

Text Books :

1. Jan M. Rabaey Anantha Chandrakasan, & Borivoje Nikolic, Digital Integrated Circuits – A design perspective, Second Edition, PHI, 2003

Reference Books:

1. S. M. Kang & Y. Leblebici, CMOS Digital Integrated Circuits, Third Edition, McGraw Hill, 2003.
2. Jackson & Hodges, Analysis and Design of Digital Integrated circuits. 3rd Ed. TMH Publication, 2005.
3. Ken Martin, Digital Integrated Circuit Design, Oxford Publications, 2001.
4. Sedra and Smith, Microelectronic Circuits 5/e, Oxford Publications, 2005.

M.Tech (VLSI Design) II Semester

Low Power VLSI Design

Course Code: **EPRVD232** Credits: **4** Hours: **4 per week**
Category: **Elective - IV**

Unit- I
Physics of Power Dissipation in CMOS FET Devices: Physics of power dissipation in MOSFET devices, power dissipation in cmos, low power vlsi design: Limits

Unit-II
Power Estimation: Modeling in signals, Signal Probability calculation, Probabilistic Techniques for signal activity estimation, Statistical Techniques, Estimation of Glitching power, Sensitivity Analysis. Power estimation using the input vector compaction, power dissipation in domino cmos, high level power estimation, Information theory based approaches, Estimation of maximum power.

Unit-III
Synthesis for Low Power: Behavioural Level Transforms, Logic Level Optimization for Low power, Circuit Level Optimization. **Design and Test of Low Voltage CMOS Circuits:** Circuit Design style, Leakage current in deep submicrometer transistors, Deep submicrometer device design issues, Key to minimizing SCE, Low voltage circuit design techniques, Designing deep submicrometer ics with elevated intrinsic leakage, multiple supply voltages.

Unit-IV
Low Power Static RAM Architectures: Organization of a static RAM, MOS Static RAM Memory cell, Banked organization of SRAMs, Reducing voltage swings on bit lines, Reducing power in write driver circuits, Reducing power in sense amplifier circuits, method for achieving low core voltages from a single supply.

Unit –V
Low Energy Computing using Energy Recovery Techniques: Energy dissipation in transistor channel using an RC model, Energy recovery circuit design, Designs with partially reversible logic, Supply clock generation.

Text Books

1. Kaushik Roy, Sharat C. Prasad, Low Power CMOS VLSI Circuit Design, John Wiley and Sons, 2000
2. Jan Rabaey, Low Power Design Essentials, Springer Publications, 2009

Reference Books:

1. Chandrakasan and R. Brodersen, Low-Power CMOS Design, IEEE Press, 1998 (Reprint Volume).
2. Chandrakasan, Bowhill, and Fox, Design of High-Performance Microprocessors, IEEE Press, 2001
3. Gary Yeap, Practical Low Power Digital VLSI Design , Springer Publications, 1997.
4. M. Keating et al., Low Power Methodology Manual, Springer, 2007.
5. S. Narendra and A. Chandrakasan, Leakage in Nanometer CMOS Technologies, Springer, 2006.
6. M. Pedram and J. Rabaey, Ed., Power Aware Design Methodologies, Kluwer Academic Publishers, 2002.
7. Piguet, Ed., Low-Power Circuit Design, CRC Press, 2005.
8. J. Rabaey and M. Pedram, Ed., Low Power Design Methodologies, Kluwer Academic Publishers, 1995.
9. J. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits - A Design Perspective, Prentice Hall, 2003.
10. S. Roundy, P. Wright and J.M. Rabaey, Energy Scavenging for Wireless Sensor Networks, Kluwer Academic Publishers, 2003.
11. Wang, Adaptive Techniques for Dynamic Power Optimization, Springer, 2008.

M.Tech (VLSI Design) II Semester

Data Converters

Course Code: **EPRVD233** Credits: **4** Hours: **4 per week**
Category: **Elective - IV**

UNIT-I
COMPARATORS: Comparator Specifications, Using an Opamp for a Comparator, Charge-Injection Errors, Latched Comparators, Examples of CMOS and BiCMOS Comparators. **SAMPLE-AND-HOLD AND TRANSLINEAR CIRCUITS:** Performance of Sample-and-Hold Circuits, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Bipolar and BiCMOS Sample and Holds, Translinear Gain Cell, Translinear Multiplier.

UNIT-II
CONTINUOUS-TIME FILTERS: Introduction to Continuous-Time Filters, Introduction to Gm-C Filters, Transconductors using Fixed Resistors, CMOS Transconductors Using Active Transistors, BiCMOS Transconductors, Active RC and MOSFET-C Filters, Tuning Circuitry, Introduction to Complex Filters. **DISCRETE-TIME SIGNALS:** Overview of Some Signal Spectra, Laplace Transforms of Discrete-Time Signals, Spectra of Discrete-Time Signals, z-Transform, Downsampling and Upsampling, Discrete-Time Filters, Sample-and-Hold Response.

UNIT-III
SWITCHED-CAPACITOR CIRCUITS: Basic Building Blocks, Basic Operation and Analysis, Noise in Switched-Capacitor Circuits, First-Order Filters, Biquad Filters, Charge Injection, Switched-Capacitor Gain Circuits, Correlated Double-Sampling Techniques, Other Switched-Capacitor Circuits. **DATA CONVERTER FUNDAMENTALS**: Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Deterministic Approach, Stochastic Approach, Signed Codes, Performance Limitations, Resolution. Offset and Gain Error, Accuracy and Linearity

UNIT-IV
NYQUIST-RATE D/A CONVERTERS: Decoder-Based Converters, Binary-Scaled Converters, Thermometer-Code Converters, Hybrid Converters. NYQUIST-RATE A/D CONVERTERS: Integrating Converters, Successive-Approximation Converters, Algorithmic (or Cyclic) A/D Converter, Pipelined A/D Converters, Flash Converters, Issues in Designing Flash A/D Converters, Two-Step A/D Converters, Interpolating A/D Converters, Folding A/D Converters, Time-Interleaved A/D Converters

UNIT-V
OVERSAMPLING CONVERTERS: Oversampling without Noise Shaping, Oversampling with Noise Shaping, System Architectures, Digital Decimation Filters, Higher-Order Modulators, Bandpass Oversampling Converters, Practical Considerations, Multi-Bit Oversampling Converters, Third-Order A/D Design Example

Text Books :

1. Tony Chan Carusone, Kenneth W. Martin, David A. Johns, Analog Integrated Circuit Design, 2nd Edition, Wiley Publications 2011.
2. Allen Holberg, CMOS Analog Circuit Design, Oxford Publications

Reference Books:

1. CMOS Data Converters for Communication - M. Gustavsson, J. Wikner, and N. Tan. Kluwer Academic Publishers, 2000.
2. Principles of Data Conversion System Design - Behzad Razavi.
3. Data Converters, Franco Maloberti, Springer Publications
4. CMOS Mixed Signal Design, Baker Li, Boyce, Wiley Publications

M.Tech (VLSI Design) II Semester

Statistical Digital Signal Processing

Course Code: **EPRVD234** Credits: **4** Hours: **4 per week**
Category: **Elective - IV**

UNIT-I
Background: Discrete-Time Signal Processing: Linear Algebra, Discrete-Time Random Processes: Introduction, Random Variables, Random Processes, Filtering Random Processes, Spectral Factorization, Special Types of Random Processes.

UNIT-II
Signal Modeling: Introduction, The Least Squares (Direct) Method, The Pade Approximation, Prony's Method, Finite Data Records, Stochastic Models. **The Levinson Recursion:** Introduction, The Levinson-Durbin Recursion, The Levinson Recursion.

UNIT-III
Lattice Filters: Introduction, FIR Lattice filter, IIR lattice filters. **Optimum Filters:** Introduction, The FIR Wiener Filter, The IIR Wiener Filter, Discrete Kalman Filter

UNIT-IV
Spectrum Estimation: Introduction, Nonparametric Methods, Minimum Variance Spectrum Estimation, The Maximum Entropy Method, Parametric Methods, Frequency Estimation, Principal Components Frequency Estimation

UNIT-V
Adaptive Filtering: Introduction, FIR Adaptive Filters, Adaptive Recursive Filters, Recursive Least Squares

Text Books

1. Monson Hayes, Statistical Digital Signal Processing, Wiley Student Edition,
2. Proakis, J.Gard & D.G.Manolakis, Digital Signal Processing : Principles, Algorithms and Applications , Fourth Edition, PHI, 2006.

Reference Books

1. Manolakis, Vijay Ingle, Stephen Kogon, Statistical and Adaptive Signal Processing, Artech Book House.
2. P.P. Vaidyanathan, Multirate systems and Filter banks, Prentice Hall, 1993
3. V. Oppenheim and R.W.Schafer, Discrete time Signal Processing, PHI 1994
4. S.J. Orfanidis, Optimum Signal Processing, McGraw Hill, 1989.
5. Insight into Wavelets, Ramachandran and Soman, Prentice Hall Publications, 2003
6. Wavelet Transforms: Introduction to Theory and Applications, Raghuveer M Rao, Ajit S, Bopardikar, Pearson Education 2000
7. John. G. Proakis, Algorithms for Statistical Signal Processing Pearson Education, 2002.

M.Tech (VLSI Design) II Semester

Active Filter Design

Course Code: **EPRVD235** Credits: **4** Hours: **4 per week**
Category: **Elective - IV**

UNIT-I

Operational Amplifiers: Operational Amplifier models, Opamp slew rate, Operational Amplifier with Resistive feedback, Analyzing opamp circuits. Examples. **First Order Filters:** Bilinear transfer function and its parts, realization with passive elements, bode plots, Active realizations, Effect of A(s), Cascade design.

UNIT-II

Second Order LowPass and BandPass Filters: Design parameters Q and w_0, Second order circuit, frequency response of lowpass and bandpass circuits, Integrators, Other Biquads. **Second Order Filters with Arbitrary transmission zeros:** Summing, Voltage feedforward, Cascade design revisited.

UNIT-III

Low Pass filters with Maximally flat magnitude: Ideal low pass filter, butterworth response, butterworth pole locations, low pass filter specifications, arbitrary transmission zeros. **Low Pass filters with Equal Ripple Magnitude Response:** The chebyshev polynomial, chebyshev magnitude response, local of chebyshev poles, comparision of maximally flat and equal ripple responses. Chebyshev filter design. **Frequency Transformation:** Low pass to highpass, low pass to bandpass, low pass to bandstop, lowpass to multiple passband transformation.

UNIT-IV

LC Ladder Filters: Some properties of lossless ladders, a synthesis strategy, General ladder design methods, frequency transformation, design of passive equalizers. **Ladder Simulations by Element Replacement:** The general impedance converter, optimal design of the gic, realizing simple ladders, gorski-popiel embedding technique, bruton's fdnr technique, creating negative components

UNIT-V

Transconductance-C filters: Transconductance Cells, Elementary transconductance building blocks, first order and second order filters, higher order filters. **Switched Capacitor Filters:** The MOS Switch, The switched capacitor, first order building blocks, second order sections, sampled data operation, switched capacitor first order and second order sections, bilinear transformation, design of switched capacitor cascade filters.

Text Books :

1. Rolf Schaumann, Van Valkenburg, Design of Analog Filters, Oxford University Press, 2001

Reference Books:

1. Integrated Continuous Time Filters, Yannis Tsividis and Johannes Voorman, IEEE Press.
2. Design of Analog Filters: Passive, Active RC and Switched Capacitor, Rolf Schaumann, M.S. Ghausi, Kenneth R. Laker.

M.Tech (VLSI Design) II Semester

Advanced Computer Architecture

Course Code: **EPRVD241** Credits: **4** Hours: **4 per week**
Category: **Elective - V**

UNIT-I

Fundamentals of Computer Design : technology trends, cost Measuring and reporting, performance quantitative principles of computer design, **Instruction set principles and examples**, classifying instruction set, memory addressing ,type and size of operands, addressing modes for signal processing, Operations in the instruction set ,instruction for control ,encoding an instruction set.

UNIT-II

Pipelining: Introduction, The Major Hurdle of Pipelining—Pipeline Hazards, How Is Pipelining Implemented? What Makes Pipelining Hard to Implement?, Extending the MIPS Pipeline to Handle Multicycle Operations. **Instruction Level Parallelism**: Overcoming hazards, reducing branch costs, High performance instruction delivery, hardware based speculation ,Limitation of ILP,ILP software approach, compiler techniques, static branch Protection VLIW approach.

UNIT-III

Memory Hierarchy Design: Introduction, Review of the ABCs of Caches, Cache Performance, Reducing Cache Miss Penalty, Reducing Miss Rate, Reducing Cache Miss Penalty or Miss Rate via Parallelism, Reducing Hit Time, Main Memory and Organizations for Improving Performance, Memory Technology, Virtual Memory, Protection and Examples of Virtual Memory. Basics of Virtual Machines.

UNIT-IV

Multiprocessors and Thread-Level Parallelism: Introduction, Characteristics of Application Domains, Symmetric Shared-Memory Architectures, Performance of Symmetric Shared-Memory Multiprocessors, Distributed Shared-Memory Architectures, Performance of Distributed Shared-Memory Multiprocessors, Synchronization, Models of Memory Consistency: An Introduction, Multithreading: Exploiting Thread-Level Parallelism within a Processor

UNIT-V

Storage Systems: Introduction, Types of Storage Devices, Buses—Connecting I/O Devices to CPU/Memory, Reliability, Availability, and Dependability, RAID: Redundant Arrays of Inexpensive Disks, Errors and Failures in Real Systems, I/O Performance Measures, Designing an I/O System in Five Easy Pieces

Text Books

1. John L. Hennessy & David A Patterson, Computer Architecture a quantitative approach 3rd edition Morgan Kuffman,2002

Reference Books

1. Computer Architecture a quantitative approach 4th edition John L. Hennessy & David A Patterson Morgan Kuffman,2005
2. Computer Architecture and Parallel Processing- Kaui Hwang and A. Briggs International Edition Mc graw hill
3. Advanced Computer Architecture, Dezso Sima,terence Fountain ,peter Kacsuk Pearson Education.

M.Tech (VLSI Design) II Semester

Computer Arithmetic

Course Code: **EPRVD242** Credits: **4** Hours: **4 per week**
Category: **Elective - V**

UNIT-I

Number Representation: Numbers and Arithmetic: What is computer arithmetic?, Motivating Examples, Numbers and their encodings, Fixed-radix positional number systems, Number radix conversion, Classes of number representations **Representing Signed Numbers:** Signed-magnitude representation, Biased representations, Complement representations, Two's- and 1's-complement numbers, Direct and indirect signed arithmetic, Using signed positions or signed digits, **Redundant Number Systems**, Coping with the carry problem, Redundancy in computer arithmetic, Digit sets and digit-set conversions, Generalized signed-digit numbers, Carry-free addition algorithms, Conversions and support functions. Introduction to Residue Number systems.

UNIT-II

Addition/Subtraction: Basic Addition and Counting: Bit-serial and ripple-carry adders, Conditions and exceptions, Analysis of carry propagation, Carry completion detection, Addition of a constant: counters, Manchester carry chains and adders, **Carry-Lookahead Adders**: Unrolling the carry recurrence, Carry-lookahead adder design, Ling adder and related designs, Carry determination as prefix computation, Alternative parallel prefix networks, VLSI implementation aspects **Variations in Fast Adders**: Simple carry-skip adders Multilevel carry-skip adders, Carry-select adders, Conditional-sum adder, Hybrid designs and optimizations, Modular two-operand adders

UNIT-III

Multiplication: Basic Multiplication Schemes, Shift/add multiplication algorithms, Programmed multiplication, Basic hardware multipliers, Multiplication of signed numbers, Multiplication by constants, Preview of fast multipliers. **High-Radix Multipliers**: Radix-4 multiplication, Modified Booth's recoding, Using carry-save adders, Radix-8 and radix-16 multipliers, Multibeat multipliers, VLSI complexity issues, **Tree and Array Multipliers**: Full-tree multipliers, Alternative reduction trees, Tree multipliers for signed numbers, Partial-tree and truncated multipliers, Array multipliers, Pipelined tree and array multipliers.

UNIT-IV

Division: Basic Division Schemes: Shift/subtract division algorithms, Programmed division, Restoring hardware dividers, Nonrestoring and signed division, Division by constants, Radix-2 SRT division, **High-Radix Dividers:** Basics of high-radix division, Using carry-save adders, Radix-4 SRT division, General high-radix dividers, Quotient-digit selection, Using p-d plots in practice, **Variations in Dividers**, Division with prescaling , Overlapped quotient-digit selection, Combinational and array dividers, Modular dividers and reducers, The special case of reciprocation, Combined multiply/divide units.

UNIT-V

Real Arithmetic: Floating-Point Representations, Floating-point numbers, The ANSI/IEEE floating-point standard, Basic floating-point algorithms, Conversions and exceptions, Rounding schemes, Logarithmic number systems, **Floating-Point Operations**: Floating-point adders/subtractors, Pre- and postshifting, Rounding and exceptions, Floating-point multipliers and dividers, Fused-multiply-add units, Logarithmic arithmetic unit.

Text Books

1. B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs, 2nd edition, Oxford University Press, New York, 2010.

Reference Books

1. Israel Koren , Computer Arithmetic Algorithms, Second Edition, Prentice Hall Publications, 2002
2. Milos D. Ercegovac, Digital Arithmetic (The Morgan Kaufmann Series in Computer Architecture and Design) , 2004

M.Tech (VLSI Design) II Semester

Logic Synthesis and Verification

Course Code: **EPRVD243** Credits: **4** Hours: **4 per week**
Category: **Elective - V**

UNIT-I
Background and Hardware Modeling: Graphs, Combinatorial Optimization, Graph Optimization Problems and algorithms, Boolean Algebra and its applications. **Hardware Modeling:** Introduction, Hardware Modeling Languages, Abstract Models, Compilation and Behavioral Optimization.

UNIT-II
Two Level Combinational Logic Optimization: Introduction, Logic Optimization Techniques, Operations on Two level logic covers, algorithms for logic minimization, Symbolic minimization and encoding problems.

UNIT-III
Multilevel Combinational Logic Optimization: Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model, Synthesis of Testable Networks. Algorithms for delay evaluation and optimization. Rule based systems for logic optimization.

UNIT-IV
Sequential Logic Optimization: Introduction, Sequential Circuit Optimization using state based models, sequential circuit optimization using network models, Implicit finite state machine traversal methods. Testability considerations for synchronous circuits.

UNIT-V
Cell Library Binding: Introduction, Problem formulation and Analysis, Algorithms for Library binding, specific problems and algorithms for library binding, rule based library binding

Text Books

1. G. De Micheli, Synthesis and Optimization of Digital Circuits, McGraw-Hill, Inc., 1994.

Reference Books:

1. G.D. Hachtel and F. Somenzi, Logic Synthesis and Verification Algorithms, Kluwer Academic Publishers, 1996

M.Tech (VLSI Design) II Semester

VLSI Physical Design Automation

Course Code: **EPRVD244** Credits: **4** Hours: **4 per week**
Category: **Elective - V**

UNIT-I
Data Structures and Basic Algorithms: Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithms for Physical design.

UNIT-II
Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms. Performance Driven Partitioning

UNIT-III
Floorplanning and Pin Assignment: Floorplanning, Chip planning, Pin Assignment. **Global Routing:** Problem Formulation, Classification of Global Routing, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms Integer Programming Based Approach, Performance Driven Routing.

UNIT-IV
Detailed Routing: Problem Formulation, Classification of Routing Algorithms, Single-Layer Routing Algorithms, Two-Layer Channel Routing Algorithms, Three-Layer Channel Routing Algorithms, Multi-Layer Channel Routing Algorithms, Switchbox Routing Algorithms

UNIT-V
Over-the-Cell Routing and Via Minimization: Over-the-cell Routing, Via Minimization. **Clock and Power Routing:** Clock Routing, Power and Ground Routing. **Compaction:** Problem Formulation, Classification of Compaction Algorithms, One-Dimensional Compaction, Two-Dimensional Compaction

Text Books

1. Naveed Sherwani, Algorithms for VLSI Physical Design Automation, Springer Publications.

Reference Books

1. Sung Kyu Lim, Practical Problems for VLSI Physical Design Automation, Springer Publications
2. Majid Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996.
3. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993.
4. Modern VLSI Design: Systems on silicon – Wayne Wolf, Pearson Education Asia, 2nd Edition, 1998

M.Tech (VLSI Design) II Semester

Advanced Digital Signal Processing

Course Code: **EPRVD245** Credits: **4** Hours: **4 per week**
Category: **Elective - V**

UNIT-I

Multirate Digital Signal Processing – Introduction, Decimation by a Factor D, Interpolation by a Factor I, Sampling Rate Conversion by a Rational Factor I/D, Implementation of Sampling Rate Conversion, Multistage Implementation of Sampling Rate Conversion, Applications of Sampling Rate Conversion, Digital Filter Banks Two-Channel Quadrature Mirror Filter Bank.

UNIT-II

Linear Prediction And Optimum Linear Filters - Random Signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process, Forward and Backward Linear Prediction, Solution of the Normal Equations Wiener Filters for Filtering and Prediction.

UNIT-III

Adaptive Filters - Applications of Adaptive Filters, Adaptive Direct-Form FIR Filters-The LMS Algorithm, Adaptive Direct-Form FIR Filters-RLS Algorithms.

UNIT-IV

Power Spectrum Estimation - Estimation of Spectra from Finite-Duration Observations of Signals, Nonparametric Methods for Power Spectrum Estimation, Parametric Methods for Power Spectrum Estimation.

UNIT-V

Power Spectrum Estimation: Filter Bank Methods: Capon's method, Eigenanalysis Algorithms for Spectrum Estimation: Pisarenko Harmonic Decomposition Method, MUSIC algorithm, ESPIRIT algorithm, Eigen Decomposition method

Text Books

1. Digital Signal Processing : Principles, Algorithms and Applications - Proakis, J.Gard and D.G.Manolakis, Fourth Edition, PHI, 2006.

Reference Books

1. Monson Hayes, Statistical Digital Signal Processing, Wiley Student Edition, 2008
2. Manolakis, Vijay Ingle, Statistical and Adaptive Signal Processing by Artech Book House, 2009.
3. P.P. Vaidyanathan, Multirate systems and Filter banks, Prentice Hall, 1993
4. V. Oppenheim and R.W.Schafer, Discrete time Signal Processing, PHI 1994
5. S.J. Orfanidis, Optimum Signal Processing, McGraw Hill, 1989.
6. Wavelet Transforms: Introduction to Theory and Applications, Raghuveer M Rao, Ajit S, Bopardikar, Pearson Education 2000.
7. Insight into Wavelets, Ramachandran and Soman, Prentice Hall Publications, 2003
8. John. G. Proakis, Algorithms for Statistical Signal Processing Pearson Education, 2002.

M.Tech (VLSI Design) II Semester

Technical Seminar

Course Code: **EPRVD211** Credits: **2** Hours: **2 per week**

Student during the Technical Seminar should cover topics not covered in the curriculum mainly related to applications of VLSI Design
Viz.

Wireless Communications, Wireless Networks, Communication Networks, Telephone Networks, Computer Organization, Microprocessors, Microcontrollers, Embedded Systems, Digital Signal Processing, Digital Signal Compression, Multimedia, Computer Architecture, Device Modeling, VLSI Fabrication, Low Power VLSI Design, Design for Yield, Design for Manufacturability, Sub Nanometer Design issues, Logic Synthesis, Physical Design etc

M.Tech (VLSI Design) II Semester

Advanced VLSI Design Laboratory

Course Code: **EPRVD212** Credits: **2** Hours: **3 per week**

This Laboratory Course takes two 3-Hour Sessions per week.

Session-I: VLSI System Design

1. Design/Simulation of other analog building blocks
    a. Comparators
    b. Oscillators
    c. PLLs
    d. switched capacitor circuits
    e. Noise Analysis

2. Mini Projects involving
    a. Unpipelined MIPS Processor
    b. Pipelined MIPS Processor
    c. Out of Order Execution with Tomasulo's Algorithm
    d. Communication Controllers
    e. Arithmetic Circuits
    f. DSP Systems

Session-II: ASIC Design

Experiments shall be carried out using Mentor Graphics/Cadence Tools

1. Part-I: Backend Design
   Schematic Entry/ Simulation / Layout/ DRC/PEX/Post Layout Simulation of CMOS Inverter, NAND Gate, OR Gate, Flip Flops, Register Cell, Half Adder, Full Adder Circuits

2. Part-II: Semicustom Design
   HDL Design Entry/ Logic Simulation, RTL Logic Synthesis, Post Synthesis Timing Simulation, Place & Route, Design for Testability, Static Timing Analysis, Power Analysis of Medium Scale Combinational, Sequential Circuits

3. Part-III: High Speed/Low Power CMOS Design
   Designing combinational/sequential CMOS circuits for High Speed
   Designing combinational/sequential CMOS circuits for Low Power

M.Tech (VLSI Design) III Semester

Project Work

Course Code: **EPRVD311** Credits: **8**

M.Tech (VLSI Design) IV Semester

Project Work

Course Code: **EPRVD411** Credits: **16**