UNIVERSITY OF CALICUT

Abstract

Faculty of Engineering – Scheme & Syllabus of M.Tech Course in VLSI Design – approved – Implemented – with effect from the academic year 2011 onwards – Orders issued.

= =

General and Academic Branch – IV 'E' Section

No.GA.IV/E1/8226/2011(**1**) Dated Calicut University P.O. 08.05.2012.

= =

Read:- 1. U.O.No.GA.IV/E1/8226/2011 dated 25.01.2012.
2. Minutes of the meeting of Board of Studies in Engineering (P.G) held on 30.03.2012 (Item.No.1)
3. Orders of Vice-Chancellor in the file of even No. dated 17.04.2012.
4. Letter from the Dean, Faculty of Engineering dated 23.04.2012.
5. Orders of Vice-Chancellor in the file of even No. dated 03.05.2012.

O R D E R

As per paper read as (1) above, an expert committee was constituted with the following members for the preparation of the scheme & syllabus for the M.Tech course in VLSI Design.

a) Dr.Reena.P (Co-ordinator), Member, Board of Studies in Engineering (PG) Professor in Electronics and Communication Engineering,Dept.of.Information Technology, Govt.Engineering College,Sreekrishnapuram, Palakkad – 678 633.

b) Prof.Martin.K.M, Scientist/Engineer – E, DOEACC Centre, Calicut, P.O NIT Campus, Kozhikode – 673 601.

c) Prof.K.S.Lalmohan, Scientist/Engineer – D, DOEACC Centre, Calicut, P.O. NIT Campus,
Kozhikode – 673 601.

Vide paper read as 2nd above, the meeting of Board of Studies in Engineering (P.G) held on 30.03.2012, vide item.No. 1 unanimously resolved to approve the Scheme & Syllabus of the M.Tech course in VLSI Design prepared by the Committee.

Vide paper read as 3rd above, the Vice-Chancellor had ordered to seek the opinion of the Dean, Faculty of Engineering regarding the approval of the minutes of the meeting of the Board of Studies in Engineering (PG) held on 30.03.2012

The Dean, Faculty of Engineering vide paper read as 4th above, recommended for the approval of the minutes of the meeting of the Board of Studies in Engineering (PG) held on 30.03.2012.

Contd..2

Considering the urgency of the matter, the Vice-Chancellor has accorded sanction to implement the Scheme & Syllabus of the M.Tech Course in VLSI Design, subject to ratification by the Academic Council, vide paper read as 5th above.

Sanction has therefore been accorded for implementing the Scheme & Syllabus of the M.Tech course in VLSI Design with effect from 2011 admission onwards.

Orders are issued accordingly.

(*The Syllabus is available in the University website)*

Sd/-
DEPUTY REGISTRAR (GA.IV)
For Registrar.

To

The Principals of all affiliated Engineering Colleges offering M.Tech Course.

Copy to :- P.S to V.C/PA. to PVC/ P.A. to Registrar/ P.A to C.E/Enquiry/ Ex.Sn/EG Sn/DR,M.Tech/ M.Tech. Tabulation Section/Dean, Faculty of Engineering/ Chairman, BOS in Engg (PG)&(UG) **System Administrator (with a request to upload in the university website)**/ SF/FC

Forwarded/By Order

Sd/-
SECTION OFFICER

UNIVERSITY OF CALICUT

M.Tech DEGREE COURSE

IN

VLSI DESIGN

Curriculum, Scheme of Examinations and Syllabi

(With effect from 2011 admissions)

Scheme of M.Tech Programme in VLSI DESIGN

(With Effect from the Academic Year 2011 onwards)

FIRST SEMESTER

Sl No	Course Code	Name of the Subject	Hours / Week			Internal	Sem End	Total	Sem-End Exam Duration	Credits
			L	T	P					
1.	VL 11 101	CMOS VLSI Design	3	1	0	100	100	200	3	4
2.	VL 11 102	Advanced Digital System Design	3	1	0	100	100	200	3	4
3.	VL 11 103	Computer Aided Design of VLSI Circuits	3	1	0	100	100	200	3	4
4.	VL 11 104	Advanced Engineering Mathematics	3	1	0	100	100	200	3	4
5.	VL 11 105	Elective 1	3	1	0	100	100	200	3	4
6.	VL 11 106 (P)	Seminar	0	0	2	100	0	100	-	2
7.	VL 11 107 (P)	Computer Aided Design of VLSI Circuits - Laboratory	0	0	2	100	0	100	-	2
		Total	15	5	4	700	500	1200		24
		Elective 1					-	-		
1.	VL 11 105A	Electronic System Design								
2.	VL 11 105B	Digital Integrated Circuit Design								
3.	VL 11 105C	Designing with Microcontrollers								

L – Lecture, T- Tutorial, P – Practical

Scheme of M.Tech. Programme in VLSI DESIGN

SECOND SEMESTER

Sl No	Course Code	Name of the Subject	Hours / Week			Internal	End-Sem	Total	DurationEnd-Sem Exam	Credits
			L	T	P					
1.	VL 11 201	SOC Design and Verification	3	1	0	100	100	200	3	4
2.	VL 11 202	Analog VLSI Design	3	1	0	100	100	200	3	4
3.	VL 11 203	Testing & Verification of VLSI Circuits	3	1	0	100	100	200	3	4
4.	VL 11 204	Elective - II	3	1	0	100	100	200	3	4
5.	VL 11 205	Elective - III	3	1	0	100	100	200	3	4
6.	VL 11 206 (P)	Seminar	0	0	2	100	0	100	-	2
7.	VL 11 207 (P)	Testing & Verification of VLSI Circuits – Laboratory	0	0	2	100	0	100	-	2
		Total	15	5	4	700	500	1200		24
		Elective II					-	-		
1.	VL 11 204A	Low Power VLSI Design								
2.	VL 11 204B	Synthesis and Optimization of Digital Circuits								
3.	VL 11 204C	Design of Digital Signal Processing Systems								
		Elective III								
1.	VL 11 205A	High Speed Digital Design								
2.	VL 11 205B	Multimedia Compression Techniques								
3.	VL 11 205C	Design for Testability								

L – Lecture, T- Tutorial, P – Practical

Scheme of M.Tech Programme in VLSI DESIGN

THIRD SEMESTER

Sl No	Course Code	Name of the Subject	Hours / Week			Marks			Total	End-Sem Exam Duration	Credits
			L	T	P	Internal		Sem End			
1.	VL 11 301	**Elective IV**	3	1	0	100		100	200	3	4
2.	VL 11 302	**Elective V**	3	1	0	100		100	200	3	4
3.	VL 11 303 (P)	Industrial Training	0	0	0	50		-	50	-	1
4.	VL 11 304 (P)	Master Research Project Phase I	0	0	22	Guide	EC*	-	300	-	6
						150	150				
		TOTAL	6	2	22	550		200	750		15
		Elective IV						-	-		
1.	VL 11 301A	Mixed Signal System Design									
2.	VL 11 301B	FPGA Architecture & Applications									
1.	VL 11 301C	Wireless Communication Systems									
		Elective V									
1.	VL 11 302A	System Verilog									
1.	VL 11 302B	Hardware-Software Co-design									
2.	VL 11 302C	VLSI Signal Processing									

***EC – Evaluation committee, L – Lecture, T- Tutorial, P – Practical**

Scheme of M.Tech Programme in VLSI DESIGN

FOURTH SEMESTER

Sl No	Course Code	Name of the Subject	Hours / Week			Internal Evaluation		ESE*		Total	Credits
			L	T	P	Guide	CommitteeEvaluation	External Guide	Viva Voce		
1.	VL 11 401(P)	Master Research Project Phase II	0	0	30	150	150	150	150	600	12
Total			-	-	30	150	150	150	150	600	12
			* The student has to undertake the departmental work assigned by HOD								
										Marks	**Credits**
								Grand Total		**3750**	**75**

FIRST SEMESTER

VL 11 101 CMOS VLSI DESIGN

Modules	Hours
Module 1 **INTRODUCTION TO CMOS CIRCUITS** MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, MOS Transistor Theory - Introduction MOS Device Design Equations, The Complementary CMOS Inverter-DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate, The Tri State Inverter, Bipolar Devices, Resistance Estimation Capacitance Estimation, Inductance, Switching Characteristics CMOS-Gate Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing, Design Margining, Reliability.	10
Module 2 **CMOS CIRCUIT AND LOGIC DESIGN** CMOS Logic Gate Design, Basic Physical Design of Simple Gate, CMOS Logic Structures, Clocking Strategies, I/O Structures, Low Power Design	8
Module 3 **SYSTEMS DESIGN AND DESIGN METHOD** Design Strategies CMOS Chip Design Options, Design Methods, Design Capture Tools, Design Verification Tools, Design Economics, Data Sheets, CMOS Testing - Manufacturing Test Principles, Design Strategies for Test, Chip Level Test Techniques, System Level Test Techniques, Layout Design for Improved Testability.	12
Module 4 **CMOS SUB SYSTEM DESIGN** Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multiplication, Shifters, Memory Elements, Control-FSM, Control Logic Implementation.	9
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. Neil. H.E. Weste and K. Eshragian, “Principles of CMOS VLSI Design”. 2nd Edition. Addison-Wesley , 2000.
2. Douglas a. Pucknell and K. Eshragian., “Basic VLSI Design” 3rd Edition. PHI, 2000.
3. R. Jacob Baker, Harry W. LI., & David K. Boyce., “CMOS Circuit Design”, 3rd Indian reprint, PHI, 2000.

REFERENCE BOOKS:

1. Semiconductor Devices Modelling and Technology Nandita Das Guptha , Amitava Das Guptha; Prentice Hall India
2. Operation and Modeling of The MOS transistor : Yannis Tsividis 2/e Oxford University Press
3. Kang & Leblebigi “CMOS Digital IC Circuit Analysis & Design”- McGraw Hill, 2003
4. Weste and Eshraghian, “Principles of CMOS VLSI design” Addison-Wesley, 2002

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 102 ADVANCED DIGITAL SYSTEM DESIGN

Modules	Hours
Module 1 **Introduction to Digital Systems Design.** Introduction - Design of Combinational Systems – Multiple output combination circuit design – McCluskey method- Introduction to PLDs - PROM based design - PAL - Arithmetic PAL devices – Study based on PAL22V10, CPLDs (MAX3000A CPLD).	10
Module 2 **Sequential Circuit Design** – Mealy Machine, Moore Machine, State diagrams, State table minimization, Incompletely specified sequential machine, Asynchronous sequential circuit design (fundamental mode)	8
Module 3 **Asynchronous sequential circuits:** Derivation of excitation table, Race conditions and cycles, Static and dynamic hazards, Methods for avoiding races and hazards, essential hazards, Designing with SM charts – State machine charts, Derivation of SM charts, and Realization of SM charts.	12
Module 4 **VHDL** Basics - Introduction to HDL - Behavioral modeling - Data flow modeling - Structural modeling - Basic language elements – Entity-Architecture-Configurations - Subprograms and operator overloading- Packages and libraries - VHDL advanced features - Model simulation - Hardware modeling examples. Synthesis. Timing Simulation. VHDL Synthesis Issues.	9
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. “Fundamentals of Digital Design”, Charles H.Roth,Jr., PWS Pub.Co.,1998.
2. “Digital Design Fundamentals”, Kenneth J Breeding, Prentice Hall, Englewood Cliffs, New
3. Jersey.1989.
4. Smith, "Application Specific Integrated Circuits", Addison-Wesley, 1997
5. J. Bhasker, "A VHDL Primer", Addison-Weseley Longman Singapore Pte Ltd. 1992

REFERENCE BOOKS:

1. Kevin Skahill, "VHDL for Prgrammable Logic", Addison -Wesley, 1996
2. Z. Navabi, "VHDL Analysis and Modeling of Digital Systems", McGRAW-Hill, 1998
3. Sudhakar Yalamanchili, “Introductory VHDL From Simulation to Synthesis”, Prentice Hall

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 103 COMPUTER AIDED DESIGN OF VLSI CIRCUITS

Modules	Hours
Module 1 Various CAD Tools for front end and Back end design, Schematic editors, Layout editors, Place and Route tools. Introduction to VLSI Methodologies - VLSI Physical Design Automation - Design and Fabrication of VLSI Devices - Fabriction process	10
Module 2 Introduction to Design Tools: Introduction & Familiarity with Design Tools from various vendors e.g. Synopsis, Mentor Tools etc. Verilog Basics - Modeling Levels - Data Types - Modules and Ports - Instances - Basic Language Concepts - Dataflow modeling - Behavioral modeling Modeling and Simulation of systems/subsystems using Verilog HDL. Typical case studies.	12
Module 3 Layout Algorithms Circuit partitioning, placement, and routing algorithms; Design rule verification; Circuit Compaction; Circuit extraction and post-layout simulation	8
Module 4 Automatic Test Program Generation; Combinational testing D-Algorithm and PODEM algorithm; Scan-based testing of sequential circuits; Testability measures for circuits.	9
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. N.A. Sherwani, " Algorithms for VLSI Physical Design Automation ", 1999.
2. S.H. Gerez, " Algorithms for VLSI Design Automation ", 1998.4. J. Bhasker, "A VHDL Primer", Addison-Weseley Longman Singapore Pte Ltd. 1992
3. Drechsler, R., *Evolutionary Algorithms for VLSI CAD*, Kluwer Academic Publishers, Boston, 1998.
4. Verilog HDL by Samir Palnitkar

REFERENCE BOOKS:

1. VERILOG HDL SYNTHESIS: A PRACTICAL PRIMER by J Bhaskar
2. Hill, D., D. Shugard, J. Fishburn and K. Keutzer, *Algorithms and Techniques for VLSI Layout Synthesis*, Kluwer Academic Publishers, Boston, 1989.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 104 ADVANCED ENGINEERING MATHEMATICS

(Common with EDT 11 104)

Modules	Hours
Module1: Transforms and Digital Representations Signals and Systems, Linear Time Invariant Systems, The Laplace Transform, Properties, The Fourier Transform, Properties of Fourier Transform, Fourier Transform of Sequence(Fourier Series) and its properties, Fourier Analysis for Continuous and Discrete Time Signals. Z Transform and its properties. Digital Arithmetic: Fixed and Floating point representation, IEEE 754 Floating point standards, Floating point arithmetic operations	9
Module 2 : Linear Algebra Linear Equations and Matrix Algebra: Fields; system of linear equations, and its solution sets; elementary row operations and echelon forms; matrix operations; invertible matrices, LU-factorization Vector Spaces: Vector spaces; subspaces; bases ; dimension; coordinates	10
Module3: Multidimensional Transforms Introduction, 2D orthogonal & unitary transforms, Properties of unitary transforms, 1D and 2D- DFT, DCT, Walsh, Hadamard Transform, Haar Transform, Slant Transform, KLT, SVD Transform	10
Module 4: Wavelet Transform Wavelet Transform: Continuous: introduction, C-T wavelets, properties, inverse CWT. Discrete wavelet transform and orthogonal wavelet decomposition using Harr Wavelets.	10
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. **"**Linear Algebra and its Applications**"**, David C. Lay, 3rd edition, Pearson Education (Asia) Pte. Ltd, 2005
2. Digital Arithmetic, Milos D. Ercegovac, Tomas Lang, Elsevier
3. "Fundamentals of Digital Image Processing", Anil K. Jain, PHI, New Delhi
4. Digital Signal Processing: a practical approach, Emmanuel C Ifeachor, W Barrie Jervis, Pearson Education (Singapore) Pte. Ltd., Delhi
5. Wavelet transforms-Introduction to theory and applications, Raghuveer M.Rao and Ajit S. Bapardikar, Person Education

REFERENCE BOOKS:

1. Schaum's Outline for Advanced Engineering Mathematics for Engineers and Scientists, Murray R. Spiegel, MGH Book Co., New York
2. Advanced Engineering Mathematics, Erwin Kreyszing, John Wiley & Sons, NEW YORK
3. Advanced Engineering Mathematics, JAIN, R K,IYENGAR, S R K, Narosa, NEW YORK
4. Signal processing with fractals: a Wavelet - based approach, Wornell, Gregory, PH, PTR, NEW JERSEY
5. Wavelet a primer, Christian Blatter, Universities press (India) limited, Hyderabad

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 105A - ELECTRONIC SYSTEM DESIGN

(Common with EDT 11 103)

Modules	Hours
Module 1 Practical Analog & Mixed Signal Circuit Design Issues and Techniques: Passive components: Understanding and interpreting data sheets and specifications of various passive and active components, non-ideal behavior of passive components,. Op amps: DC performance of op amps: Bias, offset and drift. AC Performance of operational amplifiers: band width, slew rate and noise. Properties of a high quality instrumentation amplifier. Design issues affecting dc accuracy & error budget analysis in instrumentation amplifier applications. Isolation amplifier basics. Active filers: design of low pass, high pass and band pass filters. ADCs and DACs: Characteristics, interfacing to microcontrollers. Selecting an ADC. Power supplies: Characteristics, design of full wave bridge regulated power supply. Circuit layout and grounding in mixed signal system.	10
Module 2 Practical Logic Circuit Design Issues and Techniques: Understanding and interpreting data sheets & specifications of various CMOS& BiCMOS family Logic devices. Electrical behavior (steady state & dynamic) of CMOS & BiCMOS family logic devices. Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies. CMOS/TTL Interfacing Basic design considerations for live insertion. JTAG/IEEE 1149.1 design considerations. Design for testability, Estimating digital system reliability. Digital circuit layout and grounding. PCB design guidelines for reduced EMI.	10
Module 3 Electromagnetic Compatibility (EMC): **Designing for (EMC), EMC regulations, typical noise path, methods of noise coupling, methods of reducing interference in electronic systems.**	9

Cabling of Electronic Systems: Capacitive coupling, effect of shield on capacitive coupling, inductive coupling, effect of shield on inductive coupling, effect of shield on magnetic coupling, magnetic coupling between shield and inner conductor, shielding to prevent magnetic radiation, shielding a receptor against magnetic fields, coaxial cable versus shielded twisted pair, ribbon cables. Grounding of Electronic Systems: Safety grounds, signal grounds, single-point ground systems, multipoint-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, shield grounding at high frequencies.	
Module 4 Balancing & Filtering in Electronic Systems: Balancing, power line filtering, power supply decoupling, decoupling filters, high frequency filtering, system bandwidth. Protection Against Electrostatic Discharges (ESD): Static generation, human body model, static discharge, ESD protection in equipment design, software and ESD protection, ESD versus EMC. Packaging & Enclosures of Electronic System: Effect of environmental factors on electronic system (environmental specifications), nature of environment and safety measures. Packaging's influence and its factors. Cooling in/of Electronic System: Heat transfer, approach to thermal management, mechanisms for cooling, operating range, basic thermal calculations, cooling choices, heat sink selection.	10
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. Electronic Instrument Design, 1st edition; by: Kim R. Fowler; Oxford University Press.
2. Noise Reduction Techniques in Electronic Systems, 2nd edition; by: Henry W. Ott; John Wiley & Sons.
3. Digital Design Principles & Practices, 3rd edition by: John F. Wakerly; Prentice Hall International, Inc.
4. Operational Amplifiers and linear integrated circuits, 3rd edition by: Robert F. Coughlin; Prentice Hall International, Inc
5. Intuitive Analog circuit design by: Mark. T Thompson; Published by Elsevier

REFERENCE BOOKS:

1. Printed Circuit Boards - Design & Technology, 1st edition; by: W Bosshart; Tata McGraw Hill.
2. A Designer's Guide to Instrumentation Amplifiers; by: Charles Kitchin and Lew Counts; Seminar Materials @ http://www.analog.com
3. Errors and Error Budget Analysis in Instrumentation Amplifier Applications; by: Eamon Nash; Application note AN-539@ http://www.analog.com
4. Practical Analog Design Techniques; by: Adolofo Garcia and Wes Freeman; Seminar Materials@ http://www.analog.com
5. Selecting An A/D Converter; by:Larry Gaddy; Application bulletin @ http://www.Ti.com
6. Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies; Application note SDAA011A@ http://www.Ti.com
7. JTAG/IEEE 1149.1 deigns considerations; Application note SCTA029@ http://www.Ti.com
8. Live Insertion; Application note SDYA012@ http://www.Ti.com
9. PCB Design Guidelines For Reduced EMI; Application note SZZA009@ http://www.Ti.com

In addition, National & International journals in the related topics, manufacturer's device data sheets and application notes are to be referred to get practical application oriented information.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 105B DIGITAL INTEGRATED CIRCUIT DESIGN

(Common with EDT 11 105B)

Modules	Hours
Module 1: CMOS inverters -static and dynamic characteristics, CMOS NAND, NOR and XOR Gates	10
Module 2: Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits -Method of Logical Effort for transistor sizing -power consumption in CMOS gates- Low power CMOS design	11
Module 3: Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM	12
Module 4: Bipolar gate Design- BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.	6
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, MGH, Second Ed., 1999
2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall, 1997
3. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 2000
4. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation. New York: IEEE Press, 1998.
5. Analysis and Design of Digital Integrated Circuits, Third Edition, David A. Hodges, Horace G. Jackson, and Resve A. Saleh, McGraw-Hill, 2004.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	**Module 2**	**Module 3**	**Module 4**
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 105C DESIGNING WITH MICROCONTROLLERS

(Common with EDT 11 101)

Modules	Hours
Module 1 **8-Bit 8051 Microcontroller** Introduction to Embedded Systems. **8-Bit Microcontrollers:** A popular 8-bit Microcontroller (Intel 8051) is covered under this section **Architecture:** CPU Block diagram, Memory Organization, Program memory, Data Memory, Interrupts **Peripherals:** Timers, Serial Port, I/O Port **Programming:** Addressing Modes, Instruction Set, Programming **Microcontroller based System Design** Timing Analysis Case study with reference to 8-bit 8051 Microcontroller. A typical application design from requirement analysis through concept design, detailed hardware and software design using 8-bit 8051 Microcontrollers.	10
Module 2 **32- Bit ARM920T Processor Core** **Introduction:** RISC/ARM Design Philosophy, About the ARM920T Core, Processor Functional Block Diagram **Programmers Model:** Data Types, Processor modes, Registers, General Purpose Registers, Program Status Register, CP15 Coprocessor, Memory and memory mapped I/O, Pipeline, Exceptions, Interrupts and Vector table, Architecture revisions, ARM Processor Families. **Cache:** Memory hierarchy and cache memory, Cache Architecture – Basic Architecture of a Cache, Basic operation of a cache controller, Cache and main memory relationship, Set Associativity Cache Policy – Write policy, Cache line replacement policies, allocation policy on a cache miss Instruction Cache, Data Cache, Write Buffer and Physical Address TAG RAM **Memory Management Units:** How virtual memory works, Details of the ARM MMU, Page Tables, Translation Look-aside Buffer, Domains and Memory access permissions **ARM Instruction Set:** Data Processing instructions, Branch instructions, Load - Store instructions, Software Interrupt Instruction, Program Status Register Instruction, Loading Constants	12

Thumb Instruction Set: Thumb register usage, ARM-Thumb interworking, Branch instruction, Data processing instructions, Load - store instructions, stack instructions, software interrupt instructions. **Interrupt Handling:** Interrupts, Assigning interrupts, Interrupt latency, IRQ & FIQ exceptions, Basic interrupt stack design and implementation, Non-nested Interrupt handler	
Module 3 **ARM9 Microcontroller Architecture:** A popular ARM9 Microcontroller from Atmel (AT91RM9200) is covered under this section **AT91RM9200 Architecture:** Block Diagram, Features, Memory Mapping **Memory Controller (MC)**, Memory Controller Block Diagram, Address Decoder, External Memory Areas, Internal Memory Mapping **External Bus Interface (EBI)**, Organization of the External Bus Interface, EBI Connections to Memory Devices **External Memory Interface**, Write Access, Read Access, Wait State Management **AT91RM9200 PERIPHERALS** **Interrupt Controller:** Normal Interrupt, Fast Interrupt, AIC **System Timer (ST):** Period Interval Timer (PIT), Watchdog Timer (WDT), Real-time Timer (RTT) **Real Time Clock (RTC)** **Parallel Input/Output Controller (PIO)**	9
Module 4 **AT91RM9200 PERIPHERALS** **Universal Synchronous Asynchronous Receiver Transceiver (USART):** Block Diagram, Functional Description, Synchronous and Asynchronous Modes **Development & Debugging Tools for Microcontroller based Embedded Systems:** Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, In-Circuit Emulator (ICE), Logic Analyzer etc. Brief Architecture of Power PC.	8
Tutorial	13
Total Hours	52

TEXT BOOKS:

[1] Intel Hand Book on “Embedded Microcontrollers”, 1st Edition
[2] Muhammad Ali Mazidi, Janice Gillispie Mazidi, Rolin D. McKinlay, “The 8051 Microcontroller and Embedded Systems using Assembly and C”, 2nd Edition, Prentice Hall
[3] ARM Company Ltd. “ARM Architecture Reference Manual– ARM DDI 0100E”
[4] David Seal “ARM Architecture Reference Manual”, 2001 Addison Wesley, England; Morgan Kaufmann Publishers
[5] Andrew N Sloss, Dominic Symes, Chris Wright, “ARM System Developer's Guide - Designing and Optimizing System Software”, 2006, Elsevier
[6] ATMEL Corporation, “AT91RM9200 ARM920T Based Microcontroller Rev. 1768E-ATARM–30-Sep-05”
[7] ARM Company Ltd. “ARM920T Technical Reference Manual (Rev 1) - ARM DDI 0151C”

REFERENCE BOOKS:

[1] Ayala, Kenneth J “8051 Microcontroller - Architecture, Programming & Applications”, 1st Edition, Penram International Publishing
[2] Steve Furber, “ARM System-on-Chip Architecture”, 2nd Edition, Pearson Education
[3] Predko, Myke, “Programming and Customizing the 8051 Microcontroller”, 1st Edition, McGraw Hill International
[4] Schultz, Thomas W, “C and the 8051 Programming for Multitasking”, 1st Edition, Prentice Hall
[5] Schultz, Thomas W, “C and the 8051: Hardware, Modular Programming and Multitasking”, Vol I, 2nd Edition, Prentice Hall
[6] Stewart, James W, Miao, Kai X, “8051 Microcontroller: Hardware, Software and Interfacing”, 2nd Edition, Prentice Hall
[7] Arnold. S. Berger, “Embedded Systems Design - An introduction to Processes, Tools and Techniques”, Easwer Press
[8] Raj Kamal, “Microcontroller - Architecture Programming Interfacing and System Design” 1st Edition, Pearson Education
[9] P.S Manoharan, P.S. Kannan, “Microcontroller based System Design”, 1st Edition, Scitech Publications
[10] David Calcutt, Fred Cowan, Hassan Parchizadeh, “8051 Microcontrollers – An Application based Introduction”, Elsevier
[11] Ajay Deshmukh, “Microcontroller - Theory & Applications”, Tata McGraw Hill

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	**Module 2**	**Module 3**	**Module 4**
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 106 (P)	**SEMINAR** **Hours/week: 2**	**Credits: 2**

	Hours
Objective: To assess the debating capability of the student to present a technical topic. Also to impart training to students to face audience and present their ideas and thus creating in them self esteem and courage that are essential for engineers.	Per week 2
Individual students are required to choose a topic of their interest from Embedded Systems related topics preferably from outside the M.Tech syllabus and give a seminar on that topic about 30 minutes. A committee consisting of at least three faculty members (preferably specialized in Embedded Systems) shall assess the presentation of the seminar and award marks to the students. Each student shall submit two copies of a write up of his/her seminar topic. One copy shall be returned to the student after duly certifying it by the chairman of the assessing committee and the other will be kept in the departmental library. Internal continuous assessment marks are awarded based on the relevance of the topic, presentation skill, quality of the report and participation.	
Internal continuous assessment: 100 marks	

VL 11 107(P) COMPUTER AIDED DESIGN OF VLSI CIRCUITS LABORATORY

Maximum Marks – 100

Modules	Hours
Module 1 1. Modeling and simulation of Combinational and sequential circuits using Verilog. 2. Modeling and Simulation of ALU using Verilog. 3. Modeling and Simulation of FSMs using Verilog 4. Modeling and simulation of Memory and FIFO in Verilog	12
Module 2 1. Modeling and simulation of UART in Verilog 2. Simulation of NMOS and CMOS circuits using SPICE. 3. Modeling of MOSFET using C.	14
Total Hours	26

REFERENCE BOOKS:

1. Modern Digital Electronics by R P Jain
2. Verilog HDL by Samir Palnitkar.
3. VERILOG HDL SYNTHESIS: A PRACTICAL PRIMER by J Bhaskar

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

Mid Term Internal Test	40 Marks
Laboratory Experiments & Viva Voce	10 Marks
Final Internal Test	50 Marks
Total	**100 Marks**

SECOND SEMESTER

VL 11 201 SOC DESIGN AND VERIFICATION

Modules	Hours
Module 1 **System On Chip Design Process:** A canonical SoC Design, SoC Design flow waterfall vs spiral, topdown vs Bottom up. Specification requirement, Types of Specification , System Design process, System level design issues, Soft IP Vs Hard IP, Design for timing closure,Logic design issues Verification strategy, Onchip buses and interfaces, Low Power, Manufacturing test strategies.	10
Module 2 **Macro Design Process:** Top level Macro Design, Macro Integration, Soft Macro productization, Developing hard macros, Design issues for hard macros, Design ,System Integration with reusable macros.	8
Module 3 **SoC Verification:** Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co verification and Static net list verification. Verification architecture, Verification components, Introduction to VMM, OVM and UVM.	12
Module 4 **Design of Communication Architectures For SoCs:** On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures, Communication architecture tuners, Communication architectures for energy/battery efficient systems. Introduction to bus functional models and bus functional model based verification.	9
Tutorial	13
Total Hours	52

TEXT BOOKS

1. "SoC Verification Methodology and Techniques", Prakash Rashinkar Peter Paterson and Leena Singh. Kluwer Academic Publishers, 2001.

2. "Reuse Methodology manual for SystemOnAChip Designs", Michael Keating, Pierre Bricaud, Kluwer Academic Publishers, second edition,2001.

REFERENCE BOOKS:

1. "Design Verification: Simulation and Formal Method based Approaches", William K. Lam, Prentice Hall.
2. "System- on -a- Chip Design and Test", Rochit Rajsuman, ISBN.
3. "Multiprocessor Systemsonchips", A.A. Jerraya, W.Wolf, M K Publishers.
4. "The EDA HandBook", Dirk Jansen, Kluwer Academic Publishers.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 202 ANALOG VLSI DESIGN

Modules	Hours
Module 1 Analog MOS transistor models Temperature effects and Noise in MOS transistor MOS resistors, characterization of resistive, capacitive elements and MOS devices. Passive and active CMOS current sink/ sources– basics of single stage CMOS amplifiers common Source, common gate and source follower stages frequency response.	10
Module 2 CMOS Differential Amplifiers: CMOS Operational Amplifiers one stage and two stage gain boosting Common mode feedback (CMFB) Cascode and Folded cascade structures	8
Module 3 High Performance Opamps – High speed/ high frequency opamps, micro power opamps, low noise opamps and low voltage opamps. Current mirrors, filter implementations. Supply independent and temperature independent references Band gap references PTAT current generation and constant Gm biasing – CMOS comparators – Multipliers and wave shaping circuits – effects due to nonlinearity and mismatch in MOS circuits	12
Module 4 Switched Capacitor Circuits: First and Second Order Switched Capacitor Circuits, Switched Capacitor filters, CMOS oscillators, simple and charge pump CMOS PLLs non ideal effects in PLLs, Delay locked loops and applications, basics of CMOS data converters – Medium and high speed CMOS data converters, Over sampling converters.	9
Tutorial	13
Total Hours	52

TEXT BOOKS

1. “Analog Integrated Circuit Design”, David. A. Johns and Ken Martin, John Wiley and Sons, 2001.
2. “Design of Analog CMOS Integrated Circuit”, Behzad Razavi, Tata McGraw HILL, 2002.
3. “CMOS Analog Circuit Design”, Philip Allen & Douglas Holberg, Oxford University Press, 2002.

REFERENCE BOOKS:

1. “Analog VLSI – Signal Information and Processing”, Mohammed Ismail & Feiz , John Wiley and Sons.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 203 TESTING & VERIFICATION OF VLSI CIRCUITS

Modules	Hours
Module 1 **Introduction:** Scope of testing and verification in VLSI design process; Issues in test and verification of complex chips; embedded cores and SOCs Introduction to test benches, writing test benches in Verilog HDL.	9
Module 2 **Fundamentals of VLSI testing**, Fault models. Automatic test pattern generation, Design for testability, Scan design, Test interface and boundary scan.	9
Module 3 **System Testing** and test for SOCs, Iddq testing, Delay fault testing, BIST for testing of logic and memories, Test automation.	9
Module 4 **Design Verification Techniques** based on simulation, analytical and formal approaches, Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking. Verification of simple IPs: Memory verification, FIFO verification and Verification of RISC CPU	12
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. M. Abramovici, M. A. Breuer, A. D. Friedman, “Digital Systems Testing and Testable Design” Piscataway, New Jersey: IEEE Press, 1994
2. M. Bushnell and V. D. Agarwal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000
3. T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2000.
4. P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers, 2001.
5. Samiha Mourad and Yervant Zorian, “Principles of Testing Electronic Systems”, Wiley (2000).

REFERENCE BOOKS:

1. “SoC Verification Methodology and Techniques”, Prakash Rashinkar Peter Paterson and Leena Singh .Kluwer Academic Publishers, 2001.
2. “Reuse Methodology manual for System On A Chip Designs”, Michael Keating,
3. Pierre Bricaud, Kluwer Academic Publishers, second edition, 2001.
4. “System- on -a- Chip Design and Test”, Rochit Rajsuman, ISBN.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 204A LOW POWER VLSI DESIGN

Modules	Hours
Module 1 Introduction - Simulation - Power Analysis-Probabilistic Power Analysis.	10
Module 2 Circuit -Logic - Special Techniques - Architecture and Systems.	8
Module 3 Advanced Techniques - Low Power CMOS VLSI Design - Physics of Power Dissipation in CMOS FET Devices.	12
Module 4 Power Estimation - Synthesis for Low Power - Design and Test of Low Voltages - CMOS Circuits. Low Power Static RAM Architectures -Low Energy Computing Using Energy Recovery Techniques – Software Design for Low Power.	9
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. Gary Yeap " Practical Low Power Digital VLSI Design ", 1997.
2. Kaushik Roy, Sharat Prasad, " Low Power CMOS VLSI Circuit Design ", 20003.
3. A.P.Chandrakasan and R.W. Broadersen, Low power digital CMOS design, Kluwer,1995.

REFERENCE BOOKS:

1. CMOS Analog Circuit Design", Philip Allen & Douglas Holberg, Oxford University Press, 2002.
2. Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 204B SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

Modules	Hours
Module 1 Introduction to Synthesis and optimization: High-level synthesis: Motivation and organization Scheduling Resource sharing Data path and control synthesis	9
Module 2 Logic synthesis: Algorithms and rule-based systems, Algebraic and Boolean methods Timing issues: Sequential synthesis and retiming Semicustom libraries & library mapping Algorithms and rule-based systems Structural and Boolean matching	10
Module 3 Optimization of digital circuits: Area, Timing and power optimization. RTL Coding for area, timing and power optimization. Synthesis and Generation of area, timing and power reports: RISC CPU a case study.	10
Module 4 Introduction to Hw/Sw Codesign Problem taxonomy Embedded system design Software optimization Perspectives	10
Tutorial	13
Total Hours	52

TEXT BOOKS

1. Giovanni De Micheli, “Synthesis and Optimization of Digital Circuits”, McGraw-Hill, 1994, 5th print.
2. “Logic Synthesis”, S. Devadas, A. Ghosh and K. Keutzer, McGraw Hill, 1994.
3. R. Gupta, “Co-synthesis of Hardware and Software for Embedded Systems**”,** Kluwer 1995.

REFERENCE BOOKS:

1. Edwars M.D., *Automatic Logic synthesis Techniques for Digital Systems*, Macmillan New Electronic Series, 1992
2. Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, Pearson Education, 2005.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	**Module 2**	**Module 3**	**Module 4**
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 204C DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS

(Common with EDT 11 201)

Modules	Hours
Module 1 - Digital Signal Processor: TMS320C6713 or any other popular DSP from Texas Instruments is covered under this module Architecture: CPU Architecture, Internal Memory, CPU Data Paths control Programming: Instruction Set and Addressing Modes Code Composer Studio, Code Generation Tools, Code Composer Studio Debug Tools DSP Peripherals: Multichannel Buffered Serial Port, Transmission & Reception Timers Memory of DSP: Internal Data/Program Memory External Memory Interface	9
Module 2 - Digital Signal Processing Algorithms: Filter Design: FIR Digital filter design. Fourier Transform: DFT, FFT, Spectral Analysis DTMF Speech Processing Algorithms	10
Module 3 - Digital Signal Processing Application: Real-time Implementation: Implementation of Real-time FIR Digital filter using DSP. Implementation of Real-time Fast Fourier Transform applications using the DSP Implementation of DTMF Tone Generation and Detection. Implementation of Speech processing applications	10
Module 4 - Current trends in Digital Signal Processor:	10

FPGA Technology DSP Technology Requirements Design implementation Multiply Accumulator (MAC) and Sum of Product (SOP) Implementation of Serial/Parallel Convolver using FPGAs FPGA Based DSP System Design FIR filters FIR Theory Designing FIR filters Direct Window Design method Constant Coefficient FIR Design Direct FIR Design Cooley-Tukey FFT Algorithm implementation using FPGA	
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform, 1st Edition; by: Naim Dahnoun
2. DSP Applications using 'C' and the TMS320C6X DSK, 1st Edition; by: Rulph Chassaing
3. Digital Signal Processing: A System Design Approach, 1st Edition; by: David J Defatta J, Lucas Joseph G & Hodkiss William S; John Wiley
4. Digital Signal Processing with Field Programmable Gate Arrays: 2nd Edition, by: U. Meyer – Base, Springer
5. Real - Time Digital Signal Processing: Implementations, Applications, and Experiments with the TMS320C55X, Kuo, Sen M, Lee, Bob H, John Wiley & Sons Ltd.

REFERENCE BOOKS:

1. Digital Signal Processing, Third Edition, Sanjit K. Mitra, Tata McGRWA Hill
2. Digital Signal Processing – A Practical Guide for Engineers and Scientists, Steven W Smith, Elsevier
3. Digital Signal Processing - A Student Guide, 1st Edition; by: T.J. Terrel and Lik-Kwan Shark; Macmillan Press; Ltd.
4. Digital Signal Processing Laboratory, B. Preetham Kumar, Taylor & Francis, CCS DSP Applications
5. Introduction to Digital Signal Processing, 1st Edition; by: John G Proakis, Dimitris G Manolakis
6. Digital Signal Processing Design, 1st Edition; by: Andrew Bateman, Warren Yates

7. A Simple approach to Digital Signal processing, 1st Edition; by: Kreig Marven & Gillian Ewers; Wiely Interscience
8. DSP FIRST - A Multimedia Approach, 1st Edition; by: JAMES H. McClellan, Ronald Schaffer and Mark A. Yoder; Prentice Hall
9. Signal Processing First, 1st edition; by: James H. McClellan, Ronald W. Schafer and Mark A. Yoder; Pearson Education
10. Digital Signal Processing, 1st Edition; by: Oppenheim A.V and Schafer R.W; PH
11. Digital Processing of Speech Signals, 1st Edition; by: L.R. Rabiner and Schafer R.W; PH
12. Digital Signal Processing – Architecture, Programming and Applications, by: B. Venkataramani & M.Bhaskar; Tata McGraw Hill
13. A Practical Approach to Digital Signal Processing, by: K. Padmanabhan, S. Ananthi & R.Vijayarajeswaran; New Age International Publishers
14. Theory & Application of Digital Signal Processing, 1st Edition; by: Rabiner L.R & Gold B; PH
15. Digital Signal Processing, 1st Edition; by: P Ramesh Babu,
16. 'C' Language Algorithm for DSP, 1st Edition; by: Paul M. Embree and Bruce Kimble; PH
17. http://hometown.aol.de/uwemeyerbase/indexhtml
18. www.springer.de

In addition, National/ International journals in the field, manufacturers Device data sheets and application notes and research papers in journals are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 205A HIGH SPEED DIGITAL DESIGN

(Common with EDT 11 205A)

Modules	Hours
Module 1 **Introduction to high speed digital design.** Frequency, time and distance - Capacitance and inductance effects - High seed properties of logic gates - Speed and power -Modelling of wires -Geometry and electrical properties of wires - Electrical models of wires - transmission lines - lossless LC transmission lines - lossy LRC transmission lines - special transmission lines	10
Module 2 **Power distribution and noise** Power supply network - local power regulation - IR drops - area bonding - onchip bypass capacitors - symbiotic bypass capacitors - power supply isolation - Noise sources in digital system - power supply noise - cross talk - intersymbol interference	8
Module 3 **Signalling convention and circuits** Signalling modes for transmission lines -signalling over lumped transmission media - signalling over RC interconnect - driving lossy LC lines - simultaneous bi-directional signalling - terminations - transmitter and receiver circuits	9
Module 4: **Timing convention and synchronisation** Timing fundamentals - timing properties of clocked storage elements - signals and events -open loop timing level sensitive clocking - pipeline timing - closed loop timing - clock distribution - synchronization failure and metastability - PLL and DLL based clock aligners	12
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. Howard Johnson and Martin Graham, "High Speed Digital Design: A Handbook of Black Magic",3rd Edition, (Prentice Hall Modern Semiconductor Design Series' Sub Series: PH Signal Integrity Library), 2006
2. Stephen H. Hall, Garrett W. Hall, and James A. McCall " High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices by ", Wiley , 2007
3. Kerry Bernstein, K.M. Carrig, Christopher M. Durham, and Patrick R. Hansen "High Speed CMOS Design Styles", Springer Wiley 2006
4. Ramesh Harjani "Design of High-Speed Communication Circuits (Selected Topics in Electronics and Systems)" World Scientific Publishing Company 2006

REFERENCE BOOKS:

1. William S. Dally & John W. Poulton; Digital Systems Engineering, Cambridge University Press, 1998
2. Masakazu Shoji; High Speed Digital Circuits, Addison Wesley Publishing Company, 1996
3. Jan M, Rabaey, et all; Digital Integrated Circuits: A Design perspective, Second Edition, 2003

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 205B MULTIMEDIA COMPRESSION TECHNIQUES

(Common with EDT 11 202)

Modules	Hours
Module 1 - INTRODUCTION Special features of Multimedia – Graphics and Image Data Representations – Fundamental Concepts in Video and Digital Audio – Storage requirements for multimedia applications -Need for Compression - Taxonomy of compression techniques – Overview of source coding TEXT COMPRESSION Compaction techniques – Huffmann coding – Adaptive Huffmann Coding – Arithmetic coding – Shannon-Fano coding – Dictionary techniques – LZW family algorithms.	9
Module 2 - IMAGE COMPRESSION Transform Coding – JPEG Standard – Sub-band coding algorithms: Design of Filter banks – Wavelet based compression: Implementation using filters – EZW, SPIHT coders – JPEG 2000 standards - JBIG, JBIG2 standards.	10
Module 3 - AUDIO COMPRESSION Audio compression techniques - µ- Law and A- Law companding. Frequency domain and filtering – Basic sub-band coding – Application to speech coding – G.722 – Application to audio coding – MPEG audio, progressive encoding for audio – Silence compression, speech compression techniques – Formant and CELP Vocoders	10
Module 4 - VIDEO COMPRESSION Video compression techniques and standards – MPEG Video Coding I: MPEG – 1 and 2 – MPEG Video Coding II: MPEG – 4 and 7 – Motion estimation and compensation techniques – H.261 Standard – DVI technology – PLV performance – DVI real time compression – Packet Video.	10
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. Khalid Sayood: Introduction to Data Compression, Morgan Kauffman Harcourt India, 3rd Edition, 2010
2. David Salomon: Data Compression – The Complete Reference, Springer Verlag New York Inc., 4th Edition, 2006.

REFERENCE BOOKS:

1. Yun Q. Shi, Huifang Sun: Image and Video Compression for Multimedia Engineering - Fundamentals, Algorithms & Standards, CRC press, 2003.
2. Peter Symes: Digital Video Compression, McGraw Hill Pub., 2004.
3. Mark Nelson: Data compression, BPB Publishers, New Delhi, 2008
4. Mark S. Drew, Ze-Nian Li: Fundamentals of Multimedia, PHI, 1st Edition, 2009.
5. Watkinson, J: Compression in Video and Audio, Focal press, London.1995.
6. Jan Vozer: Video Compression for Multimedia, AP Profes, NewYork, 1995
7. Gonzalez and Woods, Digital Image Processing, 3rd Ed, PHI

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 205C DESIGN FOR TESTABILITY

Modules	Hours
Module 1 Introduction to test and design for Testability Fundamentals: Modeling: Modeling digital circuits at logic, register and structural models. Levels of Modeling, Logic Simulation Types of simulation, Delay models, element evaluation, Hazard detection , Gate level event driven simulation, Logic Fault models, Fault detection and redundancy, Fault equivalence and fault location.	9
Module 2 Testing for single Stuck Faults (SSF): Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional Testing with specific fault models, Vector Simulation ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tools.	9
Module 3 Design for Testability: Testability tradeoffs and techniques Scan Architectures and testing Controllability and Observability, Generic Boundary scan, Full integrated scan, storage cells for scan design, Board level and system level DFT approaches, Boundary scan standards, Compression Techniques – Syndrome test band signature analysis.	9
Module 4 Built in Self Test (BIST):, BIST concepts and test pattern generation , Specific BIST Architectures CSBL, BEST,RTS, LOCST, STUMPS, CBIST, CEBS,RTD, SST, CATS, CSTP, BILBO. Advanced BIST concepts and design for self test at Board level Memory BIST(M BIST):, Memory test Architectures and Techniques – Introduction to memory test, Types of memories and integration, embedded memory testing model, Memory test requirement for MBIST. Embedded core testing Introduction to automatic in circuit testing JTAG testing features.	12
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. “Digital systems Testing and testable Design”, Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, Jaico Publishing House, 2001.

2. “Introduction to VLSI Testing”, Englehood cliffs, Robert J. Feugate, Jr., Steven M. Mentyn, Prentice Hall, 1998.

REFERENCE BOOKS:

1. “Design for test for digital IC & Embedded Core Systems”, Alfred Crouch, Prentice hall.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 206 (P)	**SEMINAR** **Hours/week: 2**	**Credits: 2**

	Hours
Objective: To assess the debating capability of the student to present a technical topic. Also to impart training to students to face audience and present their ideas and thus creating in them self esteem and courage that are essential for engineers.	Per week 2
Individual students are required to choose a topic of their interest from Embedded Systems related topics preferably from outside the M.Tech syllabus and give a seminar on that topic about 30 minutes. A committee consisting of at least three faculty members (preferably specialized in Embedded Systems) shall assess the presentation of the seminar and award marks to the students. Each student shall submit two copies of a write up of his/her seminar topic. One copy shall be returned to the student after duly certifying it by the chairman of the assessing committee and the other will be kept in the departmental library. Internal continuous assessment marks are awarded based on the relevance of the topic, presentation skill, quality of the report and participation.	
Internal continuous assessment: 100 marks	

VL 11 207 (P) TESTING & VERIFICATION OF VLSI CIRCUITS - LABORATORY

Maximum Marks – 100

Modules	Hours
Module 1 1. Verilog Simulation and RTL Verification a) Memory b) Clock Divider and Address Counter c) n-Bit Binary Counter and RTL Verification 2. Finite State Machines Implement and Verify Using Verilog File I/O 3. Different types of TBs for memory and adder/subtractor	12
Module 2 1. Basic Verification environment for FIFO/UART 2. Verification Planning for FIFO/UART a) Development of the test cases as per the verification plan b) Generation and Analysis of Code coverage Reports 3. Writing assertions for FIFO	14
Total Hours	26

REFERENCE BOOKS:

1. Verilog HDL by Samir Palnitkar.
2. T. Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2000. P. Rashinkar, Paterson and L. Singh,
3. "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers, 2001.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

Mid Term Internal Test	40 Marks
Laboratory Experiments & Viva Voce	10 Marks
Final Internal Test	50 Marks
Total	**100 Marks**

THIRD SEMESTER

VL 11 301A MIXED SIGNAL SYSTEM DESIGN

(Common with EDT 11 301A)

Topics	Hours
Module 1 Introduction PN Junctions, Bipolar Vs Unipolar Devices, MOS Transistor operation, MOS Transistor as a Switch, NMOS ,PMOS and CMOS Switches, CMOS Inverter AC and DC Characteristics, Analog Signal Processing, Example of Analog Mixed Signal Circuit Design	8
Module 2 Digital Sub Circuits CMOS Logic implementation basics- Logic gates and Flip flops –Transmission Gates, TG based implementation of multiplexers, de-multiplexers, encoders, decoders. Digital Circuits like ALU, Comparator, Parity generator, Timer, PWM,SRAM and DRAM, CAM	10
Module 3 Analog Sub circuits Ideal Operational Amplifier, Inverting and Non-inverting configuration Differential amplifier basics, VCO, PLL, Comparator characteristics, two stage open loop comparator ,Switched capacitor fundamentals, Switched capacitor amplifier	10
Module 4 Data Converters **DAC** : Static &Dynamic Charatersitics,1 Bit DAC, String DAC, Fully Decoded DAC,PWM DAC, Current scaling, voltage scaling DACs **ADC** : Static &Dynamic Characteristics, Nyquist Criteria , Sample & Hold Circuit ,Quantization error, Concept of over sampling, Counting ADC, Tracking ADC, Successive approximation ADC, Flash ADC, Dual Slope ADC **Over sampling Data Converters** : Over sampling fundamentals, Delta –Sigma Converter basics, $\Delta \sum$ Modulator	11
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. Gray Paul R, Meyer, Robert G, Analysis and Design of Analog Integrated Circuits, 3rd edition, John Wiley & Sons.
2. Jacob Baker, "CMOS Mixed-Signal circuit design", A John Willy & Sons, inc., publications, 2003.
3. Professor Bernhard Boser -"Analysis and Design of VLSI Analog-Digital Interface Integrated Circuits" "Addison Wisely publications" (1991).

REFERENCE BOOKS:

1. D A John, Ken Martin, Analog Integrated Circuit Design, 1st Edition, John Wiley
2. CMOS Analog Circuit Design, 2nd edition; by: Allen, Phillip E, Holberg , Douglas R, Oxford University Press, (Indian Edition
3. Ken Martin, Digital Integrated Circuit Design, John Wiley
4. Sedra & Smith, Microelectronics Circuits, 5th Edition, Oxford University Press, (Indian Edition)
5. Jan M. Rabaey, Anantha Chadrakasan, B. Nikolic ,Digital Integrated Circuits – A Design Perspective 2nd Edition, Prentice Hall of India (Eastern Economy Edition).
6. Sung-Mo Kang**,** Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis & Design,2nd Ed, Tata McGraw Hill

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 301B FPGA ARCHITECTURE AND APPLICATIONS

Modules	Hours
Module 1 Programmable logic Devices: ROM, PLA, PAL, CPLD, FPGA Features, Architectures and Programming. Applications and Implementation of MSI circuits using Programmable logic Devices.	8
Module 2 FPGAs: Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs. Introduction to advanced FPGAs: Xilinx Virtex and ALTERA Stratix	10
Module 3 Finite State Machines (FSM): Top Down Design, State Transition Table, State assignments for FPGAs,Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine. FSM Architectures: Architectures Centered around non registered PLDs, Design of state machines centered around shift registers, One_Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.	12
Module 4 System Level Design: Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs. System level design using mentor graphics/Xilinx EDA tool (FPGA Advantage/Xilinx ISE), Design flow using FPGAs. Case studies: Design considerations using FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.	9
Tutorial	13
Total Hours	52

TEXT BOOKS

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.
2. Engineering Digital Design - RICHARD F.TINDER, 2nd Edition, Academic press.
3. Fundamentals of logic design-Charles H. Roth, 4th Edition Jaico Publishing House.

REFERENCE BOOKS:

1. Digital Design Using Field Programmable Gate Array, P.K. Chan & S. Mourad, 1994, Prentice Hall.
2. Field programmable gate array, S. Brown, R.J. Francis, J. Rose, Z.G. Vranesic, 2007, BS

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 301C WIRELESS COMMUNICATION SYSTEMS

(Common with EDT 11 302A)

Modules	Hours
Module 1 - Introduction to Wireless Systems: Evolution of Wireless Communication, Cordless Telephones, Paging and messaging systems, Cellular Systems, Analog and Digital Cellular, Modulation techniques, Frequencies used and licensing, Spread Spectrum Technologies, Multiple Access Techniques for Wireless Communications, Satellite-based wireless Communications, GPS	9
Module 2 - Cellular Systems: Cellular carriers and Frequencies, Channel allocation, Cell coverage, Cell Splitting, Microcells, Picocells, Handoff, 1^{st}, 2^{nd}, 3^{rd} and 4^{th} Generation Cellular Systems, GSM, CDMA GPRS, EDGE, EVDO CDMA2000, UMTS, WCDMA, LTE, Wireless Web connectivity, Mobile IP, Wireless in local loop (WLL)	10
Module 3 - Radio propagation in Mobile Systems: Antenna Basics, Cellular and PCS Antennas, MIMO, Mobile Radio Propagation: Free-space propagation model, Two-Ray Model, Outdoor and indoor propagation models, Fading Channels, Raleigh and Ricean Distribution.	11
Module 4 - Wireless LANs and PANs: Wireless LANs: 802.11,802.11a/b/g, 802.16-WiMAX, UWB Communications, Wireless Personal Area Networks, BlueTooth, BlueTooth Protocol Architecture, IEEE 802.15 standards, ZigBee, Sensor Networks, Interfacing problems and co-existence strategies in Sensor Networks, MAC and Routing protocols in Sensor Networks.	9
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. Wireless Communications – Principles and Practice; by Theodore S Rappaport, Pearson Education Pte. Ltd., Delhi
2. Wireless Communication Technology; By: Blake, Roy; Delmar, New York.
3. Wireless Communications and Networking; By: Stallings, William; Pearson Education Pte. Ltd., Delhi
4. Bluetooth Revealed; By: Miller, Brent A, Bisdikian, Chatschik; Addison Wesley Longman Pte Ltd., Delhi

REFERENCE BOOKS:

1. Mobile and Personal Communications Services and Systems; 1st Edition; By: Raj Pandya; PHI, New Delhi
2. Fundamentals of Wireless Communication by Tse David and Viswanath Pramod, Cambridge University press, Cambridge
3. Mobile Communications; By: Schiller, Jochen H; Addison Wesley Longman Pte Ltd., Delhi
4. 3G Networks: Architecture, protocols and procedures based on 3GPP specifications for UMTS WCDMA networks, By Kasera, Sumit, Narang, and Nishit, TATA MGH, New Delhi
5. Mobile Communications Engineering; Theory and Applications, By: Lee, William C Y; MGH, New York
6. Wireless Sensor Networks: information processing by approach, ZHAO, FENG, GUIBAS and LEONIDAS J, ELSEVIER, New Delhi
7. Wireless Network Evolution: 2G to 3G by GARG, VIJAY K, Pearson Education (Singapore) Pte. ltd., Delhi

In addition, manufacturers Device data sheets, IEEE publications and application notes are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 302A SYSTEM VERILOG

Modules	Hours
Module 1 Introduction to functional verification languages, Introduction to System Verilog, System Verilog data types. System Verilog procedures, Interfaces and modports, System Verilog routines.	9
Module 2 Introduction to object oriented programming, Classes and Objects, Inheritance, Composition, Inheritance v/s composition, Virtual methods. Parameterized classes, Virtual interface, Using OOP for verification, System Verilog Verification Constructs	9
Module 3 System Verilog Assertions: Introduction to assertion, Overview of properties and assertion, Basics of properties and sequences, Advanced properties and sequences, Assertions in design and formal verification, some guidelines in assertion writing.	9
Module 4 Coverage Driven Verification and functional coverage in SV: Coverage Driven Verification, Coverage Metrics, Code Coverage, Introduction to functional coverage, Functional coverage constructs, Assertion Coverage, Coverage measurement, Coverage Analysis SV and C interfacing: Direct Programming Interface (DPI)	12
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. “SystemVerilog for Design” : A Guide to Using SystemVerilog for Hardware Design and Modeling Sutherland, Stuart, Davidmann, Simon, Flake, Peter2nd ed., 2006
2. “SystemVerilog for Verification”: A Guide to Learning the Testbench Language Features, Chris Spear, 2006
3. “Hardware Verification with System Verilog”: An Object-Oriented Framework Mintz, Mike, Ekendahl, Robert 2007

REFERENCE BOOKS:

1. “Writing Testbenches using SystemVerilog” Bergeron, Janick 2006,
2. “A Practical Guide for SystemVerilog Assertions” Meyyappan Ramanathan

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 302B HARDWARE-SOFTWARE CO-DESIGN

Modules	Hours
Module 1 Introduction: Motivation hardware & software co-design, system design consideration, research scope & overviews Hardware Software back ground: Embedded systems, models of design representation, the virtual machine hierarchy, the performance3 modeling, Hardware Software development	9
Module 2 Co-design Concepts: Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software tradeoffs, co-design.	9
Module 3 Methodology for Co-Design: Amount of unification, general consideration & basic philosophies, a framework for co-design Unified Representation for Hardware & Software: Benefits of unified representation, modeling concepts. An Abstract Hardware & Software Model: Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model Performance Evaluation: Application of t he abstract Hardware & Software model, examples of performance evaluation	12
Module 4 Object Oriented Techniques in Hardware Design: Motivation for object oriented technique, data types, modeling hardware components as classes, designing specialized components, data decomposition, Processor example.	9
Tutorial	13
Total Hours	52

TEXT BOOKS

1. Sanjaya Kumar, James H. Ayler **"**The Co-design of Embedded Systems: A Unified Hardware Software Representation**",** Kluwer Academic Publisher, 2002 .
2. H. Kopetz, "Real-Time Systems", Kluwer, 1997.
3. R. Gupta, "Co-synthesis of Hardware and Software for Embedded Systems", Kluwer 1995.

REFERENCE BOOKS:

1. S. Allworth, "Introduction to Real-time Software Design", Springer-Verlag, 1984.
2. C. M. Krishna, K. Shin, "Real-time Systems", Mc-Graw Hill, 1997
3. Peter Marwedel, G. Goosens, "Code Generation for Embedded Processors**"**, Kluwer Academic Publishers, 1995.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	**Module 2**	**Module 3**	**Module 4**
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 302C VLSI SIGNAL PROCESSING

Modules	Hours
Module 1 An overview of DSP concepts-Linear system theory- DFT, FFT- realization of digital filters- Typical DSP algorithms- DSP applications- Data flow graph representation of DSP algorithm.- Loop bound and iteration bound Retiming and its applications.	12
Module 2 Algorithms for fast convolution- Algorithmic strength reduction in filters and transforms- DCT and inverse DCT- Parallel FIR filters- Pipelining of FIR filters- Parallel processing- Pipelining and parallel processing for low power.	9
Module 3 Pipeline interleaving in digital filters- Pipelining and parallel processing for IIR filters- Low power IIR filter design using pipelining and parallel processing- Pipelined adaptive digital filters.	9
Module 4 State variable description of digital filters- Round off noise computation using state variable description- Scaling using slow-down, retiming and pipelining.	9
Tutorial	13
Total Hours	52

TEXT BOOKS:

1. K.K. Parhi, VLSI Digital Signal Processing Systems, John-Wiley, 1999.
2. Pirsch, P., Architectures for Digital Signal Processing, Wiley, 1999.

REFERENCE BOOKS:

1. Allen, J., Computer Architectures for Digital Signal Processing, Proceedings of the IEEE, Vol.73, No.5, May 1985
2. Bateman A., and Yates, W., *Digital Signal Processing Design*, Computer Science Press, New York
3. S.Y. Kung, H.J. White House, T. Kailath, *VLSI and Modern Signal Processing, Prentice Hall*, 1985

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be a minimum of two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 100 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 20 marks	Question 3 : 20 marks	Question 5 : 20 marks	Question 7 : 20 marks
Question 2 : 20 marks	Question 4 : 20 marks	Question 6 : 20 marks	Question 8 : 20 marks

VL 11 303 (P)	**INDUSTRIAL TRAINING** **Hours/week: 30 (during the period of training)**	**Credits: 1**

Objective: To enable the student to correlate theory and industrial practice.

The students have to arrange and undergo an industrial training of minimum two weeks in an industry preferably dealing with electronic design during the semester break between semester 2 and semester 3 and complete within 15 calendar days from the start of semester 3. The students are requested to submit a report of the training undergone and present the contents of the report before the evaluation committee. Evaluation committee will award the marks of end semester based on training quality, contents of the report and presentation.

End semester Examination: Marks 50

VL 11 304(P)	MASTER RESEARCH PROJECT PHASE I **Hours/week: 22**	**Credits: 6**

Objective:

To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes. The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

The project work can be a design project/experimental project and/or computer simulation project on any of the topics in electronics design related topics. The project work is allotted individually on different topics. The students shall be encouraged to do their project work in the parent institute itself. If found essential, they may be permitted to continue their project outside the parent institute, subject to the conditions in clause 10 of M.Tech regulations. Department will constitute an Evaluation Committee to review the project work. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members.

The student is required to undertake the master research project phase 1 during the third semester and the same is continued in the 4thsemester (Phase 2). Phase 1 consist of preliminary thesis work, two reviews of the work and the submission of preliminary report. First review would highlight the topic, objectives, methodology and expected results. Second review evaluates the progress of the work, preliminary report and scope of the work which is to be completed in the 4th semester. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members.

Internal Continuous assessment:

SEMESTER 4

VL 11 401(P)	MASTERS RESEARCH PROJECT PHASE II **Hours/week: 30**	**Credits: 12**

Objective:

To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes. The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

Master Research project phase II is a continuation of project phase I started in the third semester. There would be two reviews in the fourth semester, first in the middle of the semester and the second at the end of the semester. First review is to evaluate the progress of the work, presentation and discussion. Second review would be a pre-submission presentation before the evaluation committee to assess the quality and quantum of the work done. This would be a pre qualifying exercise for the students for getting approval by the departmental committee for the submission of the thesis. At least one technical paper is to be prepared for possible publication in journal or conferences. The technical paper is to be submitted along with the thesis. The final evaluation of the project will be external evaluation.

Internal Continuous assessment:

	Guide	**Evaluation Committee**
First Review	**50**	**50**
Second Review	**100**	**100**
Total	**150**	**150**

End Semester Examination:

Project Evaluation by external examiner : 150 marks

Viva Voce by external and internal examiners : 150 marks