Power Factor Correction Using Integrated UPFC for Induction Motor

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Abstract –This paper introduces an adaptive control strategy of integrated UPFC for power factor correction of induction motor ,as most of the industrial application use induction motor ,which work on lagging power factor of the power supplied .This lagging power factor will draw more current from the power factor is improved, automatically energy will be saved. The power factor improvement is a goal of electricity conservation. At no- load, power factor of the induction motor is very low and it improves no load to full load power factor is still more improved by connecting integrated UPFC in shunt to the motor circuit.

Keywords -Adaptive control strategy. Power factor correction, Integrated UPFC(SAPF – shunt active power filter), induction motor.

1. INTRODUCTION

The main objective of this study is to design an energy saving scheme for an industrial distribution network. This can be achieved by decreasing the network losses and improving the main electric load operation to a better efficiency level. The designed scheme is concerned with improving the power factor of the distribution network by adding S A P F to the network at optimal size and location.

Industrial power distribution networks encounters increase in power losses and increase in the type of load is accompanied with low powerfactor which leads to huge transfer of reactive power from the utility through the network. The main drawback of this problem is increased the losses.It can result in poor reliability, safety problems and higher energy costs.

The actual amount of power being used or dissipated in a circuit is called true power. The reactive loads such as inductors and capacitors produce reactive power.The linear combination of true power and reactive power is called apparent power.Inductive loads are Induction motors, transformers and reactors. Low power factor does not create much problem in domestic areas but cause serious problems in industries because large number of induction motors are used in industries.

II PRELIMINARIES A) POWER FACTOR

In an AC circuits there is generally a phase difference between tvoltage and current. The term $\cos(\phi)$ is known as the power factor of the circuit. If the circuit is inductive, the current is lags behind the voltage and the power factor is called lagging power factor and if the circuit is capacitive then the current leads to voltage and power factor is said to be leading power factor.

The average power in a ac circuit is expressed in terms of rms current and voltage.

P=VIcos(Ø)

A purely resistive load (incandescent lamps, electric heating elements) would have a power factor of 1.0 (unity).

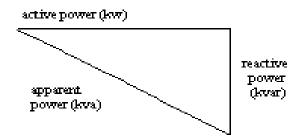
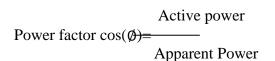


Fig 1 Power factor triangle in terms of power From the figure $(KVA)^2=(KW)^2+(KVAR)^2$



Thus power factor may also defined as the ratio of active power to the apparent power.

Power factor correction is a technique of counteracting the undesirable effects of electrical loads that create a power factor that is less than one. Power factor correction may be applied either by an electrical power transmission utility to improve the stability and efficiency of the transmission network or correction may by individual be installed electrical customers to reduce to reduced the cost charges to them by their electricity suppliers.

Low power factor is an issue, which can be solved by adding power factor correction capacitors to the plant distribution system. Capacitors work as reactive current generators "providing" needed reactive power (KVAR) into the power supply. By supplying their own source of reactive power, the industrial user frees the utility from having to supply it, and therefore the total amount of apparent power supplied by the utility will be less. Power factor correction capacitors reduce the total current drawn from the distribution system and subsequently increase the system's capacity by raising the power factor level.

B) POWER FACTOR OF AN INDUCTION MOTOR

The only possible source of excitation in an induction machine is the stator input. The induction motor therefore must operate at a lagging power factor. This power factor is very low at no load and increases to about 85 to 90 percent at full load, the improvement being caused by the increased real-power requirements with increasing load.

The presence of air-gap between the stator and rotor of an induction motor greatly increases the reluctance of the magnetic circuit. Consequently, an induction motor draws a large magnetizing current (Im) to produce the required flux in the air-gap.

- At no load, an induction motor draws a large magnetizing current and a small active component to meet the no-load losses. Therefore, the induction motor takes a high noload current lagging the applied voltage by a large angle. Hence the power factor of an induction motor on no load is low i.e., about 0.1 lagging.
- (ii) When an induction motor is loaded, the active component of current increases while the magnetizing component remains same. So, the power factor of the motor is increased. However, because of large value of magnetizing current, the power factor of the induction motor even at full load exceeds 0.9 lagging.

C) UNIFIED POWER FLOW CONTROLLER

Today, there has been large demand on transmission network, and the demand will continue to increase due to increase in large number of non-utility generator and intensified competition among them. To satisfy the demand, either new transmission lines have to be constructed or capacities of transmission lines have to be increased. As an effective solution, FACT devices are used to improve the power flow control.

AC Flexible Transmission System(FACTS) have the potential to increase the capacity of the transmission through both Functional network Versatility And Control Flexibility. FACTS controller have the capability of direct control on transmission line by changing the transmission parameters like voltage, line impedance and power angle of transmission line.

Among the FACT devices, Unified Power Flow Controller (UPFC) and Interline Power Flow Controller (IPFC) are the more advanced devices. UPFC is the combination of STATCOM and SSSC. UPFC performs both Shunt Compensation and Series Compensation.

Power flow through an alternative current line is a function of line impedance, the magnitude of sending and receiving end voltage and the phase angle between these voltages. The power flow can be increased, firstly by, decreasing the line impedance, secondly by, increasing the voltage and finally by, increasing the phase angle between the voltage. In this work power flow is controlled by controlling the phase angle.

D) DESIGN OF SAPF DEVICES

To obtain a suitable design template for the power converter and passive components, it is necessary to determine the compensation requirements imposed by the load. First step is to calculate the power rating of the power converter used in the SAPF. This power rating can be obtained as a function of load characteristics,

$$S_{SAPF} = \frac{\sqrt{(\sin \varphi_1)^2 + THD^2}}{\sqrt{1 + THD^2}} * Sload$$

Where, $\varphi 1$ is the minimum angle of load power factor and "THD" is the maximum total harmonic distortion of the load current. If only harmonic compensation is required, the power rating of the S_{SAPF} can be determined by

$$S_{SAPF} = \frac{THD}{\sqrt{1+THD^2}} * Sload$$

The design of the DC link capacitor can be developed by computing the energy balance of the SAPF. Therefore, the active power that is injected in to the SAPF system by the power converter is expressed as

$$p_{conv}(t) = p_s(t) - p_1(t)$$

= $\bar{p}_{conv} + \tilde{p}_{conv}$

where, \bar{p}_{conv} and \tilde{p}_{conv} are the dc and ac component of $p_{conv}(t)$ respectively. Considering that converter power loss can be approximated by a constant term p_{loss} , the magnitude of \bar{p}_{conv} can be given by

$$p_{conv} = \frac{1}{2}(V_s I_l - V_s I_{l(1)} \cos \phi_{(1)})$$

Where V_s , I_l and $I_{l(1)}$ are the rms of the grid voltage, the load current, and the fundamental of load current, and $\cos \phi_{(1)}$ is the load power factor. Therefore, the energy stored in the DC Link capacitor can be determined as

$$\frac{1}{2}C\Delta v_c^2 = (\bar{p}_{conv} - p_{loss}) * \Delta t$$

Thus, the voltage ripple of the dc link is expressed by

$$\Delta v_C = \sqrt{\left(\frac{V_s I_l - V_s I_{l(1)} \cos \phi_{(1)} - 2p_{loss}}{C} * \Delta t\right)}$$

Therefore mentioned equation shows that the ripple of dc link voltage can be computed as a function of energy stored in the capacitor. Based on this ripple, it is possible to design the capacitors of the dc link.

The design of filter inductor is based upon the following criteria.

- 1. Limiting the high frequency component of injected current.
- 2. Instantaneous $\frac{di_f}{dt_{(max)}}$ generated by the active filter should be greater than $\frac{di_f}{dt}$ of the load.

Based on these assumptions, the maximum ripple of the filter current can be determined as

$$\Delta i_f(t) = \frac{1}{2l_f} \int_0^{T_s/2} (v_f(t) - v_s(t)) dt$$

Where l_f is the filter inductance, $v_f(t) = q_{sw}(t)\frac{\bar{v}_c}{2}$, and $q_{sw}(t)$ is the switching function, which defines the duty cycle of power switches. Solving above equation for the worst case, the filter current ripple can be given by

$$\Delta i_{f(max)} \approx \frac{\pi(\bar{v}_{C} - 2\hat{v}_{s})}{2\omega_{sw}l_{f}}$$

Where, \hat{v}_s is the amplitude of the power main voltage vector and ω_{sw} is the switching frequency of the power converter. Next equation determines the filter inductance based on maximum derivative of the load current. This ^{r*estriction} can be expressed analytically by

$$\left[\frac{di_f}{dt}\right]_{max} \approx \frac{1}{l_f} \left(\frac{\bar{v}_c}{2} - \hat{v}_s\right)$$

The restriction on dc link voltage for achieving the desired the maximum derivative filter current can be established as

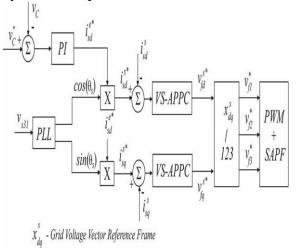
$$\bar{v}_C \ge 2(l_f) \left[\frac{di_l}{dt} \right] + \hat{v}_s$$

Based on the equation mentioned earlier, it is possible to design the power rating of the power converter and the main passive components employed on the implementation of SAPF.

E) CONTROL SCHEME

Fig.2 presents the block diagram of the proposed robust control scheme for the SAPF. In this block diagram, the dc-link voltage is regulated by a PI controller with antiwindup. It is done by generating the reference current i_{sd}^{e*} , which determines the active power component. The system phase angle of the power-grid voltage vector θ_s , determined by using a PLL. Thus, the reference phase current can be obtained by $i_{sd}^{e*} = i_{sd}^e \cos \theta_s$ and $i_{sd}^{e*} =$ $i_{sd}^e \sin \theta_s$ respectively. The reference current i_{sd}^{e*} is defined in a manner to guarantee the active power balance of the SAPF system. The phase current of the power grid are indirectly regulated by the proposed VS-APPC current controllers by generated proper active filter phase current voltage $v_{fd}^{s'*}$ and $v_{fq}^{s'*}$, respectively. These VS-APPS current controllers will be described next. The unmodeled disturbance i_{edq}^{s} and $i_{0dq}^{s'}$ can be estimated and introduced into the algorithm of VS-APPS current controllers. However, theoretical studies and experimental essays have shown that this control scheme has the capability of compensating such unmodeled $\frac{x_{dq}^{s}}{123}$ disturbance. Block perform orthogonal transformations from the dq^s reference frame to the three-phase system,

which is used for converting $v_{fdq}^{s'*}$ and $v_{f123}^{s'*}$. Based on these reference voltages, a suitable PWM strategy determines the duty cycle of VSI power switches.



x^e_{da} - Synchronous Reference Frame

Fig.2 Block Diagram of the Control Strategy

III PROPOSED METHODOLOGY

A) VS-APPS current controllers

The first approach of VS-APPC was presented in [26].However, this control structure does not deal with unmodeled disturbance.To overcome this,a modification was introduced in[27]as a solution for current control loop of an induction machine motor drive system.Here,we use this control scheme for implementing the current controllers of the proposed SAPF.

Let us consider the first-order SAPF current-voltage transfer function given by(15) whose plant parameters a_s and b_s are known with uncertainties. This main objectives of the control strategy is to estimate the values of parameters a_s and b_s to generate the inputs v_{fdq}^{s*} so that the power –grid phase current i_{sdq}^{s} follow their respective reference i_{sdq}^{s*} so that the closed-loop poles of the current control

loop are assigned to those of Hurwitz's polynomial $A_{s}^{*}(s)$ given by

$$A_{s}^{*}(s) = s^{3} + \alpha_{2}^{*}s^{2} + \alpha_{1}^{*}s + \alpha_{0}^{*}$$

Where coefficients \propto_2^*, \propto_1^* and \propto_0^* determines the closed loop performance requirements

$$A_{s}^{*}(s) = (s + \omega_{c})^{3}$$

Where ω_c is the desired controller bandwidth. The coefficients \propto_2^*, \propto_1^* , and \propto_0^* from the equation

$$A_{s}^{*}(s) = s^{3} + \alpha_{2}^{*}s^{2} + \alpha_{1}^{*}s + \alpha_{0}^{*}$$

Where coefficients $\alpha_{2,}^{*}\alpha_{1,and}^{*}\alpha_{0}^{*}$ determine the closed-loop performance requirements

$$A_{s}^{*}(s)=(s+\omega_{c})^{3}$$

Where ω_c is the desired controller bandwidth. The coefficients $\alpha^*{}_{2,}\alpha^*{}_{1,}$ and $\alpha^*{}_{0}$ from (26) are calculated by

$$\alpha^*_{2} = 3\omega_{c}$$
$$\alpha^*_{1} = 3\omega^2_{c}$$
$$\alpha^*_{0} = \omega^3_{c}.$$

In order to estimate the parameters a_s and b_s consider the SAPF filter dq current-voltage first order plant described by

$$\frac{di_{isdq}^{s}}{dt} = -a_s i_{sdq}^{s} - b_s v_{fdq}^{s*}$$

An adaptive law can be obtained for generating estimates \hat{a}_s and \hat{b}_s by using the observed signals $v^{s^*}_{fdq}$ and $i^{s^*}_{sdq}$.considering an arbitrary positive constant $a_m>0$,we can rewrite(31) by adding and subtracting the term $a_mi^s_{sdq}$ as

$$\frac{d\hat{\imath}_{sdq}^{s}}{dt} = -a_{m}\hat{\imath}_{sdq}^{s} + (a_{m} - \hat{a}_{s})\hat{\imath}_{sdq}^{s\prime} - \hat{b}_{s}v_{fdq}^{s*}$$

Where \hat{a}_s and \hat{b}_s are the estimates for a_s and b_s , respectively. The amplitude a_m defines the convergence speed of the estimated currents $\hat{\iota}^s_{sdq}$ [28].The estimation error can be defined by

$$\varepsilon_{0dq} = i_{sdq}^{s} - \hat{\iota}_{sdq}^{s}$$

In the traditional indirect APPC scheme, adaptive laws driven by the errors ε_{0dq} are used for generating estimates \hat{a}_s and \hat{b}_s can be estimated by using the following switching laws

$$\hat{a}_{s} = -\bar{a}_{s} \operatorname{sgn}(\varepsilon_{odq} i_{sdq}^{s})$$

 $\hat{b}_{s} = \overline{b}_{sgn}(\varepsilon_{0dq} v^{s*}_{fdq}) + b_{s(nom)}$

Since the following restrictions are satisfied $\bar{a}_s > a_s$ and $\bar{b}_s > b_s - b_{s(nom)}$, with $b_{s(nom)}$ being the nominal value of b_s . This guarantees that $\varepsilon_{odq}=0$ and those are the globally asymptotically stable equallibrium points. The pole placements and tracking objectives of the proposed VS-APPC are achieved if the following control law is employed

$$Q_{m}(s)L(s)V_{fdq}^{s*}(s) = -P(s)(I_{fdq}^{s}(s) - I_{sdq}^{s*}(s))$$

This addresses to the implementation of controllers transfer functions

$$\Gamma_{sdq}(s) = \frac{P(s)}{Q_m(s)L(s)}$$

Where $Q_m(s)$ is the internal model (IMP) of reference currents I_{sdq}^{S*} ; P(s) and L(s) are the polynomials(with L(s) monic).Q_m(s) is chosen to satisfy $Q_m(s)I_{sdq}^{S*}(s)=0$.For the first-order SAPF current-voltage control plant and considering that the VS-APPC control algorithm is implemented on the stationary reference

frame, which results in sinusoidal reference currents, a suitable choice for the controller polynomials are $Q_m(s) = s^2 + \omega_s^{*2}$, L(s)=1, and $P(s) = \widehat{p2s}^2 + \widehat{p1s} + \widehat{p0}$, where ω_s^{*} is the angular frequency of the voltage vector of source. This choice results in a current controller with the following transfer function

$$T_{sdq}(s) = \frac{\widehat{p2s^2} + \widehat{p1s} + \widehat{p0}}{s^2 + \omega_s^{*2}}$$

By solving the Diophantine equation for a desired Hurwitz polynomial A_s^* , the coefficients $\widehat{p2}$, $\widehat{p1}$, and $\widehat{p0}$ can be determined by

$$\widehat{p2} = \frac{\alpha_2^* - \widehat{a_s}}{\widehat{b_s}}$$
$$\widehat{p_1} = \frac{\alpha_1^* - \omega_s^{*2}}{\widehat{b_s}}$$

$$\widehat{p_{0}} = \underbrace{\overset{\propto_{0}^{*} - \omega_{s}^{*\widehat{a_{s}}}}{\widehat{b_{s}}}}_{\overline{s_{s}}}$$

$$\overbrace{s_{s}}^{s^{*}} \underbrace{c_{s}}_{c} Current Controller} \underbrace{G_{i}(s)}_{s^{*}} \underbrace{SAPF}_{s + \widehat{a_{s}}} \underbrace{b_{s}}_{i_{sdq}} \underbrace{i_{sdq}}_{s + a_{s}} \underbrace{b_{s}}_{i_{sdq}} \underbrace{i_{sdq}}_{i_{sdq}} \underbrace{c_{i}}_{i_{sdq}} \underbrace{c_{i}}_{i_{$$

Fig 3 Block diagram of proposed VS-APPC controller

The control signal v_{fdq}^{s*} generated at the outputs of VS-APPC controller can be determined by

$$\frac{dx_1^s}{dt} = x_2^s + \hat{p}_1 \varepsilon_{idq}^s$$
$$\frac{dx_2^s}{dt} = -\omega_s^{*2} x_1^s + (\hat{p}_0 - \omega_s^2 \hat{p}_2) \varepsilon_{idq}^s$$
$$v_{fdq}^{s*} = x_1^s + \hat{p}_2 \varepsilon_{idq}^s$$

Where $\varepsilon_{idq}^{s} = i_{sdq}^{s*} - i_{sdq}^{s}$

The block diagram of the VS-APPC control algorithm for a SAPF current control loop is presented in fig 3. The SAPF model generates the estimate of the source phase currents $i_{sdq}^{\widehat{s}}$. The system controller regulates the phase currents $i_{sdq}^{\widehat{s1}}$ and

compensates the modeled disturbances i_{edq}^{s} and i_{0dq}^{s} . The comparison between the estimates of the phase currents i_{sdq}^{s} and used for computing the estimation errors ε_{0dq} . To attenuate the current harmonics above the controller bandwidth, a afirst-order low-pass filters is introduced in the main current measurement, which is represented by block $G_i(s)$ given by

$$G_i(s) = \frac{1}{1 + sTf}$$

Where Tf is the low-pass time constant based on the suitable cutoff frequency. The errors ε_{idq}^{s} , together with inputs V_{fdq}^{s*} and $\iota_{sdq}^{\widehat{s}}$, and the set points $\overline{a_s}$ and $\overline{b_s}$, $b_{s(nom)}$ are used for calculating the estimate of SAPF parameters $\widehat{a_s}$ and $\widehat{b_s}$. These estimates are used for updating the SAPF model and for calculating the gains $\widehat{p2}$, $\widehat{p_1}$, $\widehat{p_0}$ of the system controller and solving the Diophantine equation.

B) Design of the current controllers

For designing the proposed VS-APPC current controllers, the following steps are necessary.

- 1. Step 1. Identify the system impedances Z_s, Z_f in order to calculate the parameters a_s and b_s . The system model is obtained substituting a_s and b_s values.
- 2. Step 2.Choose the current controller bandwidth ω_c and calculate the coefficients
- 3. Step 3.Choose a positive constant a_m . A suitable choice is $a_m > \omega_c$.
- 4. Step 4.Choose parameter \bar{a}_s to be used in the switching law. The \bar{a}_s value determines the \hat{a}_s estimation range. A suitable choice is $\bar{a}_s \approx 2a_s$ where a_s is the value calculated in step 1.

- 5. Step 5. Choose parameters \overline{b}_s and $b_{s(nom)}$ to be used in the switching law. These values determine the estimation range. A suitable choice is and ,where is the value calculated in step 1.
- 6. Step 6. Calculate controller parameters $\widehat{p2}$, $\widehat{p_1}$ and $\widehat{p_0}$ $i_s^{\tilde{r}}$ $i_s^{\tilde{r}}$

Fig 4 Block diagram of the dc-link voltage control loop.

Based on the simulation and in the theoretical studies, it can be observed that the, magnitudes of the switching laws \bar{a}_s and \bar{b}_s determine how fast the VS-APPC controllers converge to their respective references. However, high values result in high amplitudes of control signals $v_{fdq}^{s'*}$, which can address to the nonlinear behavior of the SAPF control system.

DC-Link Voltage Controller

The block diagram of the dc-link voltage control loop. Block $R_v(s)$ refers to the standard PI controller which transfer function is

$$R_{\nu}(s) = \frac{K(1+sT_i)}{sT_i}$$

Where k is the gain and T_i is the integration time constant of the PI controller used in the dc-link voltage regulation. The algorithm of the PI dc-link voltage controller is implemented with an ant wind up scheme. The delay introduced by the current control loop is neglected and its representation on this diagram is omitted. To obtain a smooth current command i_{sd}^e at the output of the dclink voltage regulator, a first-order low-pass filter is introduced in the dc-link voltage measurement, which is represented by the block $G_v(s)$ given by

$$G_{v}(s) = \frac{1}{1 + \tau_{v} s}$$

Where τ_v is low-pass filter time constant used in the dc-link

Voltage measurement the parcel $\tilde{\iota}_s^s$ related to the harmonic compensation is considered as a disturbance to be compensated by the dclink voltage controller. Therefore, the dynamic model of the dc-link together with the low-pass filter can be given by

$$G_0(s) = \frac{1}{Cs(1+s\tau_v)}$$

Thus, if the controller is included in the transfer function before the dc-link voltage open loop is

Source voltage	$E_{s} = 110V(rms), f_{s} = 60$
and frequency	Hz
Impedance	$Z_{s} = (0.2 + s0.0001)\Omega$
Filter Impedance	$Z_{\rm f} = (2 + s0.001)\Omega$
CurrentController	$\omega_{\rm c} = 1080 {\rm Hz}$
Bandwidth	
Current Controller	$A_{\rm m} = 15000$
constant	
Switching Law	$\overline{a_s}$ =2000, $\overline{b_s}$ =2000and
Parameters	$b_{s(nom)} = 1500$
Capacitor	C=2200µF

$$G_{op}(s) = \frac{K(1+sT_i)}{CT_i s^2 (1+s\tau_v)}$$

Table 1.SAPF PARAMETERS

The parameters are used in this paper are based on the above table. These parameters are rms phase voltage, frequency, line and filter impedance and capacitor value.

IV. SIMULINK MODEL

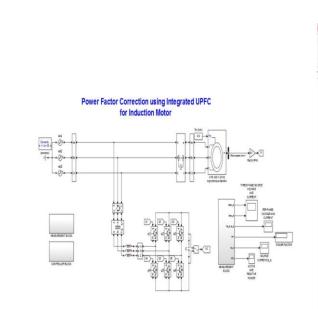


Fig 5 Simulink diagram of power factor correction using integrated UPFC

CAPACITOR VOLTAGE

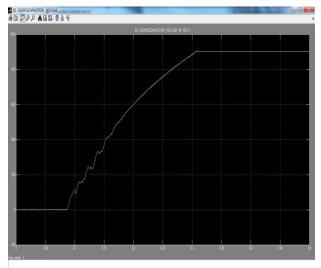


Fig 6 capacitor voltage

Initially the capacitor stores the energy through the converter and it maintains constant DC voltage in capacitor. Whenever the lagging power factor is occurred in the induction motor the converter(SAPF) supplies the reactive power for compensation the above graph shows the capacitor charging and maintaining constant DC voltage that is 900v.

SOURCE CURRENT

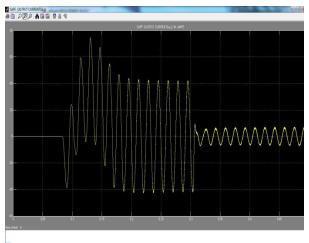


Fig 7 source current

Initially the induction motor draws 5to 6 times of rated current From the supply when the induction motor runs it draws minimum current from the supply and also it charges the capacitor. when the capacitor reaches the reference value it starts to discharge.

VOLTAGE AND CURRENT FOR PER PHASE

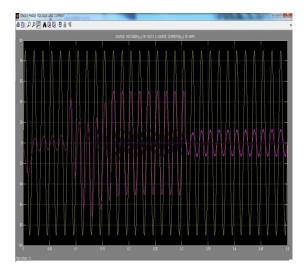


Fig 8 voltage and current for per phase The above graph represents the unity power factor voltage and current waveform.It describes, initially there is a lagging power factor and at the fifth cycle UPFC is switched on,the capacitor starts charging.When the capacitor reaches the reference value, it discharges the reactive power and hence the unity power factor is achieved.

VOLTAGE AND CURRENT FOR THREE PHASE

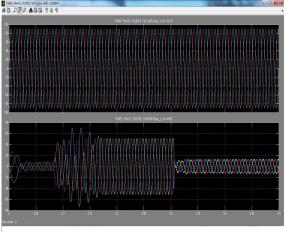


Fig 9 voltage and current for three phase

This waveform represents the voltage and current waveform.

V. CONCLUSION

This paper presented a adaptive control strategy of Integrated UPFC(SAPF)for power factor correction.It provides fast dynamic operation.It reduces penalty paid by the industry.Integrated UPFC is a most advanced technology for power factor improvement.It looks like a shunt active filter but it provides both the operation of shunt and series compensation.Its maintenance cost is low and life time is more.So it is the most advanced than other FACTS devices.

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