VLSI Design Tools & Technology (VDTT) Programme

Dated: 04.05.2012

Sub: Minutes of VDTT PEC Meeting held on 4th May 2012 at 10.30 AM in VDTT office.

Short-listing Criteria in the M. Tech programme of VLSI Design Tools and Technology (JVL).

The Programme Executive Committee (PEC) of the VDTT programme met on 4th May 2012 at 10:30 AM for short listing of M. Tech (VDTT) applications.

The following short listing criteria were decided over and above the minimum eligibility condition as laid out in the prospectus.

i) **Call for interview (Full time with GATE):**

GATE Discipline	Minimum GATE Score	Minimum degree performance	No. of candidates eligible
EC	780	**Minimum degree performance is 60% or 6.75 on 10 Point Scale**	78
EE	780		3
CS	710		20
IN	780		3
IT	710		1
PH	710		1
Others	710		0
		Total	**106**

IIT B.Tech. — CGPA > 8 2 108

ii) **Call for interview for Industry sponsored candidates (Part-time)**

A. Candidates should be an employee of a sponsoring company
B. He/She should have a minimum of 1 year experience
C. He/she should satisfy the minimum criteria of the Institute.

No. of candidates shortlisted 7.

The candidates will be interviewed by the PEC on May 15th (Tuesday) 2012, followed by an interview of the shortlisted candidates with the sponsoring industries on May 16th (Wednesday) 2012.

(Prof. Anshul Kumar)
Coordinator, VDTT Program

✓ **Dean (PGS&R)**

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