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Total No. of Questions : 08] [Total No. of Pages : 02

M.Tech.

ELECTRONICS SYSTEM DESIGN

SUBJECT CODE : EC - 502

Paper ID : [E0562]

[Note : Please fill subject code and paper ID on OMR]

Time : 03 Hours **Maximum Marks : 100**

Instruction to Candidates:

1) Attempt any **Five** questions.
2) **All** questions carry equal marks.

Q1) (a) Design a full subtractor using NOR gates. Extend it to an 8 bit subtractor.

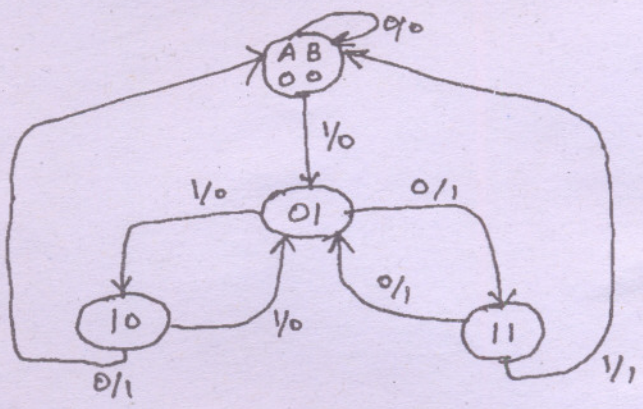
(b) Implement the following function with a multiplier with B, C and D are to be select lines:

$F(A, B, C, D) = \Sigma (0, 1, 3, 4, 8, 9, 15)$.

Q2) (a) Draw circuit diagram of R-S type flip-flop. Design a JK flip-flop using R-S flip-flop. What is clock skew?

(b) What is tri-state logic circuit and how does it help building a tri-state bus system? Discuss the advantages of this logic in reducing hardware in system implementation.

Q3) Design a sequential circuit that will function as prescribed by the state diagram in figure.



Q4) (a) Design a synchronous counter up or down and follow the sequence: 0, 1, 3, 2, 6, 4. Check the design against the lock out conditions.

(b) List the design step for next state decoders.

Q5) (a) What is system controller? Discuss the controller design phase and system documentation.

(b) Explain the MDS diagram construction concepts with flow diagram.

Q6) (a) Discuss the timing and frequency consideration of a digital system.

(b) Explain the steps for design of asynchronous machines.

Q7) (a) What are essential Hazards? How these hazards effects the operation of machine.

(b) Discuss the hazards in circuit developed by MEV method.

Q8) (a) Why grounding and shielding is needed in digital systems.

(b) Discuss the interfacing of digital system with coaxial and fiber optics cable.

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