SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act,1956)

Course & Branch :B.E - EEE
Title of the Paper :Computer Aided Design — Max. Marks :80
Sub. Code :414507 — Time : 3 Hours
Date :04/05/2010 — Session :AN

PART - A (10 x 2 = 20)

Answer ALL the Questions

1. What are the different data types used in MATLAB?
2. Write a simple program for producing an array of whole numbers in MATLAB.
3. State Maximum Power Transfer Theorem.
4. Draw the basic butterfly diagram using DFT.
5. Write the 'h' parameter equation for a two port network.
6. What is a practical Op-Amp and draw its equivalent circuit?
7. Give the features of VHDL.
8. Write the syntax for declaring a file and a signal.
9. What is package in VHDL?
10. How a repetitive structure can be created in VHDL?

PART – B (5 x 12 = 60)

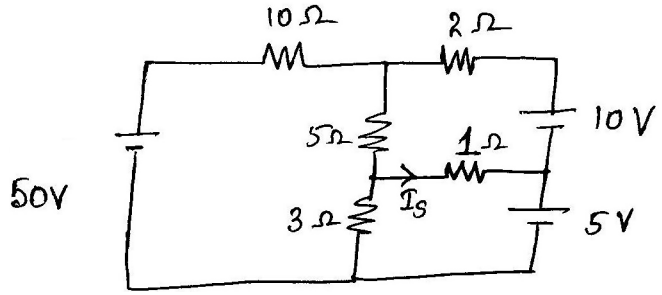
Answer All the Questions

11. Explain cell array, structures, logical and relational operators in MATLAB.

(or)

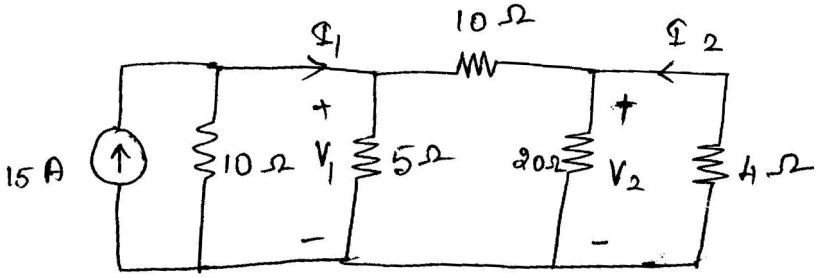
12. Create a simulink model to obtain the response for different types of input for first and second order linear systems and non linear system.

13. Find I_s by mesh analysis and write a MATLAB program to deduce the same for the circuit shown.



(or)

14. Find the four short circuit admittance parameters for the resistive two port network shown.



15. (i) Obtain the V-1 characteristics of Diode and realize the characteristics using MATLAB (ii) Obtain a simulation model for a Full wave rectifier.

(or)

16. Give a transfer function obtain steady state stability of system using MATLAB in frequency response approach and time domain approach. Verify any one method theoretically.

17. Explain the modeling styles of VHDL.

(or)

18. Explain the different data types of VHDL.

19. What is operator overloading and explain the concept the simple example.

(or)

20. Write a VHDL source code for 4 bit adder and 4 bit subtractor.