R.T.M. Nagpur University
Scheme of Examination for
M. Tech. (VLSI) First Semester

Sub. Code	Name of Subject	Teaching Scheme (Clock Hours / Week)				Assessment of Marks of Theory				Assessment of Marks for Practical				Duration of Papers
		L	T	P/D	Total	Paper	CA	Total	Min. For passing	Uni. Exa	CA	Total	Min. For passing	
IFU-01	VLSI Subsystem Design	3	-	2	5	70	30	100	50	25	25	50	25	3
IFU-02	Modeling Digital System-I	3	-	2	5	70	30	100	50	25	25	50	25	3
IFU-03	Switching Theory & Automata	3	1	-	4	70	30	100	50	--	--	--	--	3
IFU-04	Advanced Digital Signal Processing	3	-	2	5	70	30	100	50	25	25	50	25	3
IFU-05	Embedded System-I	3	-	2	5	70	30	100	50	25	25	50	25	3
	Total	15	1	8	24	350	150	500	250	100	100	200	100	Total (T+P) = 700

Second Semester

Sub. Code	Name of Subject	Teaching Scheme (Clock Hours / Week)				Assessment of Marks of Theory				Assessment of Marks for Practical				Duration of Papers
		L	T	P/D	Total	Paper	CA	Total	Min. For passing	Uni. Exa	CA	Total	Min. For passing	
IIFU01	Analog VLSI Design	3	-	2	5	70	30	100	50	25	25	50	25	3
IIFU02	Modeling Digital System-II	3	-	2	5	70	30	100	50	25	25	50	25	3
IIFU03	VLSI Signal Processing	3	1	-	4	70	30	100	50	--	--	--	--	3

IIFU04	Digital Image Processing	3	1	2	6	70	30	100	50	25	25	50	25	3
IIFU05	Elective-I	3	1	-	4	70	30	100	50	--	--	--	--	3
	Total	15	3	6	24	350	150	500	250	75	75	150	75	Total (T+P) = 650

Elective-I **1) Advanced Computer Architecture** **2) Low Power VLSI Design**
3) Embedded System-II

Third Semester

Sub. Code	**Name of Subject**	**Teaching Scheme (Clock Hours / Week)**				**Assessment of Marks of Theory**				**Assessment of Marks for Practical**				**Duration of Papers**
		L	**T**	**P/D**	**Total**	**Paper**	**CA**	**Total**	**Min. For passing**	**Uni. Exa**	**CA**	**Total**	**Min. For passing**	
IIIFU01	VLSI Testing	3	1	-	4	70	30	100	50	--	--	--	--	3
IIIFU02	Elective-II	3	1	-	4	70	30	100	50	--	--	--	--	3
IIIFU03	Seminar	--	--	12	12	--	--	--	--	--	200	200	100	--
	Total	6	2	12	20	140	60	200	100	--	200	200	100	Total (T+P) = 400

Elective-II **1) Mixed Signal Processing** **2) Computer Communication Networks**
3) Computer Graphics

R.T.M. Nagpur University
Scheme of Examination for
M. Tech. (VLSI)
Fourth Semester

Sub. Code	Name of Subject	Teaching Scheme (Clock Hours / Week)				Assessment of Marks of Theory				Assessment of Marks for Practical				Duration of Papers
		L	T	P/D	Total	Paper	CA	Total	Min. For passing	Uni. Exa	CA	Total	Min. For passing	
IVFU01	Thesis / Dissertation (Viva-Voce)	--	--	12	12	--	--	--	--	400	-	400	200	--

Note: a) Minimum Passing Marks is 50% in all Subjects.

b) Dissertation Marks will be given based on Internal Seminar & Viva-Voce.

Syllabus for M.Tech.(VLSI)

First Semester Syllabus

1FUV01 VLSI SUBSYSTEM DESIGN

Section A

Material Model Electrical Properties, Junction Diode. MOS transistor Operation Modes Threshold Voltage: Metal and Polysilicon Trapped Charge Implants Strong Inversion: Charge Modeling Constant Vt model: NMOS/PMOS transistors. I/V characteristics, Sign Conventions parasitic Bipolar Transistors CMOS Latch-up Analysis (D.C. and transient), Device capacitance and Charge Storage in MOS NMOS/CMOS circuit analysis, Small signal amplifier model Miller Effect. Layout / Fabrication, Diffusion / Implants / Wires, NMOS / CMOS Processes SCMOS Design Rules – special derivation self-aligned processes Resistor / Capacitor Layout, Logic Level Design, Cube Decomposition, Realization of Duals for CMOS Euler path layout, Topological Considerations. Don't Cares and Redundancy, layout Parasitic Reduction.

Section B

MOS Logic Families: Propagation Delay for CMOS/NMOS/PNMOS, Layout Capacitance / Resistance. Estimation; Gain effects; MOS Performance Estimation, Buffers/Capacitive Loading, Power Dissipation : Transient Optimization, Sidewall/2-d and 3-d effects: Cross-talk Fringing, Ball-park numbers for process Estimation Scaling CMOS Design Optimization: High-Speed Logic Strategies. Interconnection. Distributed R/C cross/talk, Noise, Clocking Strategies, Sub-System Design and Partitioning Dynamic Logic, Dynamic Circuits, Stored Charge and timing. Domino Logic, Switched Capacitor and Charge Flow circuits, pass-Transistor logic (CPL).
Data-Path and Memory Circuits : Static/Dynamic memories, Ancillary memory Analog Circuits.

Books:

1. Weste, "principles of CMOS VLSI Design (2nd edition)"
2. Dougles A. Pucknell and kamran Eshraghian, "Basic VLSI Systems and Circuits, Prentice Hall of India Pvt. Ltd. 1993.
3. Wayne Wolf, "Modern VLSI Design, 2nd Edition". Prentice Hall 1998.

IFUV02 MODELLING OF DIGITAL SYSTEM – 1

Section A

Programming Technologies – ROMs & EPROMs PLA . PAL gate Arrays Programmable gate arrays and applications, Antifuse FPGA, Synthesis methods for FPGA.
Hardware Description Language. Design entities, architecture Bodies, Block Statements, processes data types. Operators . Classes of Objects, Attributes, Functions and Procedures, Packages Control Statements.
Behaviour modeling.- Process Statement, Assertion Statement, Sequential wait Statement, Formatted ASCII I/O Operations Structural Modeling ; parts Library wiring of Primitives. Wiring of Iterative networks. Modeling a test bench.

Section B

Chip Level Modeling : Chip level modeling structures modeling delay, process model graphs, Functionally partitioned models, Timing Assertion, Setup & Hold time for clocked devices, Design rule checks
System Modeling : Modeling system interconnection, general model for signal interconnection, Multiplexing of signals. Multiple valued logic. Processor model. RAM model. UART model, Parallel I/O Ports, Interrupt controller
Simulation with the physical model, simulation, writing test bench, converting real and interconnection, Multiplexing of signals. Multiple valued logic. Processor model. RAM model. UART model, Parallel I/O Ports, Interrupt controller.
Simulation with the physical model, simulation, writing test bench, converting real and integer to time. Dumping results into text file, reading vectors from text file, test bench example.

Books:

1. Navabi Z, "VHDL Analysis and Modeling of Digital Systems". Prentice Hall, 1993.
2. J. Bhasker "VHDL Primer", Pearson Education, 2000.

3. Armstrong & Grey. “VHDL Design. Representation and Synthesis”, PHPTR, 2000.
4. James R. Armstrong, “Chip Level Modeling with VHDL”, Prentice hall, 1989.

IFUV03 SWITCHING THEORY AND AUTOMATA

Section A

Shannon’s expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT/INCLUSION/AOI/Driver/ Buffer gates, gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.
Linear seperability. Unateness, Physical implementation, Dual comparability, Reduced functions, various theorems In threshold logic, Synthesis of single gate and multigate threshold Network. Elementary symmetric functions, partially symmetric and totally symmetric functions, Mc-Cluskey decomposition method. Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.
Mealy Moore State Tables and Systems. State tables from Word Descriptions, Special Methods for Multi Condition Sequence Detectors, Analysis of Finite State Machines.

Section B

Minimization of sequential Machines, State Equivalence and State Table Reduction, machine Equivalence, incompletely Specified machines, Special Heuristic State Table Reduction.
Asynchronous Sequential Machines : Fundamental Mode Systems, pulse Mode Systems, Pulse In, Pulse Out (Mealy), Pulse In, level Signal Out (Moore), Hazards, Structure of and Dependencies in Sequential Machines.
State Assignment using partitions of States, Reduction of State variable and Output Dependencies. Input Independence and Autonomous Clocks, Information Flow in Sequential machines, partition pairs, Mm Pairs, Decomposition into Separate Machines
State Identification and Fault Detection Experiments.
Homing trees and Experiments. Synchronizing Trees and Experiments, Distinguishing Trees and Experiments, Machine Identification, Diagnosable Machines Memory Definiteness and Information Loss less ness.
Memory Span, Input –Output Memory, Output Memory, Input Memory, Information Loss less Machines, Synchronaizable and Uniquely Decipherable Codes.
Finite State Recognizers : Deterministic Recognizers, Transition graphs, Deterministic Graphs from Non deterministic Graphs, Regular Expressions, Regular Sets from Transition graphs

Books:

1. Kohavi, “Switching and Finite Automata Theory”. (2nd edition), McGraw Hill. 1986
2. William I Flecher, “Engineering approach to Digital Design”, Prentice Hall, 1996

IFUV04 ADVANCED DIGITAL SIGNAL PROCESSING

Section A

Multirate Signal processing : Introduction Sampling and signal Reconstruction sampling rate conversion, Decimation by an integer factor, interpolation by an integer factor, Sampling rate conversion by rational factor, Sampling rate converter as a time variant system, practical structures for decimators and interpolators, Direct from and Polyphase FIR structures, with time varying coefficients.
Multirate FIR Filter Design. Design of FIR filters for sampling rate conversion, Multistage implementation of sampling rate conversion, Applications of Interpolation and decimation in signal processing operations low pass and band pass filters, filter bank implementation, sub band processing, Decimated filter banks. Two channel filter banks, QMF filter banks, perfect reconstruction filter banks tree structure filter banks octave, band filter banks, uniform DFT filter banks.

Section B

Power Spectral Estimation : Estimation of spectra from finite duration observations of a signal, the periodogram, use of DFT in power spectral estimation, Non periodic methods for power spectral estimation. Barlett, Wech & Blackman, Tukey methods, comparison of performance of Non periodic power spectral estimation methods.
Parametric Methods of Power Spectral Estimation: Parametric Methods of Power Spectral Estimation, Relationship between auto correlation and model parameters, Auto-Regressive process and linear prediction, Yule-Walker. Burg & unconstrained least square

methods, Sequential estimation, Moving average and ARMA models, minimum variance method, Pizarenko's harmonic Decomposition method, MUSIC method.

Books:

1. Oppenhiem and Sohaffer, "Discrete time signal processing", Prentice hall
2. J.G. Proakis, D.G. Manolakis, "Digital Signal Processing principales", Prentice Hall
3. Rabinar and Gold, "Theory and Applications of Digital Signal processing", prentice Hall
4. Rabinar and Schaffer, "Digital Processing of Speech Signals", Prentice Hall
5. Orfanadis S. 'Introduction to Digital Signal Processing", Prentice Hall, 1989
6. Orfanadis S. "Optimum Signal Processing', Prentice Hall, 1990

IFUV05 EMBEDDED SYSTEM – I

Section A

The 8051 micro controller, Assembly language programming Jump, Loop and Call instructions, I/O port programming, Addressing modes, Arithmetic Instructions and programs Logic Instructions and programs, Single bit Instructions.

Section B

Timers and counters Serial Communications, Interrupts programming Interfacing LCD, ADC and sensors, Interfacing stepper motors, keyboards and DAC'S. Interfacing external memory and 8255

Books:

1. Kenneth Ayala "The 8051 Micro controller Architecture, programming and Application " Penram Publication.
2. M.A. Mazizi & J.G. Mazidi, The 8051 Micro controller:, Pearson Education 2000.

Second Semester M. Tech (VLSI) Full Time

IIFUV01 ANALOG VLSI DESIGN

Section A

Device modeling and simulation Modeling, MOS Models Diode model, Bipolar modes BSIM Spice models, Circuit simulations using Spice.
Basic Building Blocks: Switches. Current sources and sinks. Current mirrors. Voltage and current references. Amplifiers: MOS Inverting amplifier, Cascade amplifiers. Feedback amplifiers Differential amplifiers. Frequency response, noise performance in Diff amplifiers, Output amplifiers. CMOS Two stage OPAMP Design, Cascade OPAMPs, Simulation and Measurement of OPAMPs, Comparators.

Section B

Analog signal processing, CMOS Digital to analog converters, Scaling and serial, cyclic. Analog to digital converters Serial, SAR, Parallel, Pipelined, sigma-delta converters, mixed signal Layout issues.
Continuous time filters, Switched capacitor filters, Modulator and multipliers, PLL.

Books:

1. R.L. Geiger, P.E. Allen, "VLSI Design techniques for Analog and digital Circuits", McGraw Hill
2. J. Baker, D.E. Boyce. "CMOS Circuit Design, Layout and simulation", IEEE press.

IIFUV02 MODELLING OF DIGITAL SYSTEM-II

Section A

Introduction to Verilog, Module, delays, descriptions, Language elements, Expressions, Gate-level modeling User defined primitives, Dataflow modeling, Behavious modeling, Structural modeling, Tasks and functions.
Programmable Logic Devices: Basis concept, Programming technologies, Programmable logic elements, programmable logic array, programmable array logic, structure of standard PLD's, complex PLDs CPLD. Altera Max 7000 series. AMD Match 4 structure.

Section B

System Design with PLD'S : Design of combinational and sequential circuits using PLD's, Programming PAL devices, using PALASM, Design of state machines using algorithmic state machines ASM chart as a design tool
Introduction to FPGA: types of FPGA, Xilinx XC3000 series, Logic Cell Array (LCA), Configurable Logic Blocks (CLB), Input/Output Blocks (I/OB), Programmable interconnection Points (PIP), introduction to ACT 2 family and Xilinx4000 families, Design example.

Books:

1. Palmer J.E. Perlman D.E., "Introduction to digital System". McGraw Hill
2. Nelson, Nagale, Carroil, Irwin, "Digital Logic Circuit Analysis and Design", Prentice Hall
3. John Oldfield, Richard Dorf. "Field Programmable Gate Array: Re configurable logic for rapid prototyping and implementation of Digiatl System", John Wiley
4. "Programmable Logic Devices Data book and Design Guide". National Semiconductors
5. Pradnan D.K., "Fault-Tolerant-Theory and Techniques. Vol and II, Prentice Hall
6. J.Bhasker "A Verilog HDL Prime 2e". BS Publications. 2001
7. Navabi. "Verilog Digital system Design" McGraw Hill, 1999
8. Stuart Sutherland, "Verilog 2001, Kluwer. 2002
9. Surherland, "The Verilog PLI Handbook" Kluwer. 1999

IIFUV03 VLSI SIGNAL PROCESSING

Section A

Pipeling and Parallel Processing: introduction, pipeling of FIR Digital filters Parallel processing. Pipelining and parallel processing for low power.
Retiming: Introduction, Definition and properties, Solving system of inequalities, retiming techniques.
Ufolding Introduction An algorithmsfor unfolding, Properties of unfolding, Critical path, unfolding and retiming Application of unfolding.
Folding: Introduction Folding Transformation, Register Minimization Techniques, Register minimization in folded architectures Folding if Multirate systems.

Section B

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR systolic Arrays, Selection of scheduling vector, Matrix Multiplication and 2D systolic array Design, Systolic design for space representations containing Delays.
Fast Convolution: Introduction, Cook, Toom algorithm, Winogard algorithm, iterated convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Books:

1. Keshab K. Parhi. "VLSI Digital Signal Processing Systems" Wiley-Inter Sciences. 1999
2. Mohammed Ismail, Terri, Fiez, "Analog VLSI signal and information processing 1994. McGraw Hill.
3. Keshab. Parthi, VLSI Digital signal processing system Design and implementation Wiley-Inter science, 1999.
4. kung. S.Y., H.J. While house T.Kailath "VLSI and Modern singal processing, prentic hall. 1985.
5. Jose E. France, Yannis Tsividls "Design of Analog Digital VLSI circuits for telecommunications and signal processing' prentice Hall, 19994.

IIFUV04 DIGITAL IMAGE PROCESSING

Section A

Digital Image fundamentals: Elements of Digital Image system-structure of the human eyes Image formation in the eye and contrast sensitivity-sampling and Quantization of an Image-basic relationship between pixels-imaging geometry photographic film.
Image Transforms: Need for image transform Walsh transform hotel ling transform.
Image Enhancement: spatial domain method frequency domain method-histogram modification technique neighborhood averaging median filtering low pass filtering averaging of multiple images-Image Restoration: Degradation model for continuous functions-discrete formulation Digitalization of circulating and block-circulate matrices-effect of diogonalization unconstrained restorations-inverses filtering-wiener filter constrained-least square restoration.

Section B

Image Compression: Coding and inter pixel redundancies-fidelity-criteria-image compression modes-elements of information theory-transform coding.
Image Segmentation and representation ,detection of discontinuities-point, line and edge detections-gradient operators-combined detection-Thresholding -Representation. Scheme: chain codes-polygon approximation-boundary descriptors: simple descriptors-shape numbers Fourier descriptors' introduction to recognition , interpretation.

Books:

1. Rafel C. Gonzalez and Richard E. Woods "Digital image processing", Addition-wisely
2. Anil K.Jain "Fundamental of digital image processing" prentice Hall 1995.
3. Rosenfeld A.C. Kak, Digital picture processing-academic press inc 1976.
4. Hall E.L. computer image processing and recognition academic press inc 1979.
1. Huang T.S. "Picture processing and digital filtering" Springer Verlag Berlin Heidelberg.

IIFUV05 ELECTIVE –I

IIFUV05(A) ADVANCED COMPUTER ARCHITECTURE

Section A

Parallel computer model – the state of computing. Multiprocessor and Multicomputers and Multi vector and SIMD computers, PRAM and VLSI modes, Architectural development tracks Program and network properties. Conditions of parallelism, Program partitioning and scheduling, Program flow mechanisms. System interconnect architectures. Principles of scalable performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches. Processor and memory hierarchy advanced processor technology, super scalar and vector processors, memory hierarchy technology virtual memory technology, bus cache and shard memory – back plane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency modes.

Section B

Parallel and scalable architectures Multiprocessor and Multi computers, Multi vector and SIMD computers, Scalable, Multithreaded and data flow architectures.
Parallel models, Languages and compilers, Parallel program development and environments, IM INIX MACH and OSF/1 for parallel computers.

Books:

1) Kai Hwang , "Advanced Computer Architecture", McGraw Hill international, 1993.
2) William Stallings, "Computer Organization and Architecture" Macmillan, 1990.
3) M.J. Quinn, "Designing Efficient Algorithms for Parallel Computers"

IIFUV05(B) **LOW POWER VLSI DESIGN**

Section A

Introduction – Simulation – Power Analysis-Probabilistic Power Analysis.
Circuit – Logic – Special Techniques – Architecture and Systems Advanced Techniques – Low Power COMOS VLSI Design – Physics of Power Dissipation in CMOS FET Devices.

Section B

Power Estimation – Synthesis for Low Power – Design and Test of Low Voltage – CMOS Circuits. Low Power Static RAM Architectures-Low Energy Computing Using Energy Recovency Techniques VLSI-Software Design for Low Power.

Books:

1) Gary Yeap "Practical Low Power Digital VLSI Design", 1997.
2) Kaushik Roy, Sharat Prasad, "Low Power CMOS-VLSI Circuit Design", 2000

IIFUV05 (C) **EMBEDDED SYSTEM – II**

Section A

Introduction to Intellectual Property (IP) Circuits or Cores, Core examples. Peripherals interfacing with IP Cores. Core based SOC design. Concept and Fundamentals of RTOS essential features, ROS Kernel Function, RTOS examples Lynox, QNX, Neutrino, VRTX, Vx Works.

Section B

OS services. Operating Modes. Threads, Context Switching overheads, Scalability, Embedding with application code.Task Scheduling, Interrupt handling, Inter task communication. Comparison and application of various RTOS.

Books:

1) Michael Barr, "Programming Embedded System in C and C++", O Reilly & Associates Inc.
2) Steve Heath, "Embedded System Design" Butterworth Helnemann.
3) Jean J. Labrosse, "Micro C/OS II The Real Time Kernel"
4) Richard H. Barnett, Sarah A Cox Larry D, "Embedded C Programming and Atrnel AVR"

Syllabus of Examination for
Third Semester M. Tech (VLSI) Full Time

IIIFUVO1 **VLSI TESTING**

Section A

Exponential nature of the testing problem, Fault models, Stuck-at-faults, Test generation for combinational circuits,
The D algorithm. POCEM, FAN. Learning Algorithms, Fault converge, Fault simulation and fault grading,
Testability measures, Test generation, algorithms for sequential circuits, Scan and practical scan design, BIST and other design for testability techniques.

Section B

Boundary scan and the IFEE 11491 testability standard CMOS opens testing, performance and delay testing, IDDQ and other current based tests.

Synthesis for testability, Memory testing, Mixed signal testing.
Test. Effectiveness: coverage, yield and defect level, System-level test and diagnosis, MCM and core based testing.

Books:

1) Miroh Abramovici Melvin Breuer and Arthur Fridman, "Digital Systems Testing and Testable Design", IEEE Press, 1990.
2) Pradhan D.K. "Fault-Tolerant Computing – Thoty and Techniques", Vol I & II, Prentice Hall, 1986

IIIFUV02 ELECTIVE – II

IIIFUV02(A) MIXED SIGNAL PROCESSING

II. Section A

Introduction: Introduction modifying basis analog concept. Analog circuit analysis. Network independent, dependent data sampled analog system loading effects.
Analog and Mixed Signal Extensions To VHDL: Introduction, language design objectives, theory of differential algebraic equation the 1076.1. language tolerance groups, conservative system, time and simulation cycle A/D and D/A interaction, quiescent point, frequency domain modeling and examples.

Section B

Analog Extensions To Verilog: Introduction Equation construction solution, waveform filter functions, simulator, control analysis, multi-disciplinary model.
Behavioral Generic model of operational amplifiers: Introduction, description of generic Opamp model structure, configuration functional specification, Auxiliary block conflict resolution, application examples.
Non-Linear state space averaged modeling of 3-state – digital phase-frequency detector.
Introduction model, resell table integrator AC analysis, sample application.

Books:

1) Alain Vachoux Jean-Michel Berge OZ Levia "Analog and mixed signal hardware description languages (current issues in Electronic Modeiling V.10) Kluwer Academic Publisher 1997.

IIIFUV02 (A) COMPUTER COMMUNICATION NETWORKS

Section A

Introduction: Goals uses Network components, switching technologies network topologies transmission media, protocol, routing and flow, WAN, MAN, LAN, ARPANET.
Queuing Theory: Importance Queuing modes, Poisson statistics, little theorem, M/M/I and models, applications to computer networks
Data Communication Concepts: Asynchronous and synchronous transmission, error correction and detection, CRC liner arid and block codes, transmission protocols : STOP, START, BSC, SDLC and HDLC. Retransmission technique : Base band interface standards modems. Forward error detection, Automatic repeat request, Acknowledgement mechanism.
LOCAL AREA NETWORKS: Component – topologies access technique, polling ALOHA, CSMA CD token spring token passing and IEEE 802 standards. Transmission media, performance.
Comparison, applications, implementation procedure MAN and its IEEE standards switched and fast Ethernet. FDDI, and SONET.

Section B

Network protocols : Concept, functions, goals of layered Architecture, OSI reference model, X-25, Frame relaying. TCP/IP architecture and operations The IP layers and function naming addressing and routing in an internet, major application layers user services: E-mail, WWWW, FTP, TEONET.
Backbone network/internetworking:- Need for concepts devices: Hubs, switches, bridges, routers, grouters, gateways & repeaters, choice for implementation.
Broadband networks: Telecommunication networks, evolution ISDN: structures limitation –ISDN(B) services transfer modes asynchronous transfer mode(ATM) characteristics, protocols reference model, ATM cell format, ATM services and quality of services, classes of traffic and traffic management concept, introduction to VAST networks.

Books:

1. Black U., "Computer networks, protocols standards and interfaces", PHI 2nd Edition, 1997. Keiser. G.E. "Local area networks". McGrqw hill. 1989.
2. Croaches P. "Communications and network-a handbook for the first time user", 2nd edition, East-West press. 1995.
3. Taneum baum S.A. "Computer networks". Third edition PHI,. 1996.
4. Comar. D.E., "Internetworking with TCP IP-Vol-1 : principle and architecture", PHI, 1996
5. Stallings W. "High-speed Networks TCP IP and ATM design principles", Prentice Hall-inc, 1998.
6. Stalling. W. "ISDN and broadband ISDN with farm relay and ATM, 3rd edition", 1998.

IIIFUV02(C) COMPUTER GRAPHICS

Section A

Introduction to computer graphics, Raster refresh graphics displays, cathode ray tube basics, color CRT Raster Scan Basics, video-basics.
Line drawing algorithms, Bresharm's algorithms, DDA, Breasharm's Circle generation algorithm. Run length encoding cell coding Real time scan conversion Quad Trees.

Section B

Polygon filling methods grouping techniques for lines polygons, Three dimensional transformation. Hidden lines & surface Rendering, Curve generation, Brnzier and B-spine curves.
Architecture of VGA, ROMBIOS. Text operation. Graphics Modes controller, introduction to GKS Practical will be based on C++& Windows.

Books:

1) David F. Rogers, "Procedural Elements for Computer Graphics", McGraw Hill
2) David F. Rogers. "Mathematical Elements for Computer Graphics".
3) William M. Newman & Robert F. Speroyli, "principles of interactive Computer Graphic.