2006

ANALYSIS, DESIGN, AND LABORATORY EVALUATION OF A DISTRIBUTED UNIFIED POWER FLOW CONTROLLER CONCEPT

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ABSTRACT OF DISSERTATION

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A dissertation submitted in partial fulfillment of the
requirements for the degree of Doctor of Philosophy in the
College of Engineering
at the University of Kentucky

By

Qiang Li
Lexington, Kentucky
Director: Dr. Jimmie J. Cathey, Professor of Electrical engineering
Lexington, Kentucky
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ANALYSIS, DESIGN, AND LABORATORY EVALUATION OF A DISTRIBUTED UNIFIED POWER FLOW CONTROLLER CONCEPT

The Unified power Flow Controller (UPFC) is an effective equipment in controlling the power flow in the new deregulated electricity markets. The UPFC realizes its function by changing part or all of the parameters affecting flowing of the power in a transmission line. These parameters include the bus voltages, the line impedance and the power angle. The UPFC is by far the most advanced and versatile device in the Flexible AC Transmission System (FACTS) device family. The UPFC can control the transmitted real and reactive power flows independently, at the sending and receiving end of the transmission line, while maintaining proper voltage profile of the transmission line. Normally, the UPFC was customized for particular application with bulky concentrated capacity. However, several problems, reliability, cost, and footprint requirement, hinder its widespread acceptance by the electric utilities.

To overcome the drawbacks of the conventional UPFC, this dissertation proposed and studied a new UPFC technology that addresses these impediments. This novel technology is called the Distributed UPFC (DUPFC). Similar to the personal computer versus the main frame, the concept of the DUPFC intends to utilize the economics of scale to decrease the cost, complexity, and to improve the reliability of the UPFC system.

The proposed DUPFC is based on single-phase system, considering the high voltage insulation, the manufacturing cost, and the installation requirement. The proposed DUPFC unit will be designed to mount on the transmission tower, sharing the footprint of the existing transmission tower. A hierarchy control of the DUPFC system is proposed, which includes local unit control and a central control unit. The central control unit calculates series voltage and shunt real/reactive power commands for every DUPFC unit. The local DUPFC unit accepts commands from the central control unit, monitors local voltage at the connection point, and realizes its control commands. The functions and performance of the DUPFC system is verified with simulation and experiments.

KEYWORDS: Flexible AC Transmission System (FACTS), Unified Power Flow Controller, Power Regulation, Power Converter, Real Time Control

Qiang Li

December 10, 2006

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To the democracy development of China.

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CHAPTER 1 INTRODUCTION

1.1 Background

The power stations, the transmission lines, and the distribution substations compose the power system, which produce and transport electric energy into every family and business. The rapid growth in electric energy demand and the demand for low-cost energy has historically led to remotely located generation plants. The situation has made it necessary to use transmission lines to transport electric energy to the end consumers. To increase the system reliability, redundant lines exists in power transmission system. Inherent in the electric energy demand is the demand variation and non-storability. The demand characteristics require that the power flow on a particular transmission line to be controllable in a multi-path transmission network.

From as early as in 1897, when Samuel Insull, then president of the industry's National Electric Light Association and a persistent advocate of regulation, succeeded in lobbying on regulation of the electricity utility industry, until the last decade of 20th century, electric power systems have been a natural regional monopoly. The industry was state-regulated and vertically integrated. In each franchised area, one company operated the generation, transmission, and distribution. However, in 1990s, electricity industry saw a trend to deregulation and competition. The Federal Energy Regulatory Commission (FERC) enacted the Energy policy Act of 1992. In March 1995, FERC ruled in favor of open-access transmission. The acts opened the wholesale electricity trade with the expectation to make the industry more efficient, to lower the electricity cost, and to improve the industry services. The acts require an open access transmission services, which implicates that power generation and transmission must be functionally unbundled. The unbundling of power transmission from power generation will possibly make the power generation companies have less incentive to invest on auxiliary equipment. Expensive equipment, like excitation control systems and

system stabilizers, used to control reactive power generation and absorption, to stabilize the power system, and to aid power transmission become the financial burden on the transmission systems [1-3].

With increasing power demand across the country and delayed construction of both new power stations and transmission lines, the burden of the power transmission system has become more and more serious. From 1986 to 2002, U.S. electricity demand grew by 26%. At the same time, the U.S. electricity generating capacity increased by 22%. However, the transmission capacity grew very little in the country with the interconnection of new power plants. As a result, the average transmission capacity per consumer declined in the past decade, and is expected to continue decreasing in the coming decade [4].

The above-mentioned factors lead to the fact that the power transmission companies must make the best use of their transmission capacity and ensure that transmission losses are reduced to their lowest values. Thus, it is obvious that the transmission network needs to be more flexible. Fortunately, the advancement of the power electronics technology partially alleviates this problem by providing means and techniques to more efficiently utilize the existing infrastructure. The advancement includes the development of higher voltage level power semiconductors, modern control methods, suitable digital processing theory and the increased capability of microprocessors, and other related engineering techniques. The Flexible Alternating Current Transmission Systems (FACTS) are a group of power electronics devices specially designed to address the need to enhance the use and performance of the electric utility grid. A FACTS device is described by IEEE as “a power electronic based system and other static equipment that provide control of one or more AC transmission system parameters to enhance controllability and increase power transfer capability.” [5] FACTS devices have several purposes:

(1) To increase the capacity of the existing power transmission system.

(2) To control the power flow in desired transmission route.

(3) To provide dynamic stabilization enhancement for the transmission system.
(4) To provide system optimization control, when a large number of FACTS devices are installed on the power system.

This dissertation mainly focuses on the first two objectives of the FACTS devices. It also gives some consideration to the fourth objective. Unless specified, all circuit analysis is based on balanced three-phase system.

1.2 Active and Reactive Power control

After more than 100 years development, the power transmission system has evolved into a very complex network, connecting all generation centers and major buses. Electric power can typically flow over more than one path from a power generation center to an electric load. Figure 1.1 shows an IEEE 14 bus test system. The test system illustrates a section of American Electric Power System (in the Midwestern US) as of February, 1962.[1] It can be seen that a typical transmission system demonstrates a multi-path pattern between any generator and electric load. The goal of the deregulated power system is to deliver required power from any generation center to any customer via the geographically distributed transmission system in a large area.

[1] http://www.ee.washington.edu/research/pstca/pf14/pg_tca14bus.htm

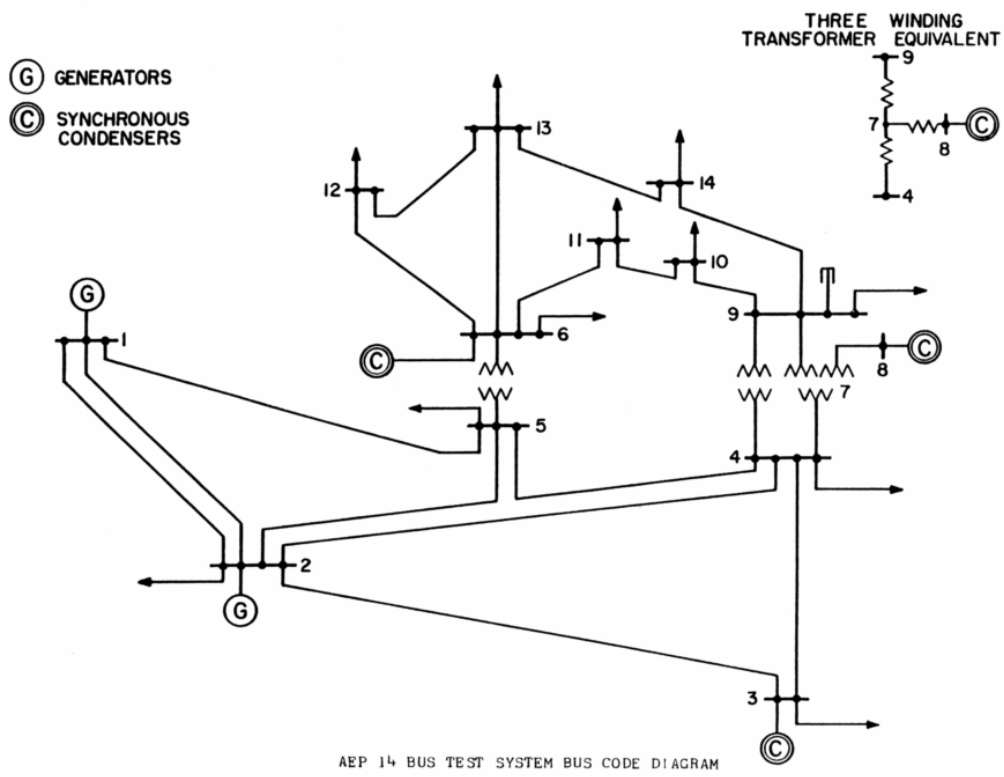


Figure 1.1 IEEE 14 bus test system

Despite the complexity of the modern transmission system, the basic theory of power transmission can be illustrated as a two machine model as in Figure 1.2. The two bus AC system has a sending-end bus with the voltage $\overline{Vs} = Vs\angle 0°$ (RMS value), a receiving-end bus with the voltage $\overline{Vr} = Vr\angle -\delta°$ (RMS value), and the line reactance X. This simple model can also represent two independent AC systems, which are connected for power transfer. An AC transmission line has distributed circuit parameters: series resistance and inductance, and shunt capacitance and conductance. In practice, transmission line inductance and capacitance are the dominant parameters in determining the power transmission. In short transmission line (less than 100 miles), the shunt capacitance is neglected. In medium and long transmission line model, nominal-T model and nominal-π model are used. However, in those cases, the effect of the shunt capacitance is the improvement of the transmittable power. Considering the major objectives of the FACTS devices, plus for simplicity consideration, the lumped

inductance equivalent circuit model is a normal practice in analyzing FACTS application in transmission system.

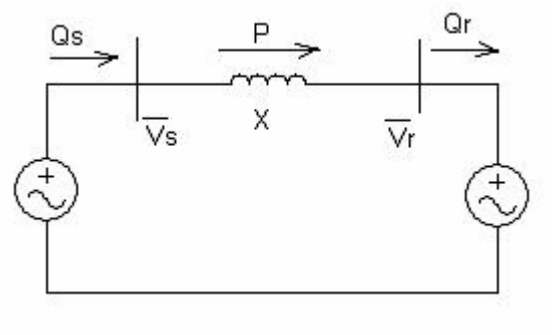


Figure 1.2 Simple two-bus AC power system

It is easy to obtain, by AC circuit analysis, that the transmitted active power from the sending end to the receiving end is [6]:

$$P = \frac{VsVr}{X}\sin\delta$$

The sending end reactive power is:

$$Qs = \frac{1}{X}(Vs^2 - VsVr\cos\delta)$$

The receiving end reactive power is:

$$Qr = \frac{1}{X}(VsVr\cos\delta - Vr^2)$$

Assume magnitude of both of the voltages are controlled to be V. Then, the active power transferred from the sending end to the receiving end is:

$$P = \frac{V^2}{X}\sin\delta \qquad (1)$$

And, the transferred reactive power is:

$$Q = Qs = -Qr = \frac{V^2}{X}(1-\cos\delta) \qquad (2)$$

From the equation (1) and (2), we can see that power transmission in the simple two machine model is determined by the magnitude of the sending and

receiving end voltages, the phase angle difference between the two voltages, and the transmission line impedance. More specifically, the real power transfer primarily depends on the phase angle difference δ, which is called the power angle. The real power transfer also depends on the voltage magnitude of the two voltages. The reactive power flows from the high voltage to the lower voltage bus. Figure 1.3 depicts the relationship between the real and reactive power, and the power angle. It can also be concluded that by adjusting the voltage magnitudes, the power angle, and the line inductance, the active and reactive power flow along the transmission line can be controlled accordingly.

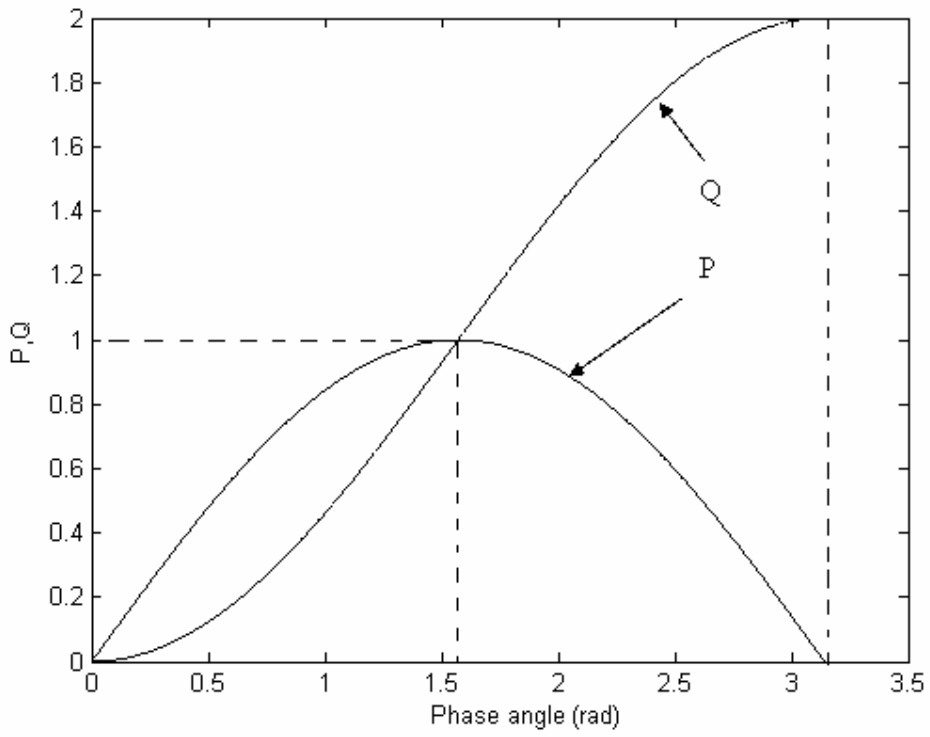


Figure 1.3 Power transmission vs. power angle

Until recently, control of the active and reactive power on a transmission line was realized by adjustment of the bus voltages of the generation plants, transformer taps, and transmission line impedances. Much of the function of controllability was realized at the generation stations. Those control include the automatic generation control (AGC), excitation control, transformer tap-changer

control, and the phase shifting transformer control. The AGC system, as in Figure 1.4, controls the shaft torque on the generator, thus the rotation speed of the generator. So, the frequency and active power of the generator output can be controlled [7, 8]. The excitation control system, as in Figure 1.5, adjusts the field excitation of a synchronous generator to control the output voltage magnitude. This is an efficient way to control the reactive power on the transmission line [9, 10]. The transformer tap-changer control system adjusts the transformer output voltage in a range to vary the voltage, thus the reactive power in the transmission system [11]. The phase-shifting transformer changes the phase angle of the voltage. It mainly controls the active power flow in the transmission line [12].

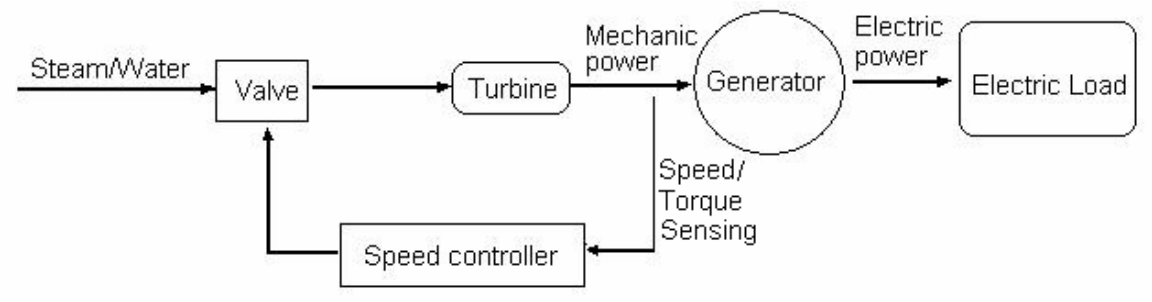


Figure 1.4 Automatic generation control system

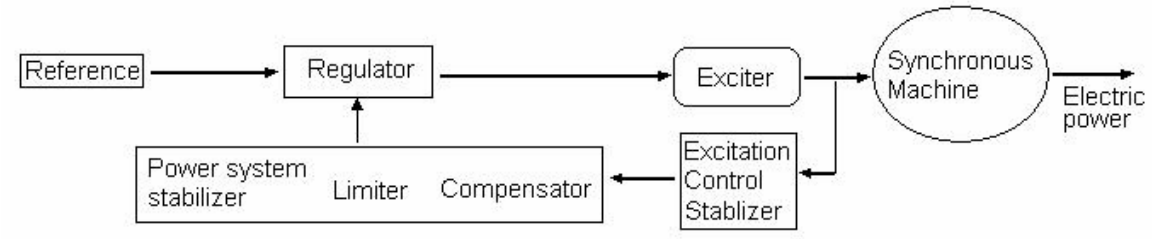


Figure 1.5 Excitation control system

1.3 FACTS devices in power transmission systems

Inspired by the way the traditional electro-mechanical system control the power transmission, researchers and engineers came up with the power-electronics based FACTS controllers. Compared with the traditional

electro-mechanical system control, FACTS devices have the following advantages [13]:

- The main advantage of FACTS over simple mechanical devices is their near-instantaneous response to changes in the system voltage.
- Lower maintenance requirements without rotary parts.
- Lower losses compared with mechanical/rotary compensators.
- High reliability.
- Possibility of individual phase control.

The FACTS devices form a large group of power electronic based converters designated to enhance controllability and increase power transfer capacity. These devices can be classified into two groups: thyristor based FACTS devices and converter based FACTS devices.

Thyristor based FACTS devices use conventional thyristor in building the circuit. If the FACTS devices use thyristors without self-turn-off ability, the device is called a thyristor controlled device. If the thyristor in the FACTS device can be turned off by applying appropriate gate voltage, the device is called a thyristor switched device. According to which circuit parameter the device changes, the thyristor controlled FACTS devices can be categorized to the following groups:
(1) **Static VAR compensator (SVC)**. This group of devices is shunt devices, as shown in Figure 1.6. They generate or absorb reactive power to maintain or control specific parameters of the electric power system. Typically, SVC is used to control the bus voltage. SVC includes Thyristor Controlled Reactor (TCR), Thyristor Switched Reactor (TSR), and Thyristor Switched Capacitor (TSC). [14-22]

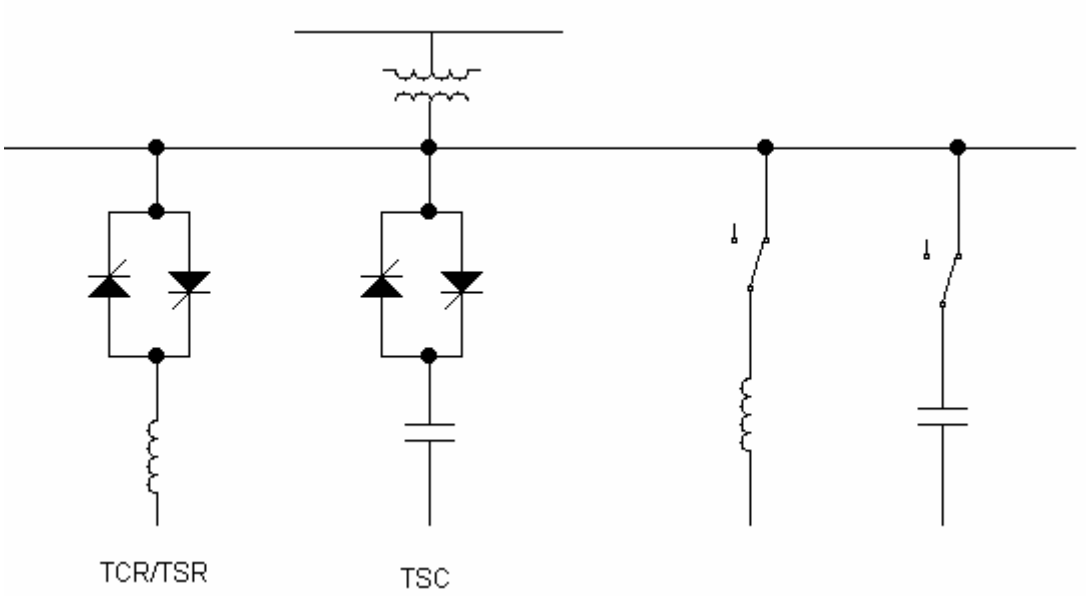


Figure 1.6 Thyristor controlled static VAR compensator

(2) **Thyristor controlled/switched series capacitor/reactor (TCSC/TSSC/TCSR/TSSR).** As shown in Figure 1.7, thyristor controlled/switched series devices are put into circuit in series with the transmission line. This group of devices controls the transmission inductance in a stepwise mode (thyristor controlled devices) or smooth mode (thyristor switched devices). They are used to control the power flow and provide dynamic stabilization. [23-29]

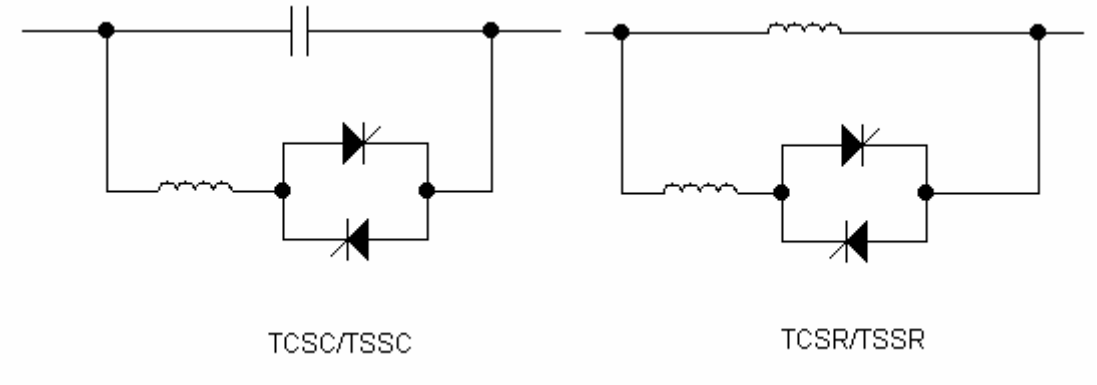


Figure 1.7 Thyristor controlled/switched capacitor/reactor

(3) **Thyristor controlled phase shifter transformer (TCPST).** As shown in Figure 1.8, the TCPST inject a small voltage $\overline{V_i}$, perpendicular to the voltage $\overline{V}$, into the transmission line. In this way, the transmission line voltage phase angle changes, without much magnitude change. TCPST controls the power angle as in Equation (1), thus control the transmittable active power. [30-31]

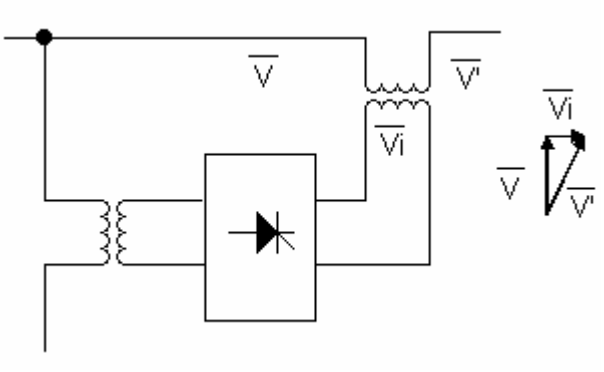


Figure 1.8 Thyristor controlled phase shift transformer

As the semiconductor industry moves forward, power electronic devices have developed remarkably. Commercially available phase-controlled thyristor (also known as silicon-controlled rectifier or SCR) can be rated up to 8,500V and 2370A [32]. The gate turn-off Thyristor (GTO), which can be turned on and turned off by gating signals, has rated up to 6500V, 1500A [33]. , Figure 1.9 depicts the packaging of a 6500V GTO from DYNEX Semiconductor Ltd. Based on the GTO, other voltage control type high power devices were invented. Those devices include MTO (MOS Turn-off Thyristor) [34], ETO (Emitter Turn-off Thyristor) [35-36], IGCT (Integrated gate-commutated thyristor) [37], and MCT (MOS Controlled Thyristor) [38], etc. Those devices improve the turn-off capability and ease the gate driver circuits of the GTO. Switching frequency of those GTO based devices can go to several kilo Hertz.

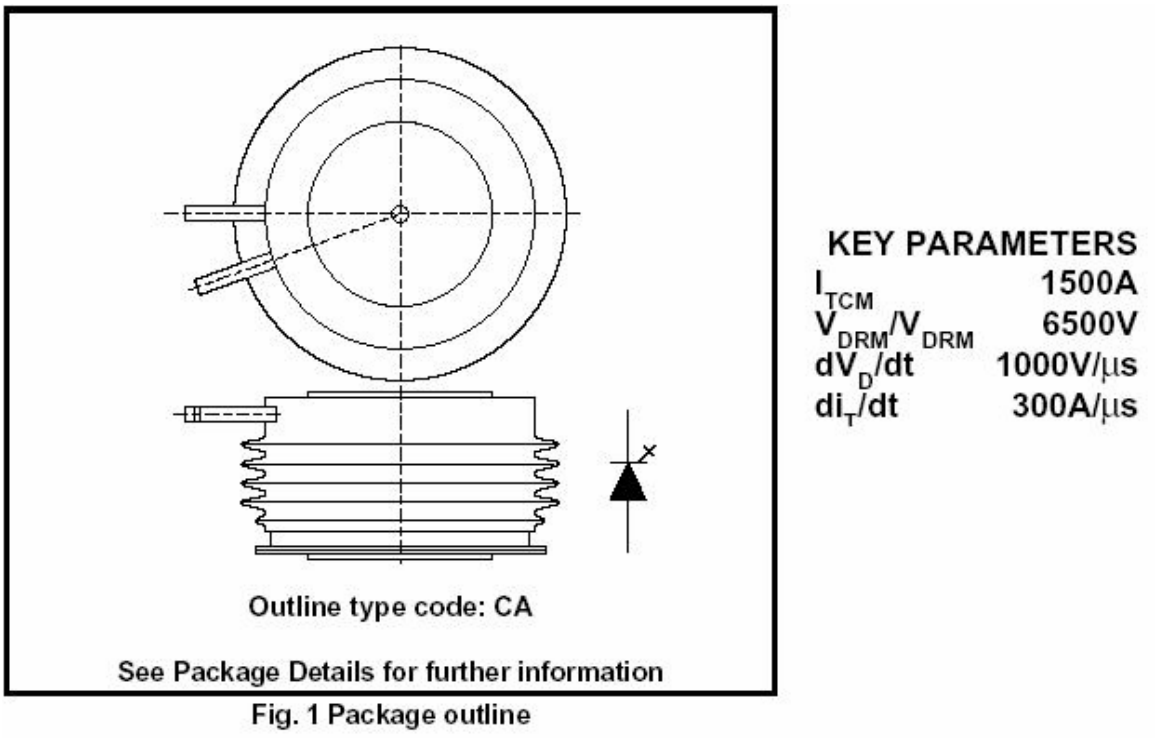


Figure 1.9 GTO DGT409BCA from DYNEX semiconductor ltd.

In medium power application, the IGBT (Insulated Gate Bipolar Transistor), which has better turn on/off ability, has extended its voltage level greatly [39-42]. IGBT with voltage rating of 6500 Volts and current rating of 400A is commercially available from DYNEX Semiconductor Ltd. [42]

At the same time, emerging devices based on silicon carbide (SiC) and diamond have been invented in both research labs and industries. Silicon carbide has wider band gap, higher thermal conductivity and melting point than present silicon devices. It is chemically inert. Its outstanding electric and physical properties make it an excellent material for high voltage, high frequency, and high working temperature power devices [43-44]. Commercially, some companies have been offering SiC diodes, rated at 300V, 600V, and 1200V.[2] Field emission devices made from chemical vapor deposition (CVD) diamond is an emerging technology that has potential applicability for power electronics. Due to its low or

[2] www.cree.com

even negative electron affinity, diamond is a prime candidate material for field emission devices. It also has other advantageous properties: the strongest known material; high dielectric strength and thermal conductivity; chemical inertness; and, immunity to radiation. Its thermal conductivity is over 5 times that of copper [45-46]. Figure 1.10 illustrates the SEM (Scanning Electron Microscope) image of a CVD diamond field emission triode developed at the Vanderbilt University. There is no commercially available CVD diamond device yet. However, with related technology development, we can expect diamond vacuum devices to be available commercially for power electronics reasonably soon.

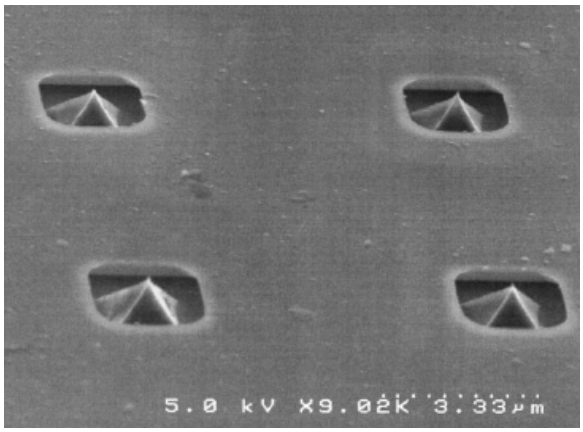


Figure 1.10 SEM image of the 2X2 microtips of the CVD diamond field emission triode

The GTO and the developing devices, high voltage IGBT and the emerging silicon carbide and diamond devices, facilitate the high voltage level converter based FACTS devices in power transmission application. High voltage, high frequency devices are expected to revolutionize utility application “by extending the use of Pulse Width Modulation (PWM) technology to high voltage applications” [47].

With the background of the development of high voltage, high power devices, other types of converter-based FACTS devices have been developing rapidly. The converter-based FACTS devices are categorized into three groups according to the parameters they changed in the power transmission equations (1) and (2).

(1) **STATic synchronous COMpensator (STATCOM)**. The STATCOM is used to control the line voltage by injecting or absorbing reactive power. It can provide full capacitive/inductive current at any voltage. Whereas the reactive current in thyristor-based SVC is decided by its capacitor/inductor value and system voltage. The STATCOM also demonstrates better transient stability than SVC. According to the energy storage device the STATCOM uses, there are voltage source and current source based STATCOMs. The voltage source STATCOM uses a capacitor as the energy storage device, as illustrated in Figure 1.11. The current source STATCOM has an inductor as the energy storage device. In practice, there have been several STATCOM installations in USA, Japan, and some other countries. [48-53]

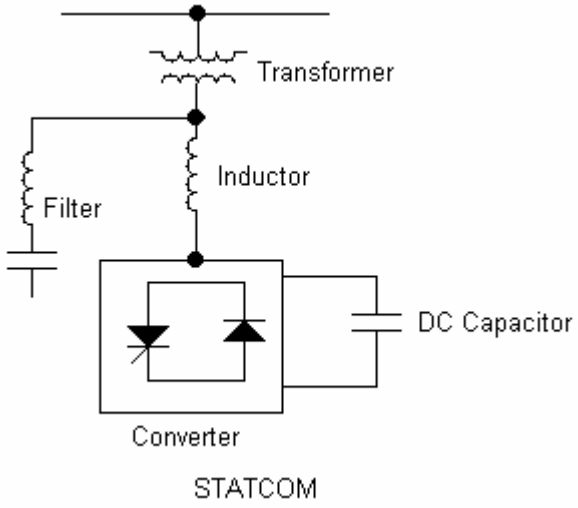


Figure 1.11 Voltage source STATCOM

(2) **Static Synchronous Series Compensator (SSSC)**. The SSSC is a converter-based series device. Without an extra energy storage device, the SSSC is used to inject a voltage V_c into the transmission line, which is either leading or lagging the line current by 90^0 as illustrated by Figure 1.12. Thus, the effect is that the inductance of the transmission line is changed accordingly. Compared with thyristor based series devices, the voltage injected by the

SSSC is not limited of the transmission line current. The injected voltage by the SSSC can be controlled independently. [54-57].

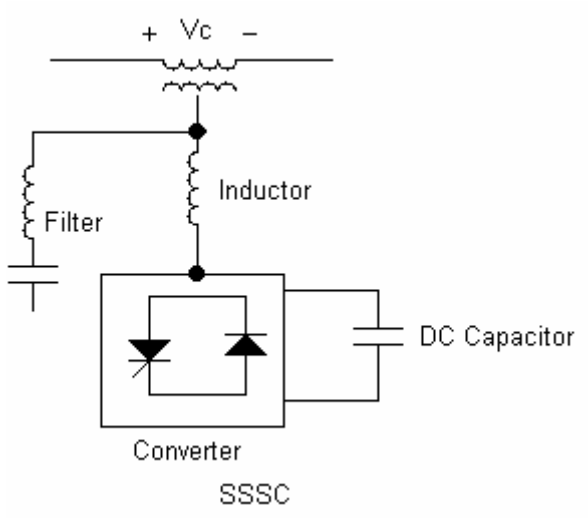


Figure 1.12 Typical structure of the SSSC

(3) **Unified Power Flow Controller (UPFC)**. The UPFC concept was proposed by Gyugyi in 1991. As its name implied, UPFC can change all the parameters affecting power flow in the transmission line, including the voltage magnitude, the line impedance, and the power angle. Figure 1.13 illustrates the typical structure of a UPFC. It has two switching converters, the shunt converter and the series converter, sharing the same DC link capacitor. The unique characteristic of the UPFC is that the real power can flow between those two converters. Converter2 can inject a voltage into the transmission line V_c with controllable magnitude and phase angle. Reactive power exchanged between converter2 and converter1 is generated locally in itself. Converter1 can supply or absorb the real power demanded by converter2. At the same time, converter1 also works as a STATCOM controlling the bus voltage. In the UPFC, the converter2 provides the main function by injecting a voltage V_c into the transmission line. The magnitude of the injected voltage can be in the range of 0 to the maximum voltage rating of the converter2. Its phase angle can be from 0^0 to 360^0. [58-60].

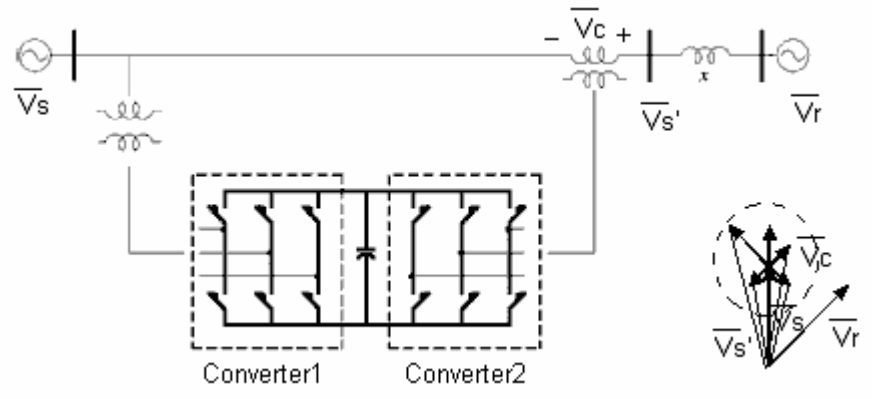


Figure 1.13 Typical configuration of UPFC

The development of the converter-based FACTS devices is progressing rapidly. There are numerous researchers in universities and industry working in this area. The most recent FACTS devices include Interline Power Flow Controller (IPFC) [61], Unified Power Quality Conditioner (UPQC) [62], to just list a few of them. Research is also being conducted on FACTS devices with energy storage components, like battery storage and Super Conducting Magnetic Energy Storage (SMES) [63-66].

The FACTS device is a proven technology in power transmission application. There have been quite a few installations. Those installations include WAPA's Kayenta advanced series capacitor (in fact, a TCSC), BPA's Slatt Thyristor Controlled Series Capacitor (TCSC), North-South interconnection TCSC, Stode TCSC in Sweden, TVA's Sullivan Static Condenser (STATCOM), AEP's Inez unified Power Flow Controller (UPFC), etc. [13, 67] This dissertation mainly focuses on the UPFC application in addressing the problem of power flow control and voltage regulation.

1.4 Proposed research

1.4.1Motivation

The above discussed Unified Power Flow Controller (UPFC) offers good promise to enhance the performance of the electric power grid by providing voltage stability while improving the power flow potential. The UPFC of present technology is typically located at either the sending end or receiving end of a transmission line. It will be referred to as a concentrated UPFC (CUPFC). There are three major problem areas associated with the CUPFC that have hindered its widespread acceptance by the electric utilities - reliability, cost, and footprint requirement. This dissertation studies a new UPFC technology that addresses these three impediments. This novel technology is called the Distributed UPFC (DUPFC). The following discussion clarifies the problems attributed to the CUPFC while introducing the DUPFC advantages.

a. **Reliability** - The CUPFC loses all capability upon occurrence of a single point failure. Further, since each installation is a custom design, repair operation can only be handled by the manufacturer. Downtime can easily consume a couple of weeks while incurring the labor cost of high level technicians and/or engineers to make repairs. The DUPFC is by nature a group of independently functioning devices - say maybe a 100 miniature UPFCs. Thus, a single point failure leaves the system with still a 99% full performance capability.

b. **Cost** - The CUPFC is a custom design assembled on site making the initial cost prohibitively expensive except for locations in the grid where performance is extremely deficient. The CUPFC has a price tag in the $250/kVA. The proposed DUPFC lends itself to a standard design suitable for assembly line manufacture. The implementation of the emerging SiC or CVD switch technology should allow use of simple SPWM switching schemes rather than the transformer mixing of 24-48 step waveforms as done with the present CUPFC technology. Further, the high voltage capability of the emerging switches has the potential to operate the

shunt portion of the DUPFC with direct connection to the transmission level voltages. The magnetics of the CUPFC are half, or more, of the total device volume and form a significant portion of the initial cost. Between the assembly line manufacturing process and the reduction in the required magnetics, it is anticipated that the DUPFC initial cost can be in the $100/kVA range.

The DUPFC should also show advantage in maintenance cost. Warehousing of spare units will now be practical. Replacement of failed units can be handled by utility linemen. Failed units can be serviced at repair centers.

c. **Footprint** - The CUPFC must have a new footprint near a substation. Typically, an expansion of the substation real estate will be necessary leading to hearings, permits, and likely court supported condemnation proceedings - expensive undertakings that can require months to years to complete. The DUPFC mounts on existing transmission towers, thus installation is truly a zero footprint situation totally under control of the electric utility.

1.4.2Proposed DUPFC System Structure

To the problems the CUPFC confronts, this dissertation provides a feasible solution – the Distributed UPFC (DUPFC). Same as the personal computer to main frame, the concept of the DUPFC intends to utilize the economics of scale to decrease the cost, complexity, and to improve the reliability of the UPFC system.

The DUPFC system control is shown in Figure 1.14. A certain number of DUPFC units are installed along the transmission line between two buses. The number of DUPFC units is decided by the total required kVA rating divided by the kVA rating of single DUPFC unit.

For implementation, a central control unit accepts control commands from the system operator. Those commands include real and reactive power to be transmitted from one bus to the other, and the voltage to be controlled at some

point along the transmission line. The central control unit computes the total required series voltage, and the shunt real and reactive power based on control commands, sampled voltage and power flow data from the transmission line. It also calculates series voltage and shunt real/reactive power commands, V_{se_n} and Q_{sh_n}, for every DUPFC unit. The central control unit provides an efficient interface between the system operator and the power transmission system. It also monitors working conditions from the field. The communication between the central control unit and the power transmission line and the DUPFC units can be done by power line carrier signal or by wireless signal through communication satellite.

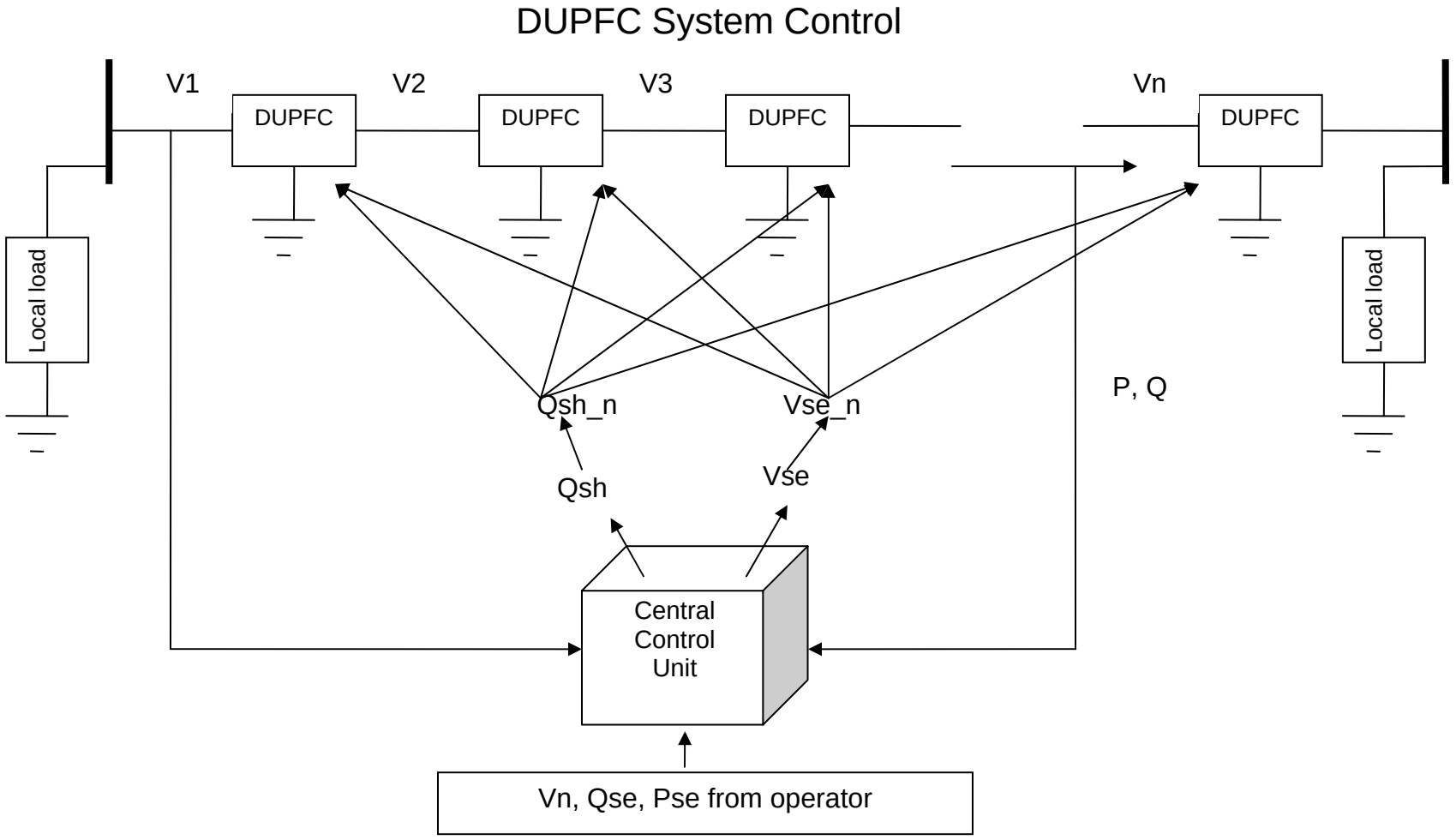


Figure 1.14 The DUPFC system structure

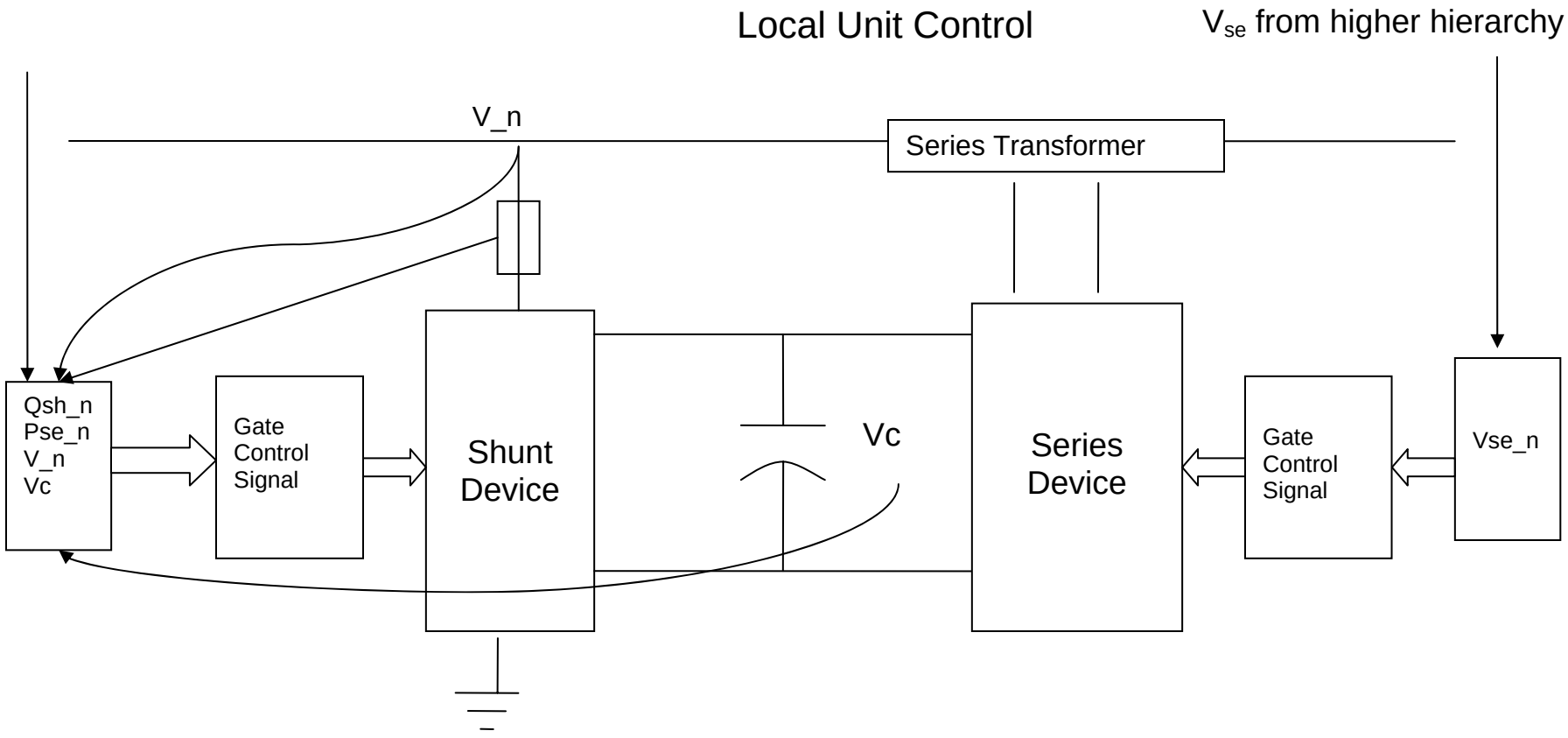


Figure 1.15 DUPFC unit diagram

The local DUPFC unit, as demonstrated in Figure 1.15, accepts commands from the central control unit. These commands include series voltage (magnitude and phase angle), and the shunt reactive power, which is to maintain voltage magnitude at certain point along the transmission line. The local unit monitors local voltage at the connection point, which provides phase angle reference for the injected series voltage, and the magnitude and phase angle reference for the shunt voltage. The local DUPFC unit works in the same way as the CUPFC works. The major differences between local DUPFC unit and the CUPFC are:

(1) Rating of the DUPFC is smaller than CUPFC. While the CUPFC always rates up to MVAR, the DUPFC unit in the DUPFC system will be rated at hundreds of kVAR. The small rating of the DUPFC unit gives itself the flexibility to be installed on existing transmission tower, to be mass manufactured in assembly lines, and to be maintained individually.

(2) The control command of DUPFC is from the system central control unit, which is to coordinate with other units to maintain certain power transmission state or realize certain control tasks.

(3) Considering the unit manufacturing cost, especially the insulation cost. The proposed system should be realized on a single-phase basis. A possible unit structure is depicted in Figure 1.16.

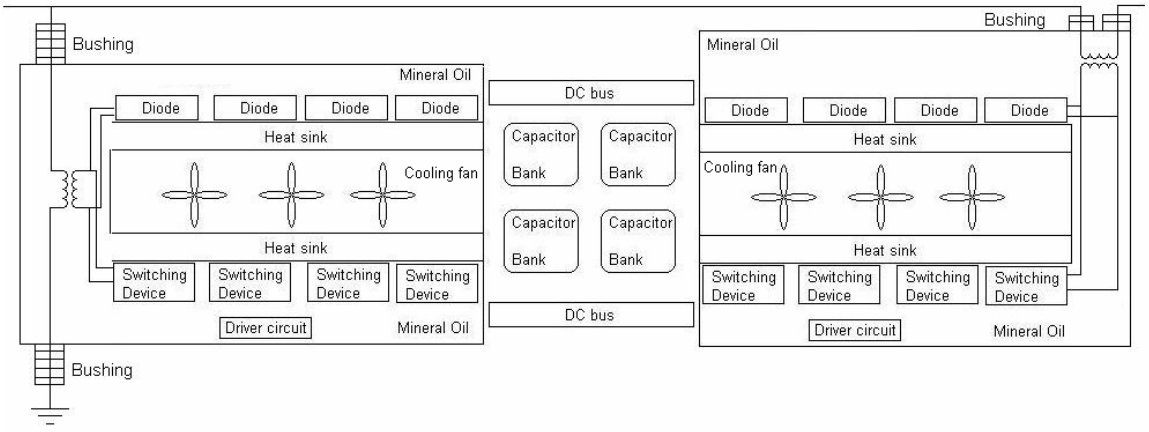


Figure 1.16 Proposed structure of a DUPFC unit

Figure 1.17 and Figure 1.18 illustrate a typical transmission tower structure. The proposed DUPFC unit will be designed to mount on the transmission tower.

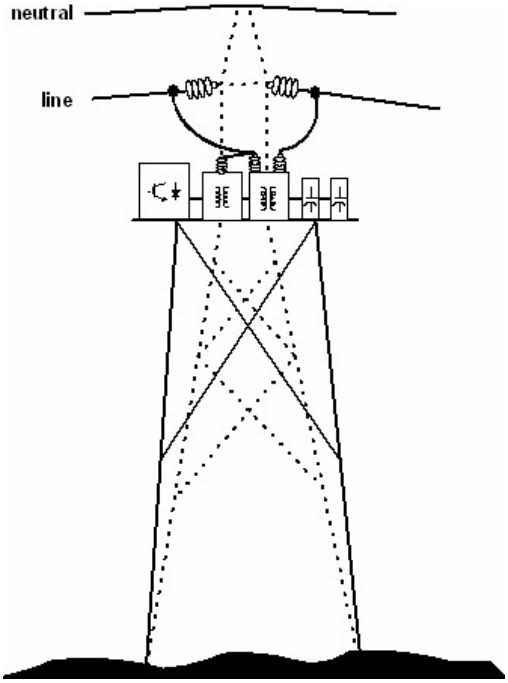


Figure 1.17 Transmission tower structure

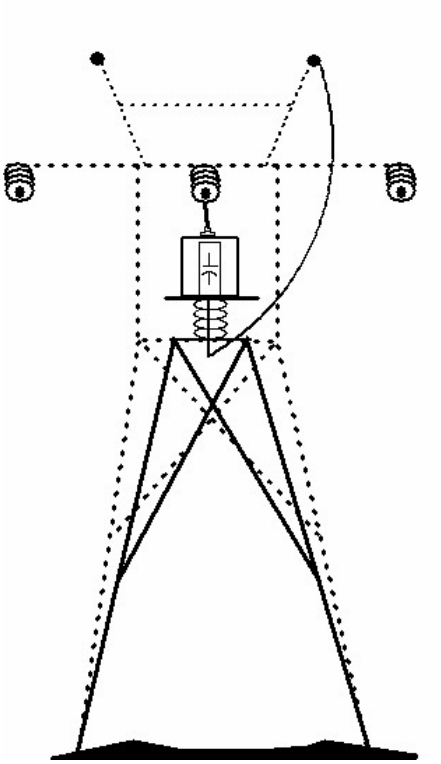


Figure 1.18 Side view of transmission tower structure

The originality of this dissertation work lies in the following goals:

1. Introduction of the DUPFC concept.
2. Presentation of performance analysis for the DUPFC.
3. Demonstration of feasibility through a laboratory model.
4. Formulization of rudimentary control concepts.
5. Identification of apparent strengths and weakness of the DUPFC.

1.5 Thesis outline

In Chapter 2, the topology of the DUPFC unit is discussed. The control for the DUPFC unite is analyzed and derived, together with functions and general control strategies. Particular control scheme related with DSP application is also discussed. This chapter gives a theoretical guideline for the control aspect of the proposed DUPFC technology.

Chapter 3 concentrates on the simulation of the proposed system. Most of the simulation was accomplished on Matlab/Simulink.

Chapter 4 demonstrates the laboratory prototype of the DUPFC system. A simplified two unit system was introduced to verify the DUPFC concept. Final conclusions on the research presented in this dissertation are given in Chapter 5.

CHAPTER 2 CONTROL SCHEME THEORETICAL DERIVATION

In this chapter, operating principles of a CUPFC are introduced. Different converter topologies suitable for UPFC application are discussed. Basic design and control blocks of CUPFC are explained together with a Matlab/Simulink model. Based on the prior developed control of the CUPFC, a control scheme for DUPFC is proposed.

2.1 UPFC working principles

The UPFC has the ability to control all the parameters affecting power flow in a transmission line, i.e. the bus voltage, the line impedance, and the power angle. It realizes the function by injecting a voltage between the sending and receiving end buses. Figure 2.1 depicts a typical three-phase UPFC configuration.

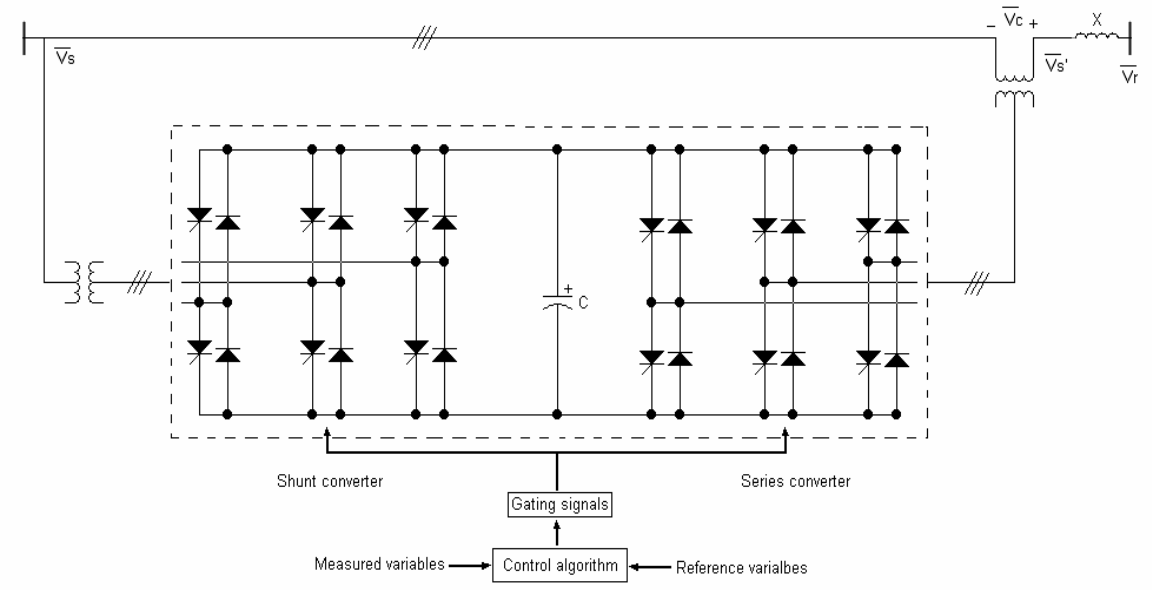


Figure 2.1 UPFC structure

As can be seen in Figure 2.1, if the series converter is disconnected, the shunt converter works as a STATCOM along with the DC capacitor and the shunt

transformer. In this situation, the STATCOM generates or absorbs reactive power to or from the Point of Connection (POC).

If the shunt converter is disconnected, the series converter will function as a SSSC along with the DC capacitor and the series transformer. The SSSC works as a voltage source injecting a voltage V_c into the transmission line through the series transformer. Magnitude of V_c is independent of the line current. Phase angle between V_c and the line current is either 90^0 or -90^0.

In the two above described situations, the shunt and series converter generates/absorbs reactive power independently. Thus, the UPFC can be modeled as a dependent voltage source (the SSSC) and a dependent current source (the STATCOM). The model is shown as Figure 2.2. Two voltage sources, V_{Th1} and V_{Th2}, are used to model two independent AC systems. X_{Th1} and X_{Th2} are their Thevenin equivalent reactance. Since the relationship between the current in the shunt converter and the effective shunt reactance is $I_c = \frac{V_1}{jX_s}$, the coefficient k_1 of the controllable current source modeling the shunt converter is equivalent to the shunt converter admittance. Likewise, the coefficient k_2 of the controllable voltage source is equivalent to the series converter reactance. For study, the circuit parameters are chosen as the following:

$\bar{V}_{Th1} = 1\angle 25^0$, X_{Th1} = 0.15pu

$\bar{V}_{Th2} = 1\angle 5^0$, X_{Th2} = 0.15pu

X = 1.00 pu

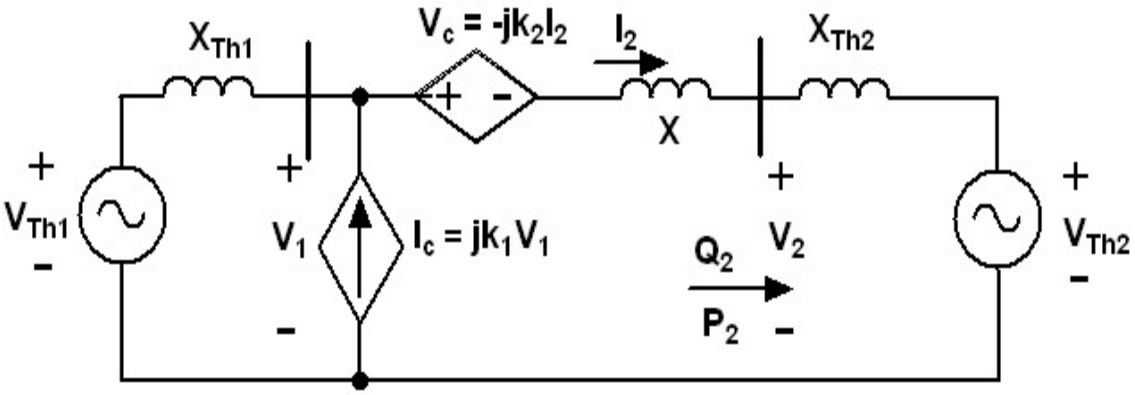


Figure 2.2 UPFC model without real power exchange between its two converters

A Matlab program is used to demonstrate the effect of the UPFC. Figure 2.3 shows the bus voltage magnitudes with different shunt and series compensation. It is obvious that the shunt device is very effective in adjusting the bus voltages. As k_1 increases from -0.25 to 0.25, magnitude of the bus voltage V_1 increases accordingly. Figure 2.4 depicts the line current magnitude with different shunt and series compensation. It can be seen that the transmission line current can be controlled by the series device effectively. The transmitted real and reactive power from bus 1 to bus 2 is illustrated in Figure 2.5. The effect of the shunt and series device in adjusting the real and reactive power flow is obvious. As k_1 and k_2 increase, the reactive power and the active power increase accordingly. The generated real and reactive power from two Thevenin equivalent voltage sources is illustrated in Figure 2.6.

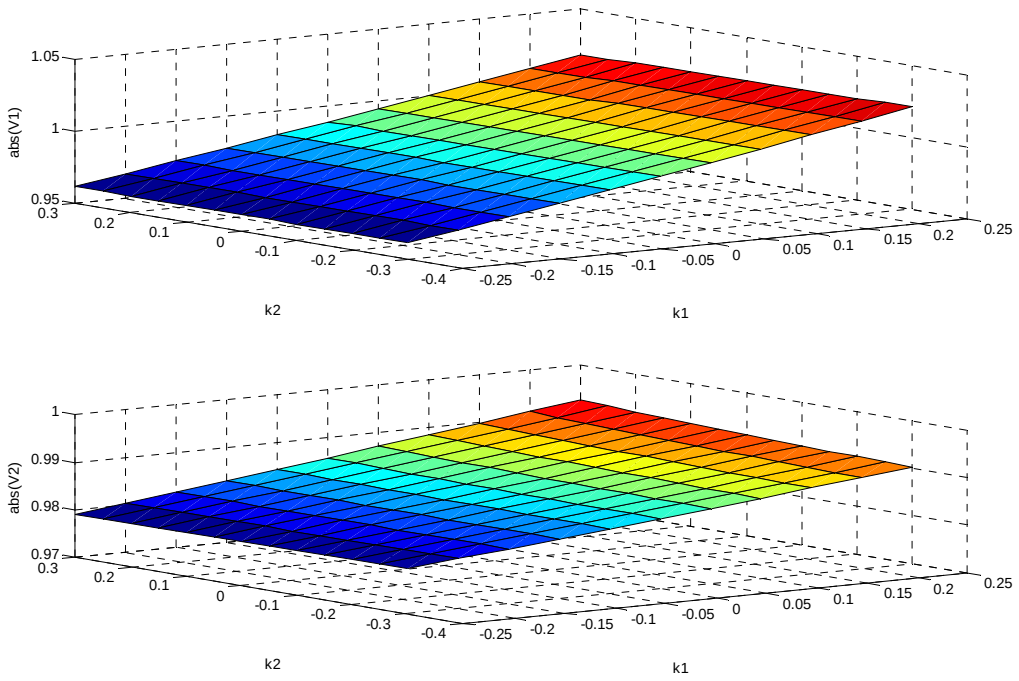


Figure 2.3 Bus voltage magnitude with different shunt and series compensation

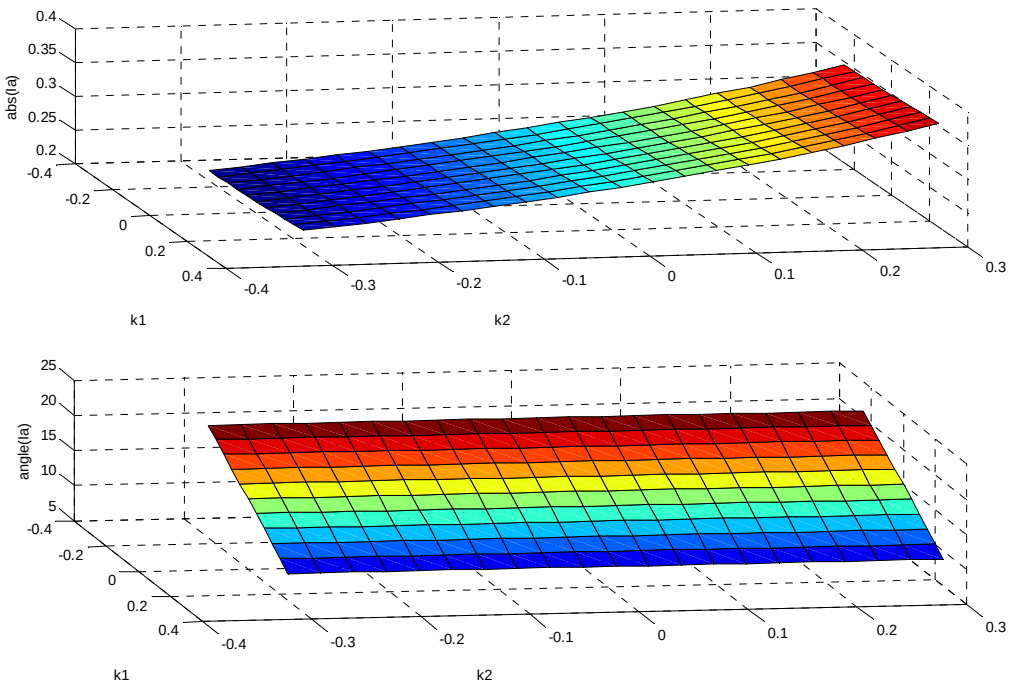


Figure 2.4 Line current magnitude with different shunt and series compensation

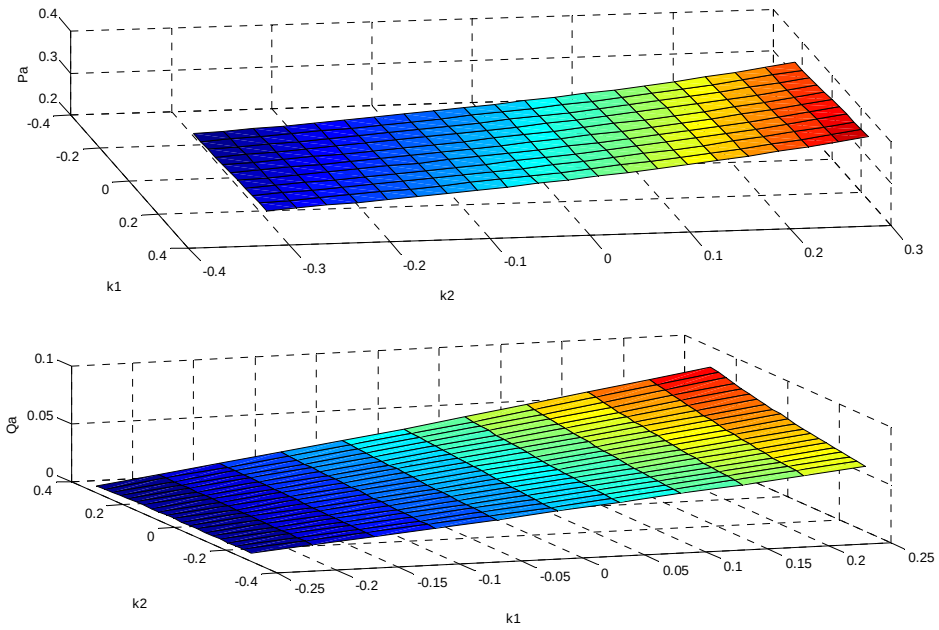


Figure 2.5 Transmitted active and reactive power with different shunt and series compensation

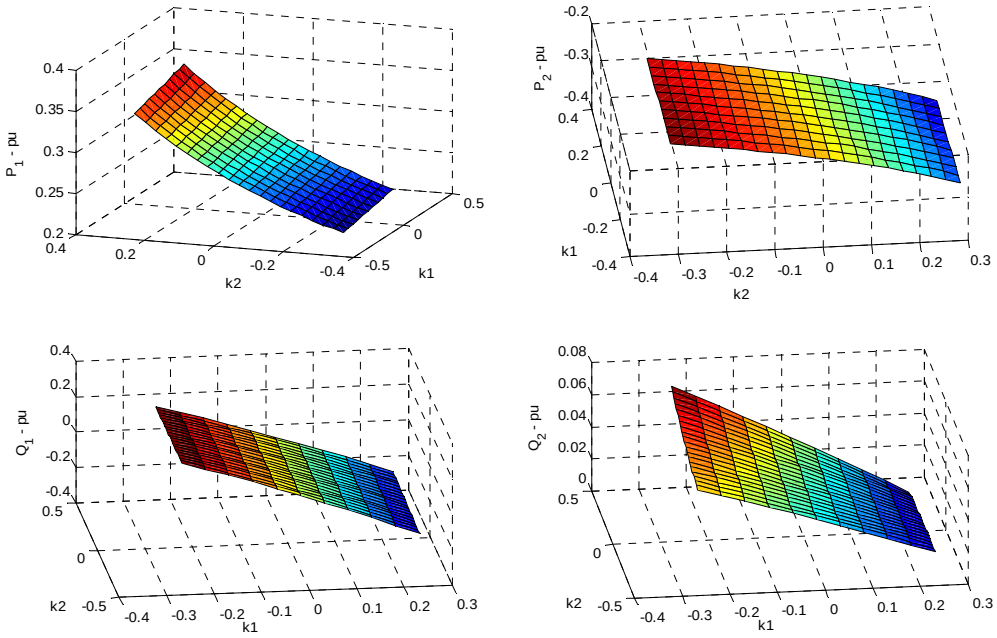


Figure 2.6 Generated power from voltage sources with different shunt and series compensation

When the two converters exchange real power, the series converter of the UPFC can change the bus voltage in other patterns. As shown in Figure 2.7, the series converter can inject a voltage Vc, which is in phase with the bus voltage. The effect is equivalent to the tap-changing transformer. However, the magnitude of the injected voltage can be continuously controlled in the range of voltage level allowable for the series converter. The series converter can also inject a voltage which is in quadrature to the bus voltage. This case is demonstrated in the previous simulation. In this mode, the series converter works to change the effective inductance of the transmission line. The series converter can also be used to change the power angle without change of the bus voltage magnitude. In the last mode, the UPFC injected a voltage which changes all the transmission line parameters: the bus voltage magnitude, the line inductance, and the phase angle [59].

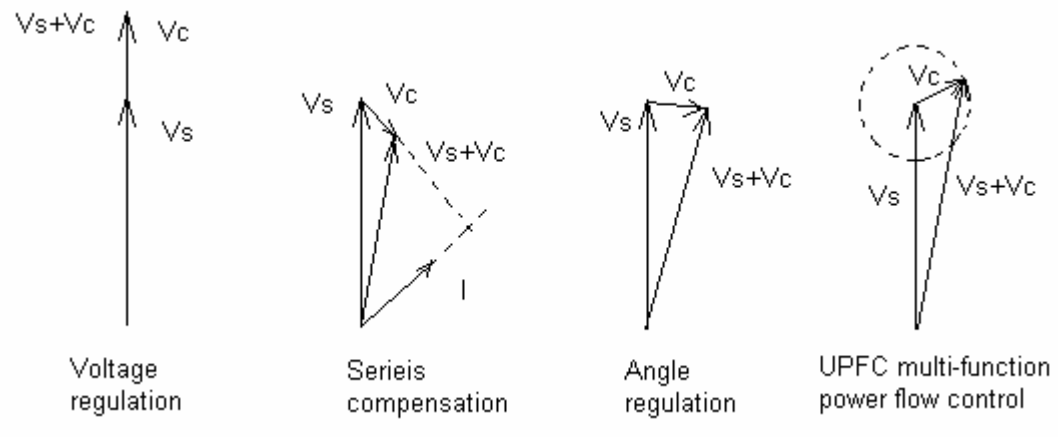


Figure 2.7 Phasor diagram when UPFC working in different modes

In practice, the series converter injected voltage is limited by several factors. One of them is the voltage rating of the inverter. The voltages on the DC capacitor, the switching devices, and the related transformer cannot exceed the designed voltage rating of each component. Due to the ability to exchange both reactive and real power with the transmission line, the series converter injected voltage can be at any phase angle when the voltage magnitude is lower than the rated

value of the converter. Thus, the achievable V_s+V_c will be in a circle as in Figure 2.7. Moreover, the voltage drop at the series transformer inductance also needs to be taken into account. The effect is that the available series converter injected voltage range shifted as the dotted line circle illustrates. The voltage drop is related to the line current. At heavy loaded transmission line, the series transformer inductance can cause additional voltage drop.

The other constraint is the bus voltage Vs'. The Vs' is limited in the range from certain minimum value to a maximum value. The constraint is shown as two curves. The result of all the constraints is that the achievable and available voltage Vs' is in the shaded area as in Figure 2.8 [68].

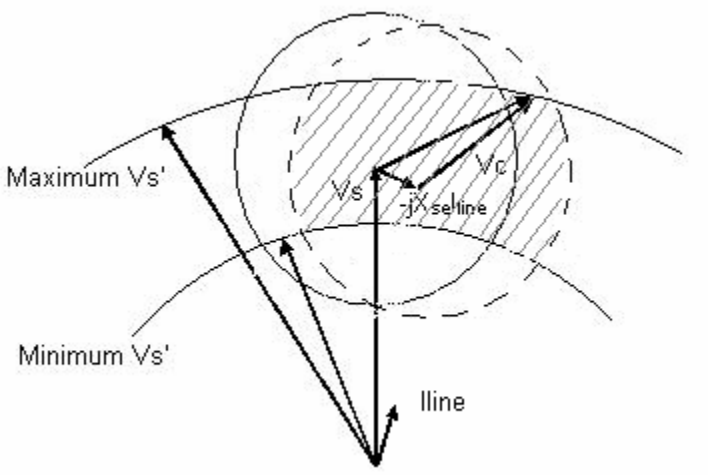


Figure 2.8 Voltage constraints of UPFC series device

2.2 Voltage source converter

In FACTS application, there are two types of converters. One is voltage source converter (VSC) as shown in Figure 2.9. The VSC use a capacitor as the energy storage device. Structure of the VSC is simple. It is highly efficient. It has fast dynamic response. The control for VSC is relatively easy [5, 69]. The other type is a current source converter (CSC) as in Figure 2.10. The CSC uses an inductor as energy storage device. Compared with VSC, the CSC has the

advantages of lower output dv/dt, easy regeneration capability and implicit short-circuit protection [70-73]. In practice, due to higher conduction loss and more complicated control of the CSC, the VSC is the dominant topology in FACTS application. However, with suitable switching devices and energy storage techniques, like superconducting devices, the CSC could be promising in high power applications [74]. This dissertation uses the voltage-source converter as the energy processing device.

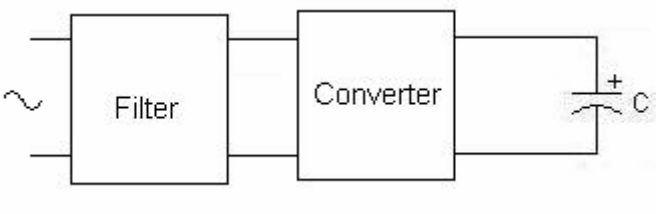


Figure 2.9 Voltage sourced converter

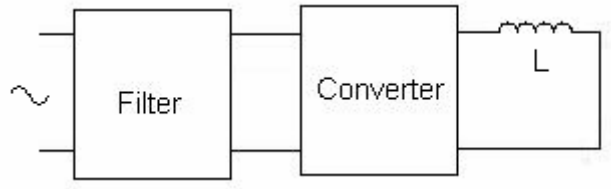
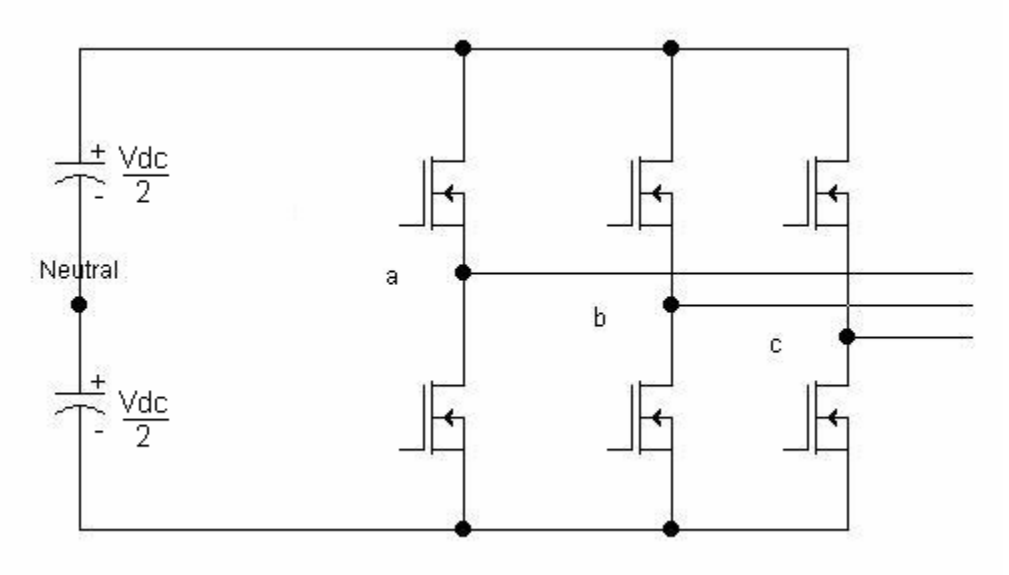


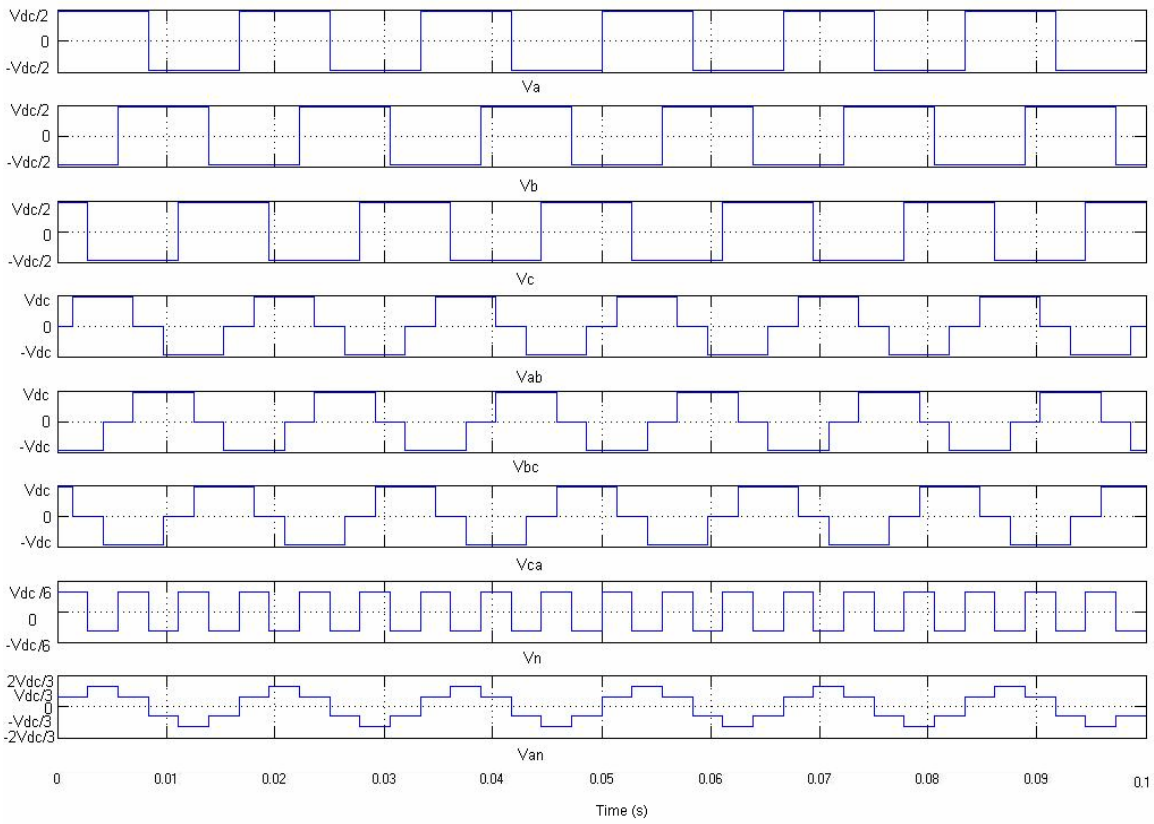
Figure 2.10 Current source converter

Figure 2.11 (a) illustrates a typical three-phase voltage-source converter with six switching devices. The switching devices used in the diagram are MOSFETs. The converter consists of three phase-legs, which operate 120 degrees apart. Figure 2.11 (b) shows some important voltage waveforms. Each phase leg voltage conducts 180^0. The voltages are bus voltages with respect to hypothetical DC capacitor midpoint labeled as *Neutral* in Figure 2.11 (a). Line voltages V_{ab}, V_{bc}, V_{ca} have peak voltage as V_{dc}. The three line voltages have pulse-width of 120^0. The hypothetical neutral voltage $V_n = \frac{1}{3}(Va + Vb + Vc)$. Its peak value is $V_{dc}/6$. The phase-to-neutral voltage, $V_{an} = (V_a - V_n)$ is also shown in Figure 2.11 (b).

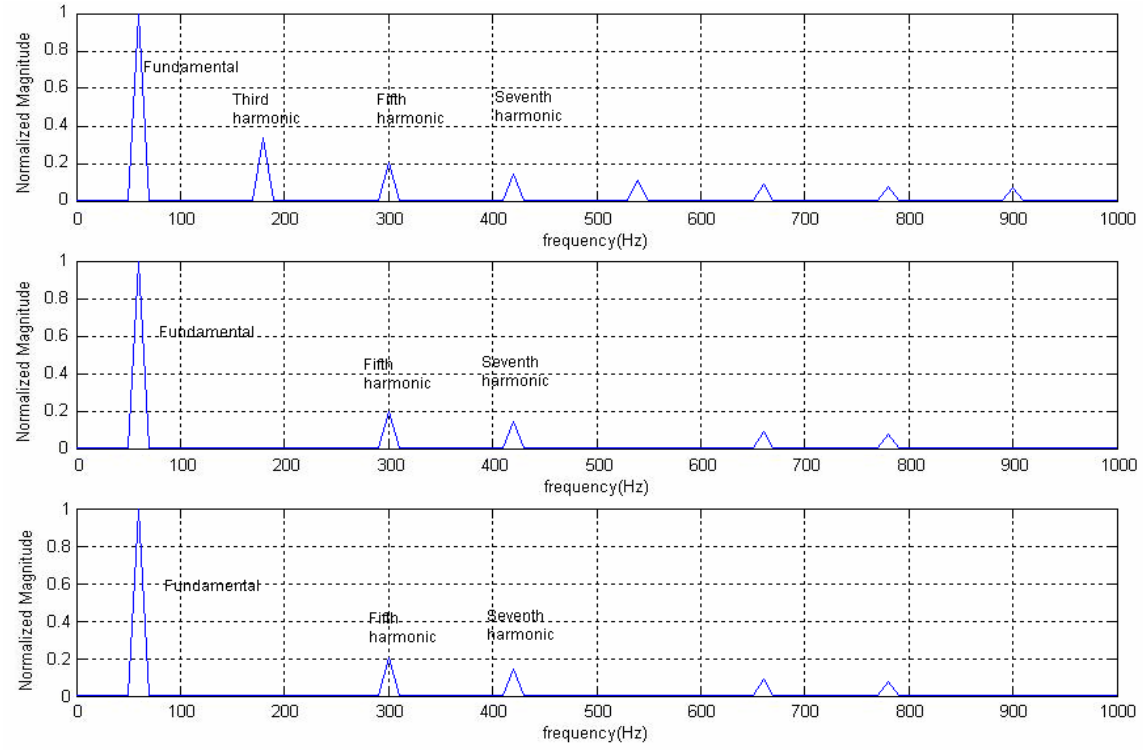
Figure 2.11 (c) illustrates the harmonic contents of the voltages. The first plot is the harmonic contents of one phase leg. The second plot is the harmonic content of the phase-to-neutral voltage. And the last one is the harmonic contents of the line-to-line voltage. It can be seen that the three-phase arrangement effectively eliminates the harmonics, of which frequency is $3\times N$ (N = 1, 2, …). However, the 5^{th} and 7^{th} harmonics still exists in the line and phase-to-neutral voltages.



(a)


Vdc/2
0
-Vdc/2
Va
Vdc/2
0
-Vdc/2
Vb
Vdc/2
0
-Vdc/2
Vc
Vdc
0
-Vdc
Vab
Vdc
0
-Vdc
Vbc
Vdc
0
-Vdc
Vca
Vdc /6
0
-Vdc/6
Vn
2Vdc/3
Vdc/3
0
-Vdc/3
-2Vdc/3
Van
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1
Time (s)

(b)


Normalized Magnitude
Fundamental
Third harmonic
Fifth harmonic
Seventh harmonic
frequency(Hz)
Normalized Magnitude
Fundamental
Fifth harmonic
Seventh harmonic
frequency(Hz)
Normalized Magnitude
Fundamental
Fifth harmonic
Seventh harmonic
frequency(Hz)

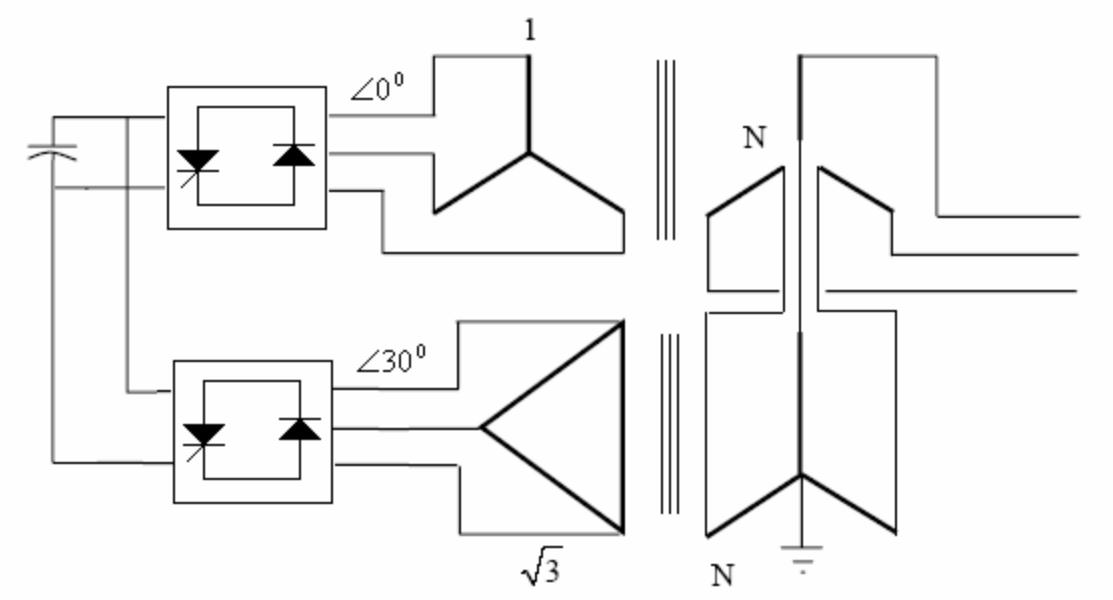
(c)

Figure 2.11 Three–phase full-bridge voltage-sourced converter
(a) Topology
(b) Waveforms for 180^0 conduction
(c) Harmonic contents of the voltages

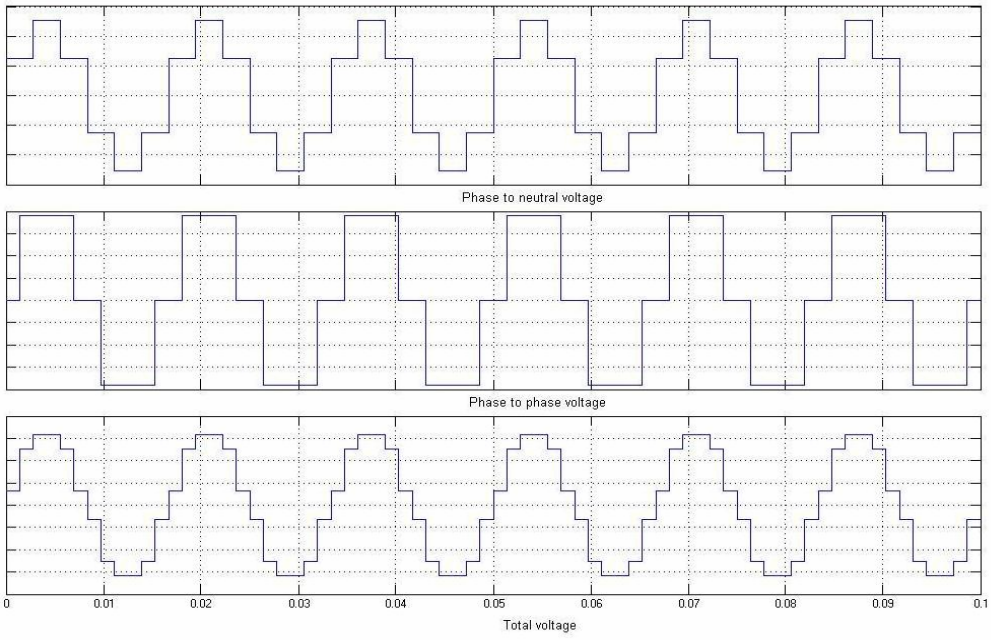
In FACTS application, to effectively eliminate the low-frequency harmonics, and also to increase the power and voltage rating, several different techniques are used, including coupling transformer, multi-level converter, and PWM techniques.

2.2.1 Coupling transformer

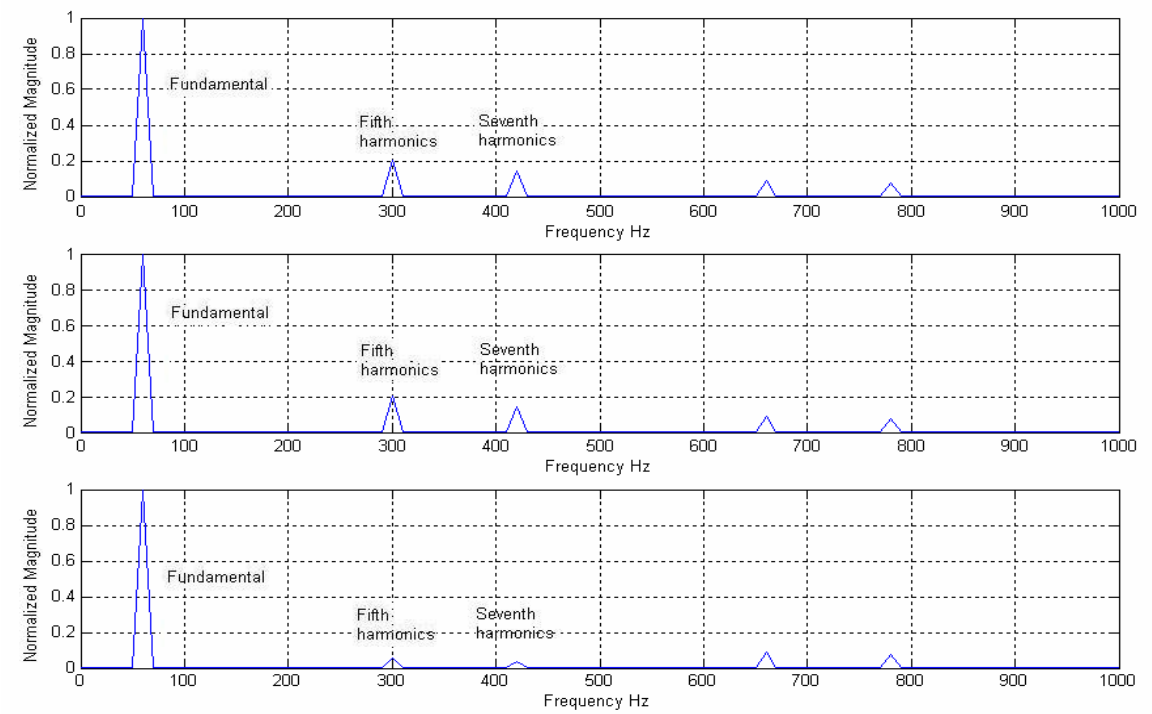
Coupling transformer technique uses n transformers with primary or secondary windings phase shifted by $60^0/n$ to cancel the phase shift due to converter operation. The secondary voltages are summed together to increase the voltage levels of the output voltage. Figure 2.12 (a) depicts the transformer connection of the 12-pulse operation. The primaries of the two sets of transformer are connected in parallel to the common DC capacitor. The secondary of the transformers are connected in series. One of the transformers uses Y/Y configuration, the other one uses Δ/Y configuration. Figure 2.12 (b) shows the voltage waveforms of the converter. The first waveform is the phase-to-neutral voltage transformed by the first transformer. The second waveform is the phase-to-phase voltage through the second transformer. Those two voltages are summed through the series connection of the secondaries of the two transformers. The resulted voltage is a 6-level voltage. Figure 2.12 (c) shows the harmonic contents of the voltages. The first plot is the FFT analysis of the phase-to-neutral phase voltage. The second plot is the FFT analysis of the line voltage. The last one is the harmonic contents of the result voltage. The 12-pulse VSC operation eliminates the 5^{th} and 7^{th} harmonics effectively. Higher number of converters can be used to remove more harmonics. The TVA's STATCOM application uses 48-pulse converter [75].


1
∠0⁰
N
∠30⁰
√3
N

(a)


Phase to neutral voltage
Phase to phase voltage
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1
Total voltage

(b)



(c)

Figure 2.12 Twelve pulse VSC

(a) 12 pulse VSC transformer connection

(b) 12 pulse VSC voltage waveforms

(c) 12 pulse VSC voltage frequency spectrum

The necessity of the customized transformer is the major disadvantage of the coupling transformer technique. Normally the transformer is bulky, heavy, and lossy.

2.2.2 Multi-level converter

The second technique to increase voltage capacity and power rating, and also to suppress harmonic contents is the multi-level converter. This technique has drawn tremendous interest world-wide after the three-level diode-clamped converter was proposed in 1980's by Akira Nabae, Isao Takahashi, and Hirofumi Akagi [76]. Besides the diode clamped converter, the capacitor clamped converter and the cascaded multi-level converter are the major topologies proposed by

numerous papers [77-81]. Figure 2.13 depicts the configuration of the three types of multi-level converters with three voltage levels. Each configuration only illustrates one basic leg of every type of converter, respectively.

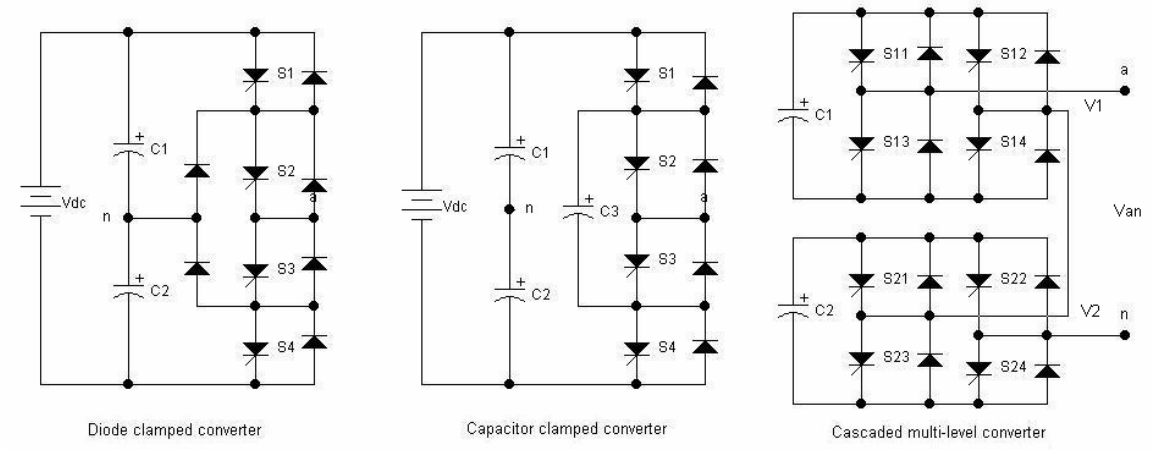


Figure 2.13 Three different types of three-level converters

For the diode clamped three-level converter, the output voltage level of one phase leg to the neutral can be Vdc/2, 0, and –Vdc/2, depending on the on/off states of the switching devices. When the switches S1 and S2 are on, the phase leg output is Vdc/2. When the switches S3 and S4 are on, the phase leg output is –Vd/2. When the switches S2 and S3 are on, the output is 0. The switch gating signals and the phase leg output are depicted in Figure 2.14.

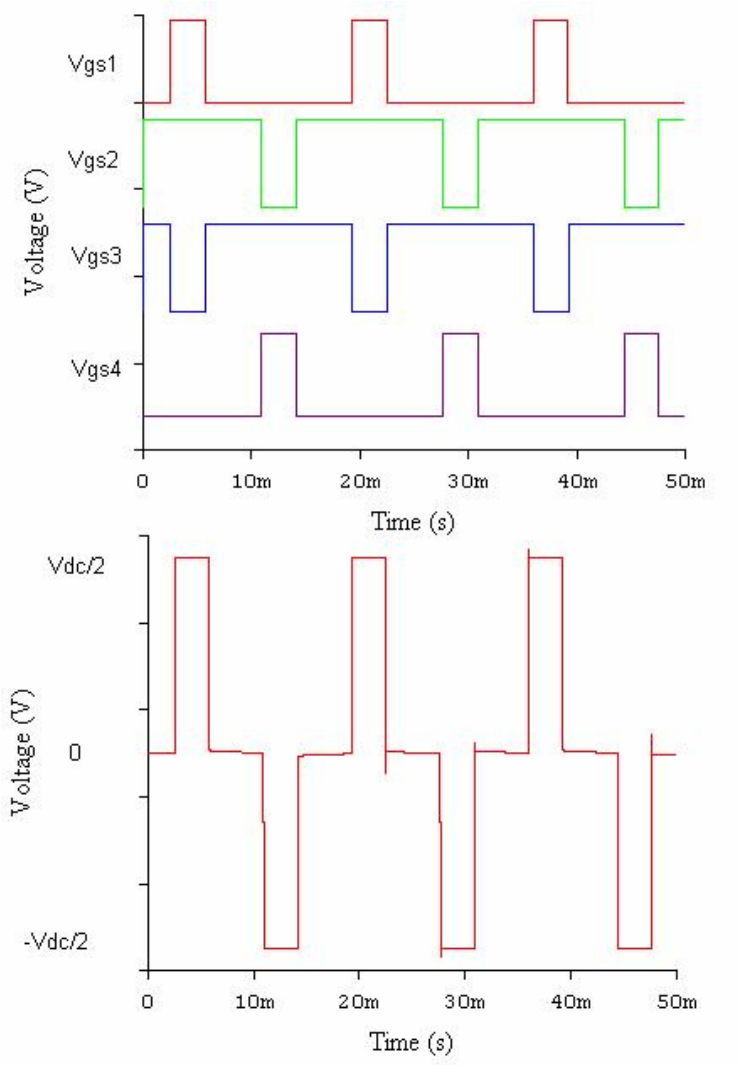


Figure 2.14 Gating signals and one phase leg output of the diode clamped converter

For the capacitor clamped three-level converter, the phase leg output is Vdc/2 when the switches S1 and S2 are on. When the switches S3 and S4 are on, the phase leg output is –Vdc/2. The output is 0, when the switches S2 and S3 are on, or when the switches S1 and S4 are on. When the switches S1 and S4 are on, the capacitor C3 is charged. When the switches S2 and S3 are on, the capacitor C3 is discharged. The voltage across the clamping capacitor C3 can be balanced by selecting different switching combination at zero voltage output.

The cascaded multi-level converter is distinctly different from the previous two types of multi-level converters in that it has separate DC voltage sources for every stage of converter. Each stage of the cascaded multi-level converter is a full bridge inverter. AC terminals of the voltage converters are connected in series. The phase leg output is the sum of the two converters. $V_{an} = V_1 + V_2$, where V_1 is the output of the first converter, V_2 the output of the second converter. Output of every converter can be one of the three voltage levels: Vdc, 0 and –Vdc. For the full bridge converter 1, when the switches S11 and S14 are on, V1 = Vdc. When the switches S12 and S13 are on, V1 = -Vdc. When all the switches are off, V1 = 0. Tthe working principle is the same for the full bridge converter 2. The conducting angles of the two full bridge converters can be controlled to minimize certain harmonics. The critical waveforms of the cascaded multilevel converter are shown in Figure 2.15.

The multilevel converter has the following advantages compared to conventional converter topologies:

1. It increases the voltage rating of the converter and generates output voltage with lower dv/dt. With several devices in series to share the high DC voltage, individual devices only need to block part of the voltage. In some application, the multilevel converter can replace the existing system without a bulky transformer. At the same time, with lower voltage potential on every stage, the dv/dt can be lowered.
2. It can eliminate some of the output voltage harmonics while individual switching devices switch at lower frequency (even at line frequency). When the number of levels in those converters is the high enough, the system may not need a filter circuit.
3. Since it allows the devices to switch at lower frequency, the switching losses of the devices can be very low.
4. Compared with the transformer coupling method, multilevel converter removes the bulky coupling transformer. Thus, the system cost, efficiency,

and size may be improved significantly. This method will take advantage of the rapid development of the semiconductor industry.

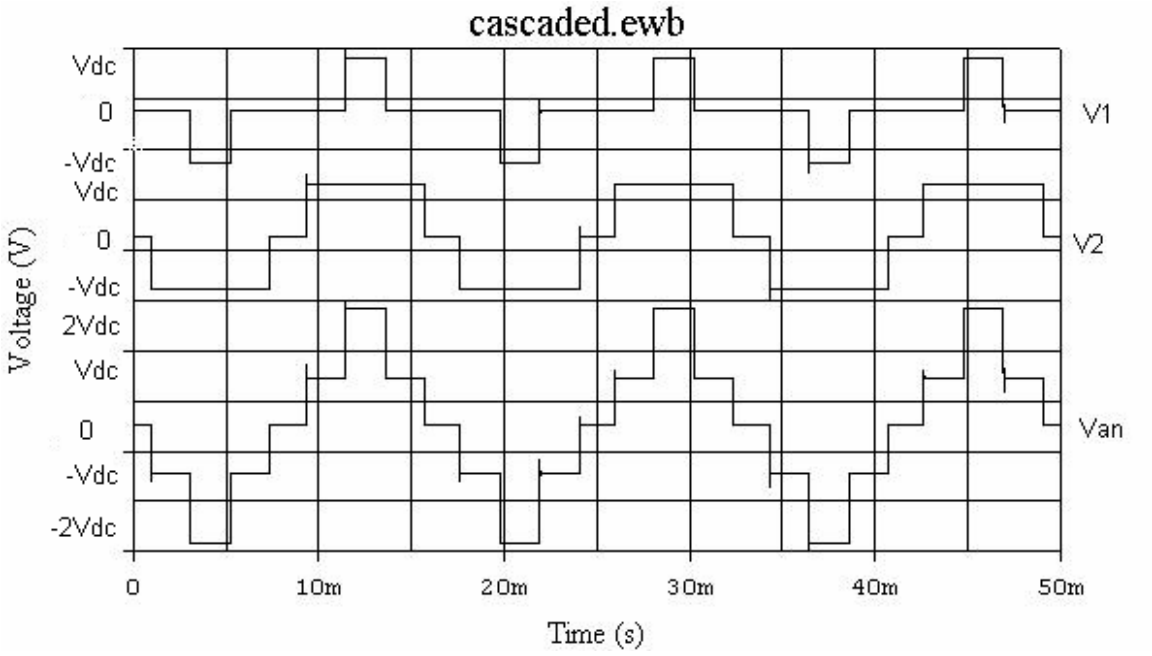


Figure 2.15 Cascaded multilevel converter voltage waveforms

At the same time, the multilevel converter also has some limitations:

1. More devices are needed for multilevel converter. For the diode clamped converter, extra clamping diodes are needed. For the capacitor clamped converter, extra clamping capacitors are needed. The number of extra clamping diodes for the diode clamped converter is (m-1)$\times$(m-2), where m is the number of voltage levels. The number of extra clamping capacitors for the capacitor clamped converter is (m-1) $\times$ (m-2)/2. When the number of the voltage levels increase, number of the clamping devices increases greatly.
2. The conduction time for different device is different. As an example, in Figure 2.15, the second full bridge converter conducts current much longer than the first full bridge converter. In designing the multilevel converter, different devices may need different ratings. Or, the worst case need be considered to choose somewhat oversized devices.

3. At some working conditions, especially when there is real power exchange, the DC bus voltages may have an unbalance problem. The voltage unbalance problem can be solved in different ways. One of the methods replaces the capacitor with batteries or pulse-width-modulation (PWM) voltage regulators. However, the additional balance circuit results in more system complexity and cost.
4. The system may be complicated compared with traditional converter topologies. With much more switching devices, the control and coordination of the overall system is complex [77].

In the past two decades, a tremendous amount of research has been done in multilevel converters. Some research has focused on increasing the voltage levels [82]. Some researchers have come up with new topologies, like mixed level hybrid multilevel converter [83], asymmetric hybrid multilevel converter [84], and soft switched multilevel converter [85]. Some research has concentrated on control and modulation strategies [86-87].

The multilevel voltage source converter solves the harmonics and EMI problems. It also balances voltage stress on switching devices. It is a very promising technique for high-voltage and high power applications. The three-level diode clamped inverter has been widely used in adjustable speed drive at medium voltage level [77]. To solve the problem of input current distortion, the three-level active front end (AFE) has been a widely accepted solution for high power motor drives [77, 88]. Figure 2.16 illustrates the configuration of the motor drive system diagram.

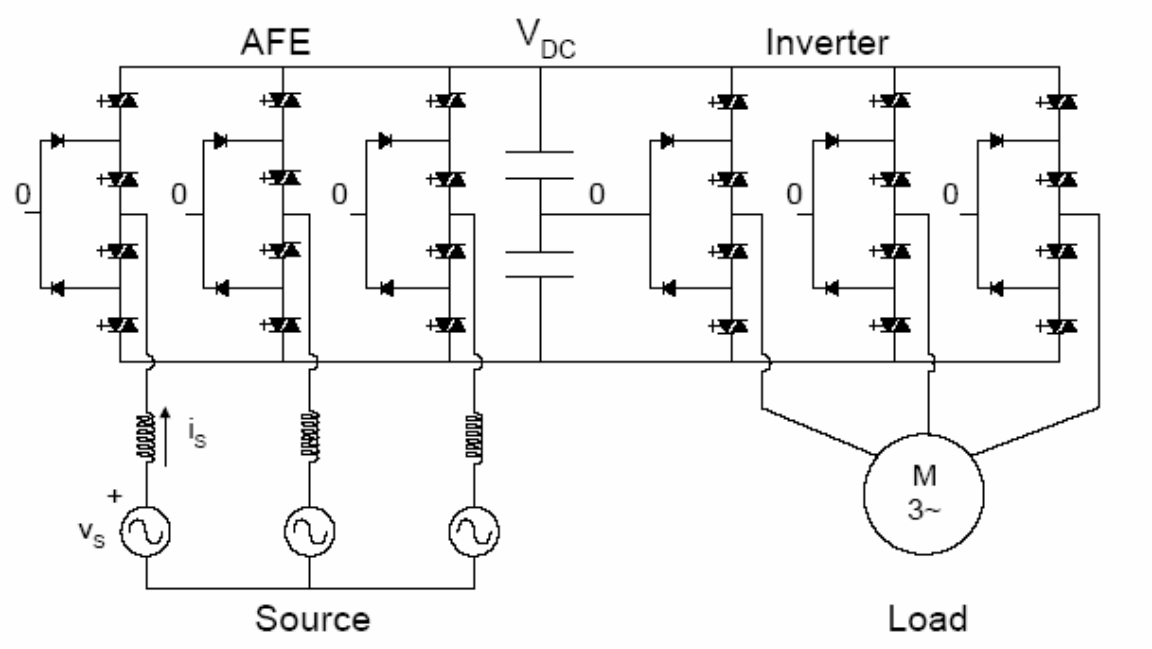


Figure 2.16 Three-level AFE for high power motor drive [88]

In power utility application, the three multilevel converters can be used in reactive power compensation without voltage unbalance problem. In this kind of application, multilevel converter draws only reactive power from the utility. The phase current is in quadrant with the voltage. The capacitor voltage can be balanced [77, 89-93].

When there is real power exchange between the power system and the converter, like application in the unified power flow controller, there may be voltage balance problems. One method to solve this problem is by using pulse-width-modulation (PWM) voltage regulators [94]. While most of the publications focus their research on diode clamped multilevel converter in UPFC application [94-95], there are several papers that study the capacitor clamped converter [96] and cascaded multilevel converter [97] in the UPFC.

The first UPFC installation at the Inez Station of the American Electric Power (AEP) in Kentucky for voltage support and power flow control uses diode clamped three-level GTO-based converters with a coupling transformer technique [98-99].

The power circuit configuration is depicted in Figure 2.17. Both converter1 and converter2 are composed of 12 three-level diode clamped converters with 48 switching devices.

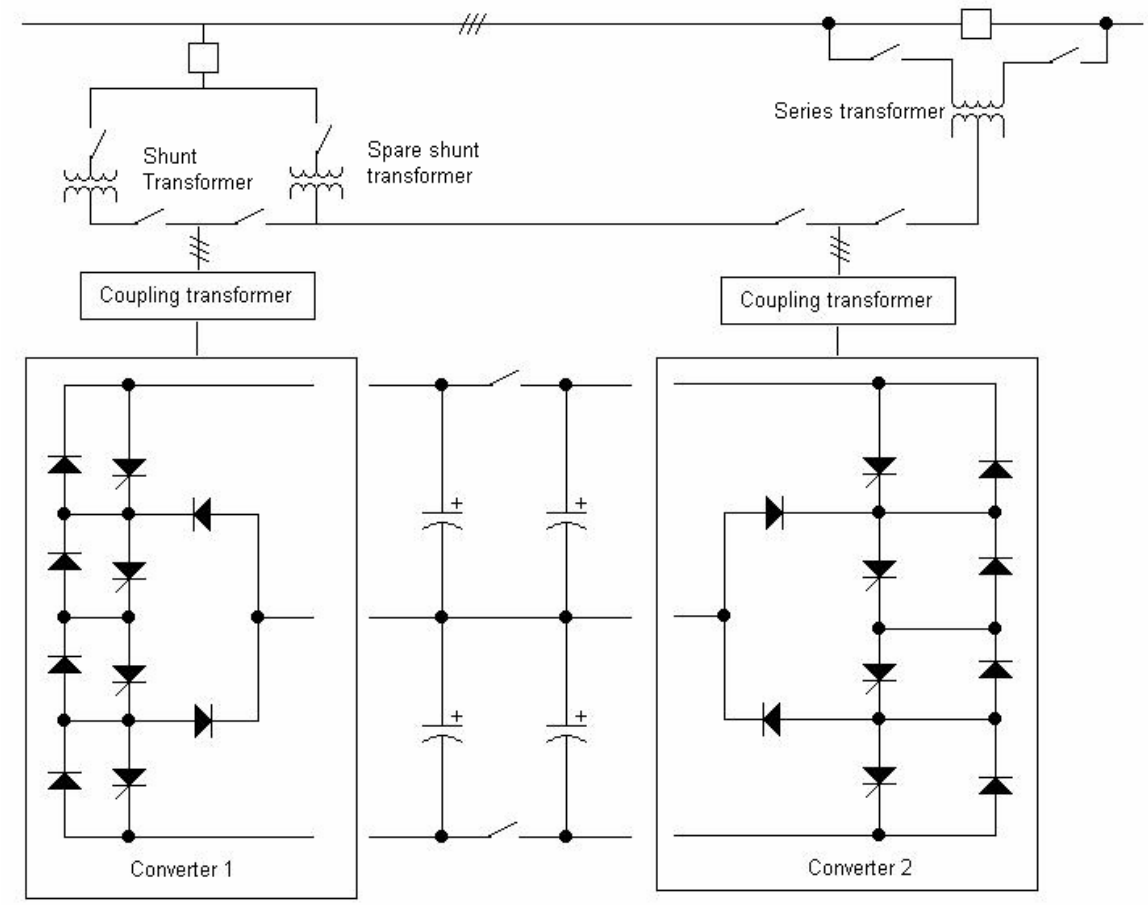


Figure 2.17 UPFC circuit diagram at Inez for AEP [5]

2.2.3 Pulse-Width Modulation (PWM)

Pulse-Width Modulation (PWM) is a proven technique to eliminate low order harmonics in DC/AC inverter. Especially, the Sinusoidal Pulse-Width Modulation (SPWM) technique is very effective in reducing waveform distortion and eliminating low order harmonics. Figure 2.18 (a) illustrates the working principle of the bipolar SPWM technique. Reference signal at desired frequency is compared with the carrier signal. If the reference signal is larger than the carrier signal, the output is high. If not, the output is low. FFT analysis of the phase leg output

voltage, as in Figure 2.18 (b), shows that the low order harmonics are effectively eliminated. Harmonic contents are pushed into much higher switching frequency range. Higher frequency harmonics are easy to filter. A smaller size low pass filter can remove the high frequency harmonics easily.

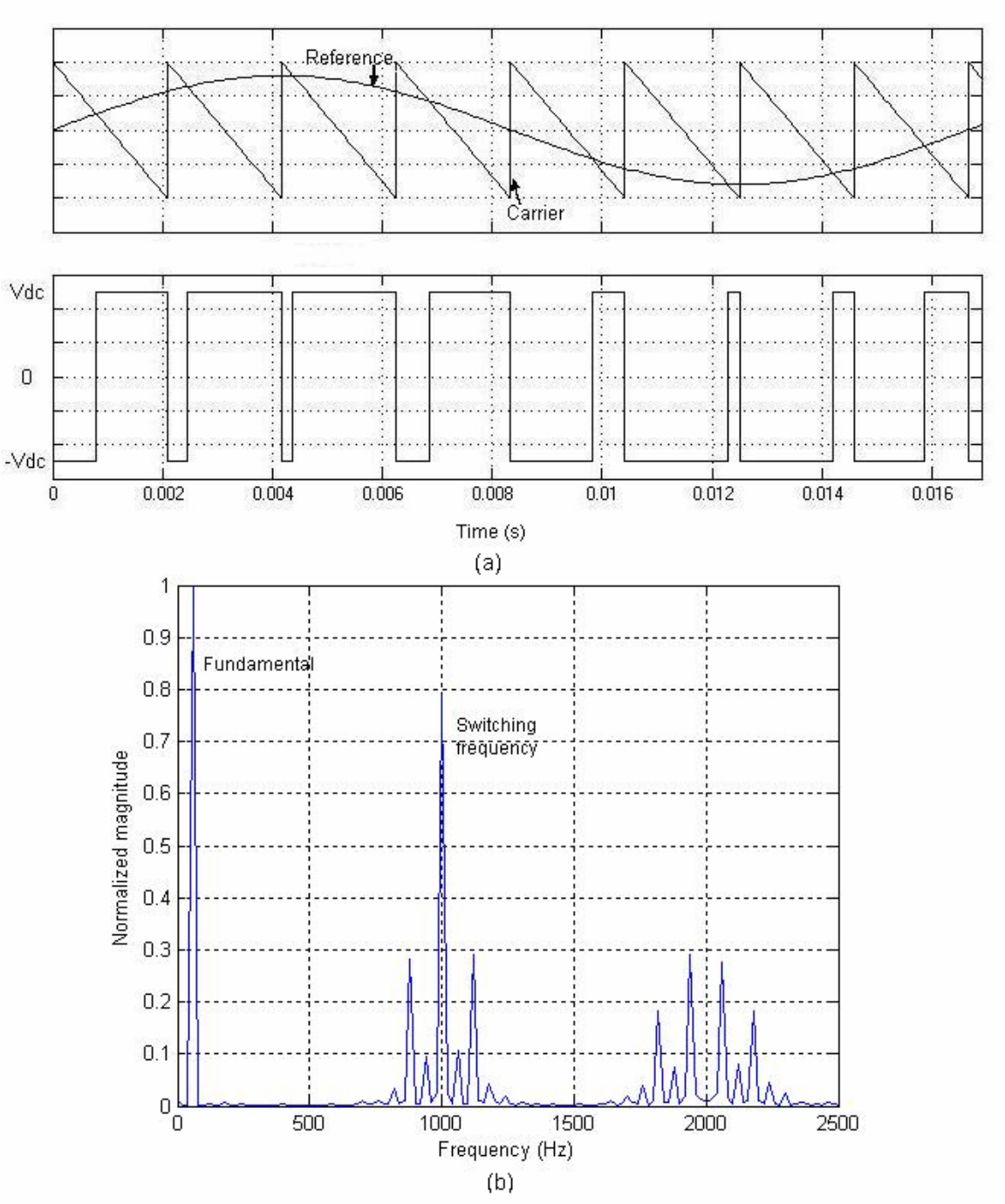


Figure 2.18 SPWM switching method

PWM converters of lower voltage and lower power applications, from several watts to several hundred watts, have had switching frequencies of several hundred kilohertz, and even megahertz [100-102]. In industrial drives, power converters switch at tens of kilohertz. For converters more than 1MW, the switching frequency may be several kilohertz. However, in FACTS applications, normally involving power of tens, even hundreds of MW, PWM technique of higher switching frequency was not considered a favorable choice, due to higher switching losses. However, switching frequency of several hundred hertz may be considered if other advantages offset the switching losses [5]. Moreover, as new low switching loss devices emerge, the SPWM technique may get accepted in FACTS applications in the near future.

In FACTS application, the application of the PWM technique can eliminate the costly and bulky mixing transformer in the current CUPFC. PWM technique can also be combined with the multilevel converter topologies to take advantage of the benefit of the both methods in suppressing harmonics and alleviating the high voltage pressure on the switching devices.

2.2.4 DUPFC converter choice

The CUPFC is a concentrated system installed at some point on the transmission line, normally at either the sending or the receiving end of the transmission line. As mentioned in 1.4.1, it has problems in reliability, cost and footprint requirement. The DUPFC system is to substitute the CUPFC in a distributed structure along the transmission line. In realizing the concept, there are several problems to consider.

(1) Power Rating

One of the major advantages of the DUPFC is its zero new footprint. To realize this goal, the DUPFC unit is designed to be installed on a platform, which

shares the existing footprint with the transmission tower. The mechanical structure of the structure was shown in Figure 1.17 and Figure 1.18. For enough mechanical strength, the total weight of the DUPFC unit cannot be over certain limit. The weight includes the shunt and series transformers, the heat sinks and fans, the capacitor banks, and the power electronics. The overall size and weight of the DUPFC unit is decided by the power rating of the device. By rough calculation, the power rating of one unit device is decided to be around 600 kVA. The total weight of the device will be around 8,000 lbs.

Moreover, to achieve the equivalent functionality, the total power of the installed DUPFC on a transmission line should be roughly equal to the power of the traditional CUPFC on the same line. For a 300MVA, 100 km transmission line, 30% of the transmission line power rating is chosen. 167 DUPFC units are needed along the transmission line.

(2) Voltage Pressure

For the DUPFC to be applied in the transmission systems, in which 138kV, 169kV, and 345kV are the normal voltage levels, the device must survive the high voltage pressure. The single-phase design alleviates the voltage pressure over the device to some extent. For the above-mentioned normal transmission voltages, corresponding single-phase peak voltage are 112.7kV, 138kV, and 281.7kV respectively. The design as in Figure 2.19 considers the voltage capability of currently existing switching devices, with two power transformers. For the emerging devices as silicon carbide and CVD diamond switching devices, the rated device voltage are expected to be greater than 10kV and 15kV [103]. The high voltage blocking capability of the emerging devices has the potential to eliminate the shunt transformer for the future DUPFC device. The number of series switching devices needed for blocking the high transmission line voltage in a three level diode clamped converter is listed in Table 2.1. In fact, five level, or

even higher level, converter can be used to further decrease the number of series devises.

Considering those factors, the diode clamped multilevel converter structure shown in Figure 2.19 is considered feasible for the present technology. In the configuration, most of the device is floating. Only the primary side of the shunt transformer is connected to the high transmission voltage. Thus, the structure needs only one high voltage insulator between itself and the transmission line.

Table 2.1 Expected number of series devices for emerging devices using the three level diode clamped converter topology

Line-line voltage	Series devices/cell (SiC)	Series devices/cell (CVDD)
138 kV	6	4
169 kV	7	5
345 kV	14	9

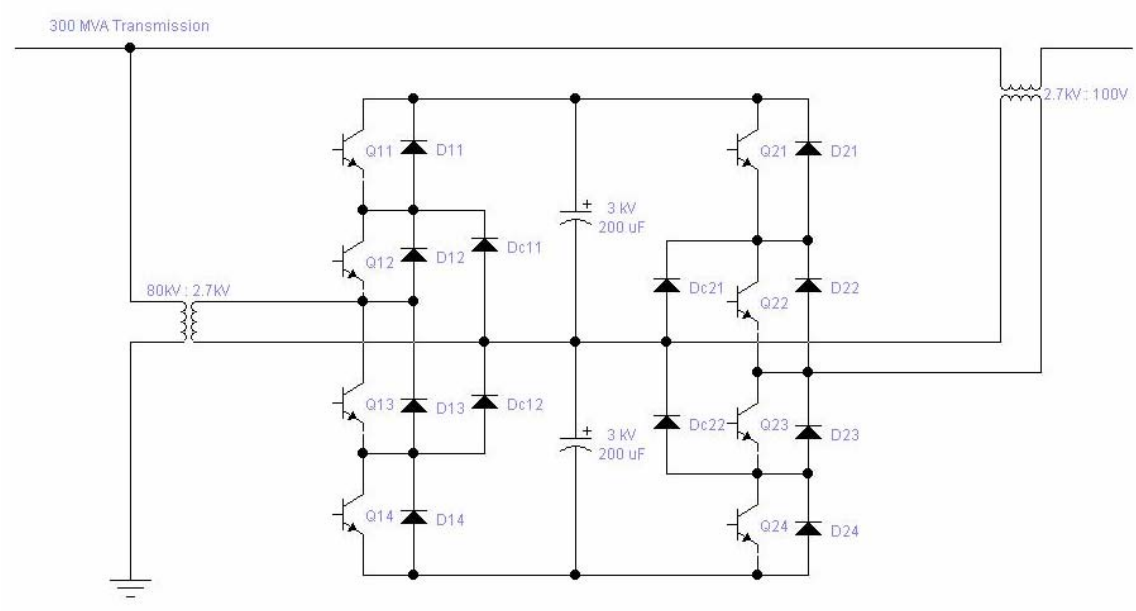


Figure 2.19 Prefered DUPFC unit configuration

For the DUPFC, power rating of every unit device is designed to be in the range of hundreds of kVA. In this power rating, PWM at lower switching frequency,

like hundreds, or a few kilohertz, is feasible. For the three level diode clamped inverter, all PWM techniques can be used to remove lower order harmonics [104-105]. Figure 2.20 illustrates the working principle of the carrier-based three-level PWM inverter. The reference signal is compared with two triangle waveforms to produce gating signals for the switches of the three-level inverter. The lowest trace is the output of one phase leg of the inverter.

The main purpose of this dissertation is to investigate the possibility of the DUPFC concept. In both simulation and experiment, the single-phase half-bridge converter topology with SPWM is used to verify the concept. However, in practical application, the multi-level converter may be used to take advantage of the benefit of the technique.

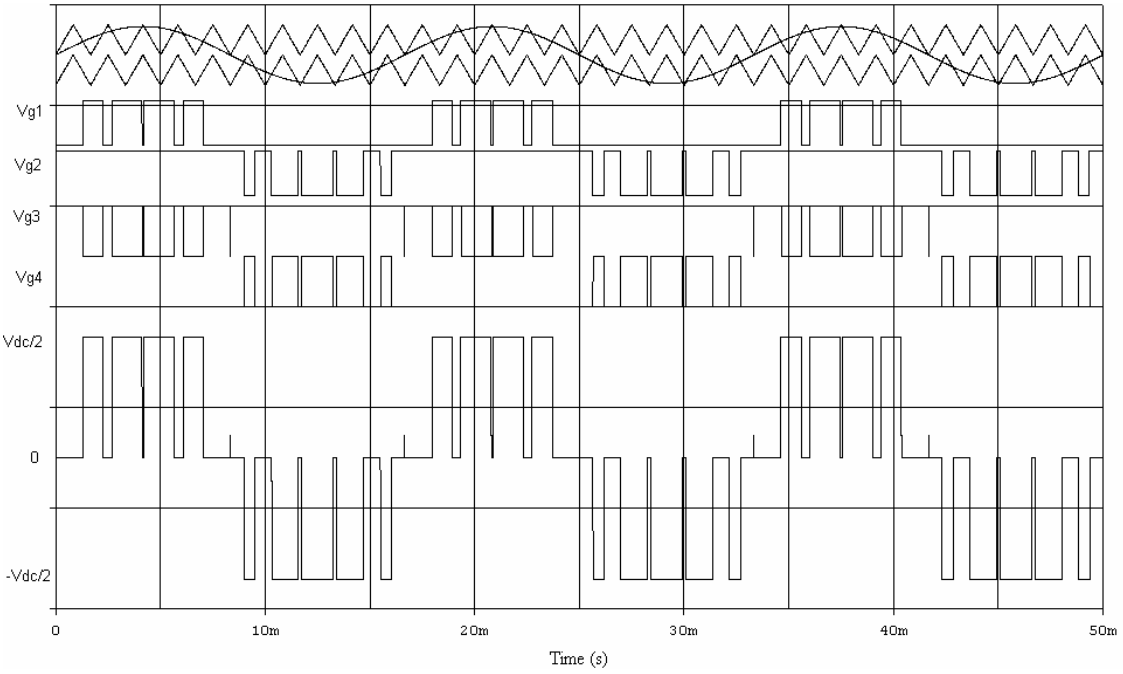


Figure 2.20 Waveforms of three level carrier-based PWM method

2.3 Instantaneous power measurement in d-q axis space

In UPFC application, controlling the power flow on a transmission line depends on precision measurement of the real and reactive power. For fast

response of the FACTS devices, the traditional definition of real and reactive power by averaging over cycles cannot satisfy the requirement. The instantaneous power theory, introduced by Akagi [106], provided a powerful tool for power system real time control.

2.3.1 Three phase instantaneous power

In a balanced three-phase power system, without zero or negative sequence components, is shown in Figure 2.21. The three-phase voltages can be expressed as:

$$\begin{cases} v_a = V\cos(\omega t) \\ v_b = V\cos(\omega t - 120^0) \\ v_c = V\cos(\omega t + 120^0) \end{cases} \quad (1)$$

where V is the peak value of the voltages.

And the currents can be written as:

$$\begin{cases} i_a = I\cos(\omega t - \theta) \\ i_b = I\cos(\omega t - \theta - 120^0) \\ i_c = I\cos(\omega t - \theta + 120^0) \end{cases} \quad (2)$$

where I is the peak value of the currents.

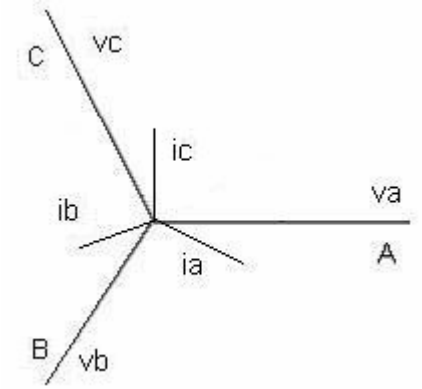


Figure 2.21 Three-phase power system phasor diagram

In matrix format, the voltage and current can be expressed as:

$$\bar{v} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \quad \bar{i} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3}$$

Transform the a-b-c system variables into the stationary two axis α - β system as in Figure 2.22. The voltage and current vectors rotate in this orthogonal axis system at the speed of ωt.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = [C_{\alpha\beta}] \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = [C_{\alpha\beta}] \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{4}$$

where, $[C_{\alpha\beta}] = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\sqrt{\frac{1}{6}} & -\sqrt{\frac{1}{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix}$.

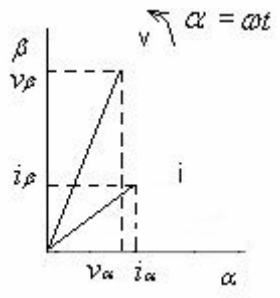


Figure 2.22 Voltage and current in the α - β system

It is clear that only the current component which is in phase with the voltage instantaneous component contribute to the real power. So, the instantaneous real power is defined as:

$$p = v_\alpha i_\alpha + v_\beta i_\beta \tag{5}$$

Likewise, the reactive power is defined as:

$$q = v_\alpha i_\beta - v_\beta i_\alpha \tag{6}$$

Furthermore, transform the variables in α-β system into the rotating two axes d-q system as in Figure 2.23. In this co-ordinate system, the d axis is always coincident with the instantaneous voltage vector. And the q axis is in quadrature with the d axis. The d axis and q axis rotate at the speed of ωt. In this axis system, the voltage and the current vector are stationary compared with the d and q axis.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = [C_{dq}] \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}, \quad \begin{bmatrix} i_d \\ i_q \end{bmatrix} = [C_{dq}] \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{7}$$

where, $[C_{dq}] = \begin{bmatrix} \cos\alpha & \sin\alpha \\ -\sin\alpha & \cos\alpha \end{bmatrix}$, α is the phase angle of the voltage.

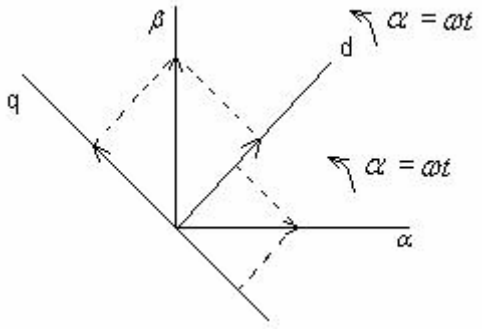


Figure 2.23 Voltage and current in the d-q system

After d-q transformation, the real and reactive power can be derived as: $p = v_d i_d$, $q = v_d i_q$, where, $v_d = |v|$, $v_q = 0$. By performing d-q transformation, the real and reactive power, thus the real and reactive current can be processed independently. The control algorithm can be greatly simplified.

2.3.2 Single phase instantaneous power

The instantaneous power defined in the previous section is based on balanced three-phase system. For a single-phase system, it is possible to use the same method by constructing a three phase system from the single phase variables.

Method 1: Suppose v_s, i_s are the sampled single phase voltage and current. Let $v_a = v_s$, $i_a = i_s$. By delaying v_s, i_s 120^0 and 240^0, we can get v_b, i_b, and v_c, i_c. Perform the same transformation as in 2.3.1, the magnitude of the single phase voltage can be obtained. So are the real and reactive current and power. In this method, there is a 240^0 delay.

$$\begin{cases} v_a = V_s \cos(\omega t) \\ v_b = V_s \cos(\omega t - 120^0) \\ v_c = V_s \cos(\omega t - 240^0) \end{cases} \quad (8)$$

$$\begin{cases} i_a = I_s \cos(\omega t - \theta) \\ i_b = I_s \cos(\omega t - \theta - 120^0) \\ i_c = I_s \cos(\omega t - \theta - 240^0) \end{cases} \quad (9)$$

Method 2: Let $v_a = v_s$, $i_a = i_s$. The value we get by delaying v_s, i_s 60^0 is negative the value by delaying v_s, i_s 240^0. So, by delaying v_s, i_s 60^0, we get $-v_c$, $-i_c$. Then, $v_b = -v_a - v_c$, $i_b = -i_a - i_c$. In this construction method, there is only 60^0 delay [107].

It is difficult for an analog circuit to realize the construction of three-phase system from single-phase signals. However, by utilizing microcontroller and digital signal processor, the delaying function can be implemented easily, fast, and precisely.

2.4 Control of a centralized unified power flow controller

Generally, control of the CUPFC is developed from vector control, which is based on the d-q transformation. This method was used in STATCOM control [108]. In [109], the vector-control was used to build a control structure for the CUPFC. An additional predictive control loop and a pre-control signal for a dc voltage control was used to increase the stability and improve the transient system performance. A fundamental frequency model was developed in [110] for simulation on EMTP. In [111], real and reactive power between the shunt and the

series converter was coordinated to improve the transient performance of the CUPFC.

Depending on the purpose of the operation, the UPFC has several operating modes. For the shunt converter, the current was controlled by the request of real power from the series device and the power losses in the switching devices and the capacitor, and the reactive power request from control to absorb or provide reactive power from the sending end or the point of connection. The shunt converter can have VAR control mode and automatic voltage control mode.

In the VAR control mode, the shunt converter is controlled to draw an inductive or capacitive VAR requested by reference command, by controlling proper gating signals for the switching devices. The feedback to the shunt converter is the shunt converter current. At the same time, the shunt converter keeps the DC capacitor voltage constant.

In the automatic voltage control mode, the shunt converter is controlled to keep the voltage at the point of connection to be in a certain range. The feedback signal to the shunt converter is the voltage at the POC.

The series converter controls the line power flow by injecting proper voltage in series with the transmission line. In different operating conditions, the series converter has the following different working modes:

1. Direct voltage injection mode: In this mode, the magnitude and phase angle of the series converter is controlled to follow the reference values.

2. Phase angle shifter emulation mode: In this mode, the series inverter injects a voltage to control the line voltage to have a specified phase angle shift.

3. Line impedance emulation mode: In this mode, the series injected voltage is controlled to be proportional to the line current. The result is that the series device is effectively a variable complex impedance.

4. Automatic power flow control mode: This is a unique function mode for the UPFC in which the line real and reactive power can be controlled automatically by the series device. The real and reactive current reference is computed from reference power command. The control system senses the line current as the feed back signal. In this control mode, the d-q transformation is used to separately control the real and reactive current as an effective control scheme in realizing the control function.

In most cases, the UPFC would be used in automatic voltage control mode for the shunt converter, and automatic power flow control mode for the series converter. In this mode, the UPFC control the voltage magnitude at the point of connection by locally generating or absorbing the reactive power. At the same time, the line transmitted power is controlled by controlling the magnitude and phase angle of the series injected voltage. This control mode is the most advantageous compared with other types of FACTS devices. The proposed DUPFC concept and control scheme is based on this control mode as a complete system.

Figure 2.24 shows a typical control scheme for the UPFC system. The system control accepts operator input and power system real data. Based on the operator inputs and the power system data, the system control generates reference signals for the functional control block. The reference signals include the magnitude of the voltage at the point of connection, the real and reactive transmission line power, and other reference signals. The functional control block use these reference signals and the real time local electric data feedback, including the shunt converter current, series converter output voltage, and the DC capacitor voltage, to generate current reference for the converter control block and the voltage

reference for the series converter control block. The converter control blocks use appropriate reference from the functional control block and the power system to produce proper gating signals for the switching devices in the two converters.

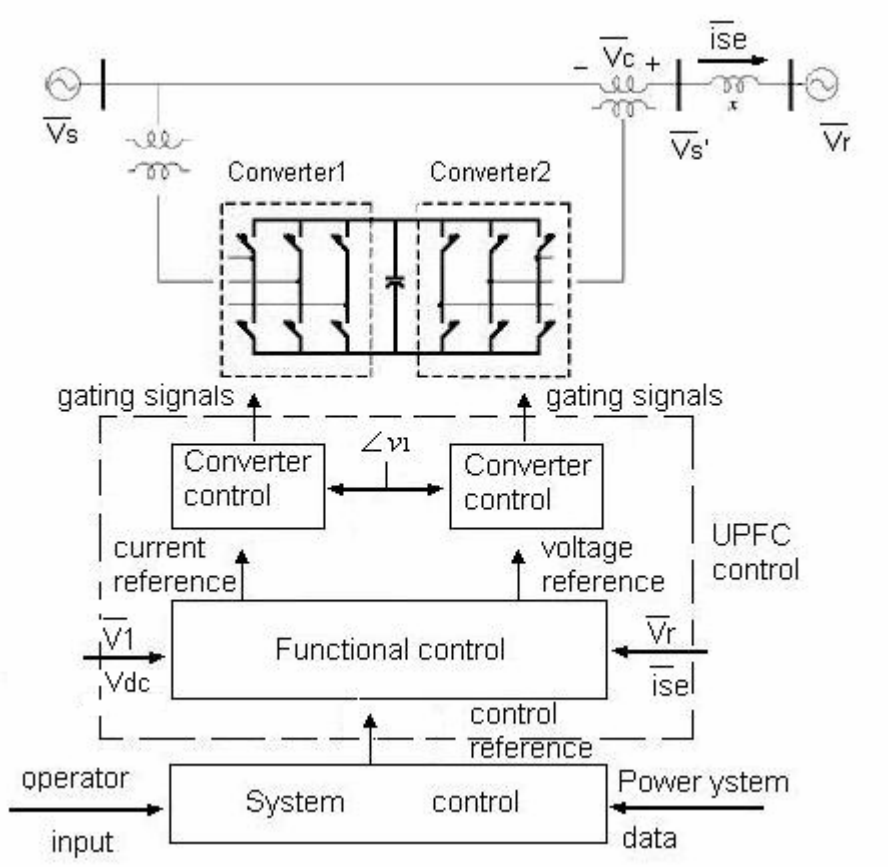


Figure 2.24 Typical UPFC control system hierarchy [5]

2.4.1 Control variable references for the functional control

This section describes how the system control block uses operator inputs (control command) and the power system data to compute the reference signals for the functional control block. **By default, variables with star symbol (*) as superscript are reference signals.**

A typical unified power flow controller is depicted as in Figure 2.25. Control objectives in the system are the voltage magnitude $|v_1|$ and the transmission line

real and reactive power flow P and Q. $|v_1|$ is controlled by the shunt device by injecting leading or lagging current into the point of connection. The effect is illustrated as arrow 1 in Figure 2.25. System power flow P and Q are controlled by the series device by injecting proper voltage into the transmission line. The series device exchanges real and reactive power with the system. The reactive power is exchanged locally with the DC capacitor bank, depicted as arrow 2 in the figure. The active power the series device injected into the line is drawn from the shunt device via the DC capacitor bank. The real power flow is illustrated by the arrow 3 pair in the diagram.

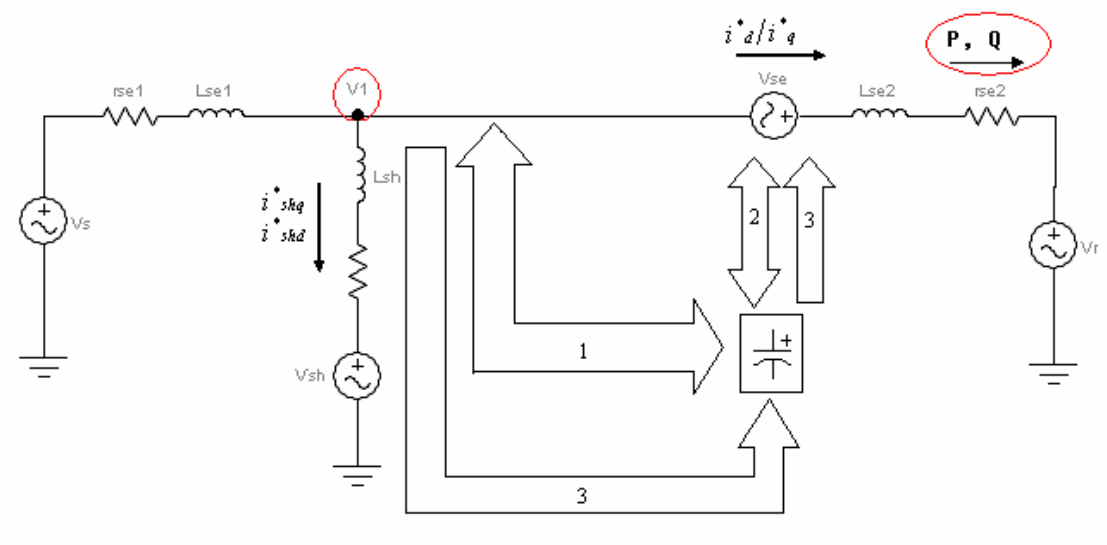


Figure 2.25 Power flow in a unified power flow controller

(2) Series converter reference

By d-q transformation, the transmitted real and reactive power to the receiving end bus is controlled independently. In d-q axis for the three phase system, $p = v_{rd}i_d$, $q = v_{rd}i_q$, where v_{rd} is the d axis component of the receiving end voltage. i_d and i_q are real and reactive components of the line current respectively. So, the d-axis and q-axis reference current in the transmission line are calculated as equation (10). The computation process is depicted as Figure 2.26.

$$\begin{cases} i^*_d = \dfrac{p^*}{v_{rd}} \\ i^*_q = \dfrac{q^*}{v_{rd}} \end{cases} \tag{10}$$

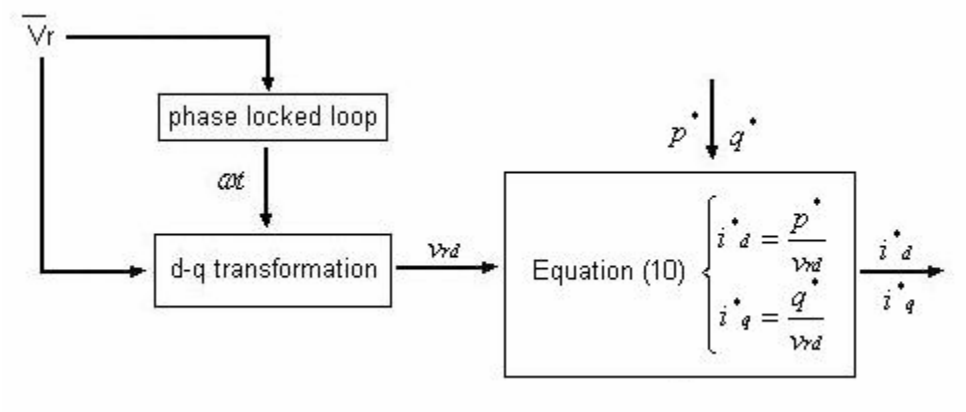


Figure 2.26 Series current reference computation

(3) Shunt converter reference

Magnitude of the sending end bus voltage v_1 is controlled by shunt device reactive power injection. So, the reactive injection power q_{sh} can be controlled by a PI controller. Reference value of q_{sh} is:

$$q^*_{sh} = (\frac{K_{iv}}{s} + k_{pv})\ (|v_1|^* - |v_1|) \tag{11}$$

where $|v_1|^*$ is the sending end voltage magnitude reference, and $|v_1|$ the real time voltage magnitude. K_{iv} and K_{pv} are the integral and the proportional gain for the PI controller. If the rotating axis is synchronous with the sending end voltage, the d axis component of the voltage is the instant magnitude of the voltage. So, $|v_1| = v_{1d}$.

Then, the q-axis reference current in the shunt branch should be:

$$i^*_{shq} = \frac{q^*_{sh}}{v_{1d}} \tag{12}$$

The d-axis reference current for the shunt branch is decided by the active power p_{se} drawn by the series device. At the same time, the real component of the shunt converter current is responsible of providing power losses in the switching devices and the DC capacitor. This is reflected by keeping the DC capacitor voltage constant. So,

$$i^*_{shd} = \frac{p^*_{se}}{v_{1d}} + (k_{pDC} + \frac{k_{iDC}}{s})(V^*_{DC} - V_{DC}) \quad (13)$$

where v_{1d} is the d axis component of the voltage at the point of connection. $p^*_{se} = v_{sed}i_{sed} + v_{seq}i_{seq}$ is the instantaneous real power injected into the transmission line by the series converter. v_{sed} is the real component of the injected voltage. i_{sed} and i_{seq} are the real and reactive components of the line current respectively. k_{iDC} and k_{pDC} are the integral and the proportional gain for the PI controller. The real power drawn by the series converter is supplied by the shunt converter through the DC capacitor.

The shunt current reference computation process is illustrated in Figure 2.27.

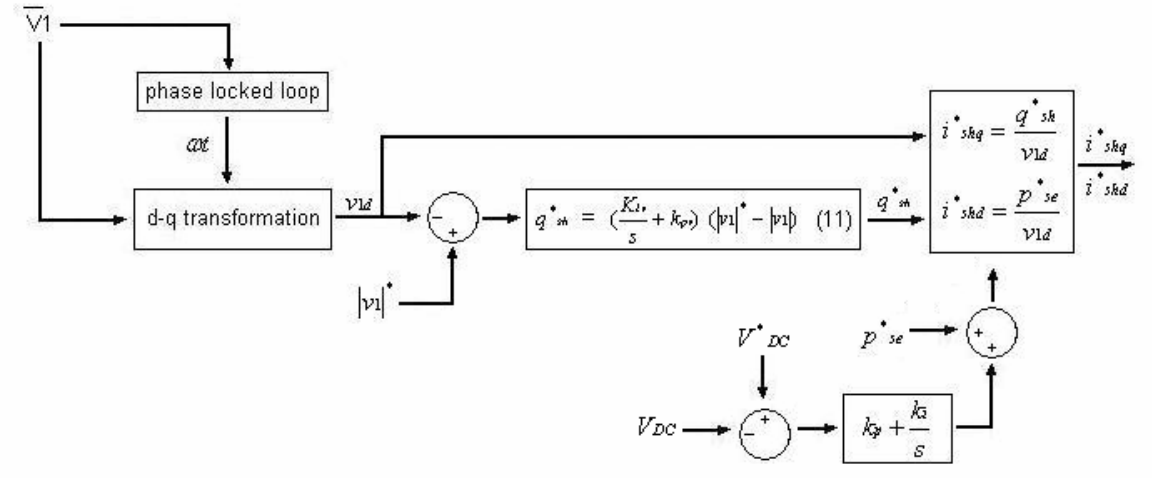


Figure 2.27 Shunt current reference computation

Here, the DC capacitor bank is assumed to be an ideal capacitor. In practice, the capacitor has Equivalent Series Resistance (ESR). The power loss due to ESR is also compensated by the shunt device.

2.4.2 UPFC state space equation

The series device for a balanced three phase system is modeled on a per phase basis as a voltage source with series resistance R and inductance L as in Figure 2.28.

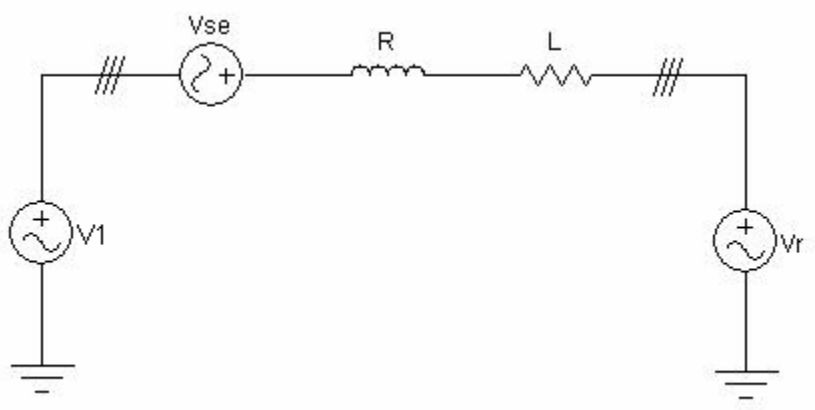


Figure 2.28 Series device model

The resulting three-phase circuit equation set can be written as:

$$\begin{cases} v_{1a} + v_{sea} - v_{ra} = Ri_a + L\dfrac{d}{dt}i_a \\ v_{1b} + v_{seb} - v_{rb} = Ri_b + L\dfrac{d}{dt}i_b \\ v_{1c} + v_{\sec} - v_{rc} = Ri_c + L\dfrac{d}{dt}i_c \end{cases} \tag{14}$$

Organize equation (14) into matrix format:

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} -\dfrac{R}{L} & 0 & 0 \\ 0 & -\dfrac{R}{L} & 0 \\ 0 & 0 & -\dfrac{R}{L} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_{1a} + v_{sea} - v_{ra} \\ v_{1b} + v_{seb} - v_{rb} \\ v_{1c} + v_{\sec} - v_{rc} \end{bmatrix} \tag{15}$$

Transform the equation (15) into d-q axis system:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega \\ -\omega & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_{1d} + v_{sed} - v_{rd} \\ v_{1q} + v_{seq} - v_{rq} \end{bmatrix} \tag{16}$$

Shunt device modeled as a voltage source is depicted as in Figure 2.29, with series resistance r_{sh} and inductance L_{sh}.

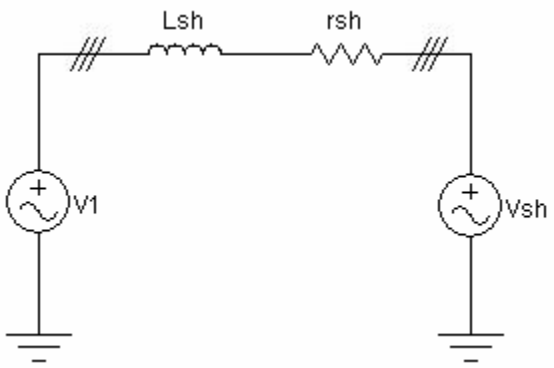


Figure 2.29 Shunt device model

In a-b-c axis system, the circuit equation is written as:

$$\begin{cases} v_{1a} - v_{sha} = r_{sh} i_{sha} + L_{sh}\frac{d}{dt} i_{sha} \\ v_{1b} - v_{shb} = r_{sh} i_{shb} + L_{sh}\frac{d}{dt} i_{shb} \\ v_{1b} - v_{shb} = r_{sh} i_{shb} + L_{sh}\frac{d}{dt} i_{shb} \end{cases} \tag{17}$$

In matrix format, the equation (17) can be organized as:

$$\frac{d}{dt}\begin{bmatrix} i_{ash} \\ i_{shb} \\ i_{shc} \end{bmatrix} = \begin{bmatrix} -\frac{R_{sh}}{L_{sh}} & 0 & 0 \\ 0 & -\frac{R_{sh}}{L_{sh}} & 0 \\ 0 & 0 & -\frac{R_{sh}}{L_{sh}} \end{bmatrix}\begin{bmatrix} i_{sha} \\ i_{shb} \\ i_{shc} \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_{1a} - v_{sha} \\ v_{1b} - v_{shb} \\ v_{1c} - v_{shc} \end{bmatrix} \tag{18}$$

Transform the equation (18) into d-q-0 system:

$$\frac{d}{dt}\begin{bmatrix} i_{shd} \\ i_{shq} \end{bmatrix} = \begin{bmatrix} -\frac{R_{sh}}{L_{sh}} & \omega \\ -\omega & -\frac{R_{sh}}{L_{sh}} \end{bmatrix}\begin{bmatrix} i_{shd} \\ i_{shq} \end{bmatrix} + \frac{1}{L_{sh}}\begin{bmatrix} v_{1d} - v_{shd} \\ v_{1q} - v_{shq} \end{bmatrix} \quad (19)$$

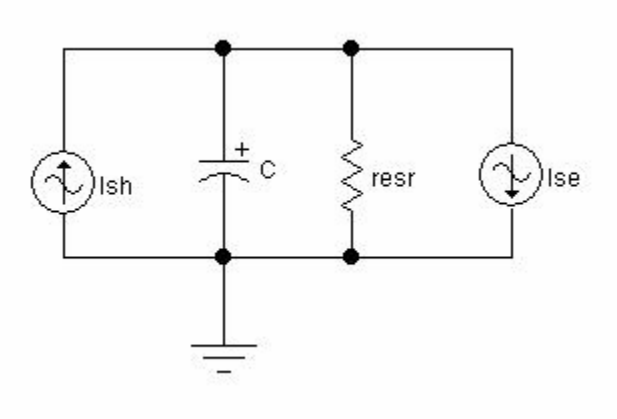


Figure 2.30 DC capacitor voltage control model

The losses of the shunt device, series device, and the DC capacitor are modeled as a shunt connected resistance with the DC capacitor. The model is shown in Figure 2.30. The voltage of the DC capacitor bank is decided by the real power drawn and injected by the shunt and series devices. The node current at the positive of the capacitor can be written as:

$$i_{sh} - i_{se} = C\frac{dv_{DC}}{dt} + \frac{v_{DC}}{r_{esr}} \quad (20)$$

where i_{sh} and i_{se} are the currents drawn by the shunt and series converter respectively. The currents are decided by the real power drawn or provided by the shunt and series devices. So, equation (20) can be revised as:

$$\frac{p_{sh} - p_{se}}{v_{DC}} = C\frac{dv_{DC}}{dt} + \frac{v_{DC}}{r_{esr}} \quad (21)$$

The real power provided by the shunt converter is expressed as equation (22). The d-q rotating axis is synchronous with the voltage v_1. So, the q-axis voltage component of the voltage is 0.

$$p_{sh} = v_{1d}i_{shd} + v_{1q}i_{shq} \quad (22)$$

The real power drawn by the series converter is written as in equation (23). The d-q rotating axis is synchronous with the receiving end voltage v_r.

$$p_{se} = v_{sed} i_{sed} + v_{seq} i_{seq} \tag{23}$$

Substitute equations (22) and (23) into equation (21), we get.

$$\frac{v_{1d} i_{shd} + v_{1q} i_{shq} - v_{sed} i_{sed} - v_{seq} i_{seq}}{v_{DC}} = C \frac{dv_{DC}}{dt} + \frac{v_{DC}}{r_{esr}} \tag{24}$$

Reorganize the equation as:

$$\frac{dv_{DC}}{dt} = \frac{v_{1d} i_{shd} - v_{sed} i_{sed} - v_{seq} i_{seq}}{C v_{DC}} - \frac{v_{DC}}{C r_{esr}} \tag{25}$$

Neglecting the voltage harmonics due to the inverter switching, the shunt and series converter output voltage d-q components can be expressed as:

$$\begin{bmatrix} v_{shd} \\ v_{shq} \\ v_{sed} \\ v_{seq} \end{bmatrix} = v_{DC} \begin{bmatrix} k_{sh} \cos(\delta_{sh}) \\ k_{sh} \sin(\delta_{sh}) \\ k_{se} \cos(\delta_{se}) \\ k_{se} \sin(\delta_{se}) \end{bmatrix} \tag{26}$$

where k_{sh} and k_{se} are the constants for the relationship of the shunt and series converter versus the DC voltage. It integrates the transformer turns ratio and the modulation index of the shunt and series converter. δ_{sh} and δ_{se} are the phase angle of the shunt and series converter output fundamental voltage with respect to reference voltage, normally the sending or receiving end bus voltage.

Substitute (26) into (25), we get:

$$\frac{dv_{DC}}{dt} = \frac{3k_{sh} \cos(\delta_{sh}) + k_{sh} \sin(\delta_{sh}) - k_{se} \cos(\delta_{se}) - k_{se} \sin(\delta_{se})}{2C} - \frac{v_{DC}}{C r_{ser}} \tag{27}$$

Combining equation (16), (19), and (27), we can get the UPFC state space equation as:

$$\dot{x} = Ax + Bu \tag{28}$$

where

$$x = \begin{bmatrix} i_{shd} \\ i_{shq} \\ i_{sed} \\ i_{seq} \\ v_{dc} \end{bmatrix},$$

$$A = \begin{bmatrix} -\frac{R_{sh}}{L_{sh}} & \omega & 0 & 0 & \frac{1}{L_{sh}} k_{sh}\cos(\delta_{sh}) \\ -\omega & -\frac{R_{sh}}{L_{sh}} & 0 & 0 & \frac{1}{L_{sh}} k_{sh}\sin(\delta_{sh}) \\ 0 & 0 & -\frac{R}{L} & \omega & -\frac{1}{L} k_{se}\cos(\delta_{se}) \\ 0 & 0 & -\omega & -\frac{R}{L} & -\frac{1}{L} k_{se}\sin(\delta_{se}) \\ \frac{3}{2C} k_{sh}\cos(\delta_{sh}) & \frac{3}{2C} k_{sh}\sin(\delta_{sh}) & \frac{3}{2C} k_{se}\cos(\delta_{se}) & \frac{3}{2C} k_{se}\sin(\delta_{se}) & \frac{1}{Cr_{ser}} \end{bmatrix},$$

$$\text{And, } B = \begin{bmatrix} \frac{1}{L_{sh}} v_{1d} \\ \frac{1}{L_{sh}} v_{1q} \\ \frac{1}{L}(v_{s1d} - v_{rd}) \\ \frac{1}{L}(v_{1q} - v_{rq}) \\ v_{dc} \end{bmatrix}$$

The output function is:

$$Y = Cx \tag{29}$$

Where

$$Y = \begin{bmatrix} y_1 \\ y_2 \\ y_3 \\ y_4 \end{bmatrix}$$

$$\text{And, } C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

The state equation of the UPFC is non-linear. To simplify the problem, we assume the DC capacitor is large, which means the DC capacitor voltage can be seen as a constant. The state equation (28) can be simplified into a forth order system:

$\dot{x}$ = Ax+Bu (30)

where

$$x = \begin{bmatrix} i_{shd} \\ i_{shq} \\ i_{sed} \\ i_{sed} \end{bmatrix}$$

$$A = \begin{bmatrix} -\frac{R_{sh}}{L_{sh}} & \omega & 0 & 0 \\ -\omega & -\frac{R_{sh}}{L_{sh}} & 0 & 0 \\ 0 & 0 & -\frac{R}{L} & \omega \\ 0 & 0 & -\omega & -\frac{R}{L} \end{bmatrix}$$

This state space equation is already decoupled. The series and the shunt converter control can be dealt with separately if issues of transient response compensation were to be addressed.

2.4.3 Series device control

In the transformation of the series device state space equation, the rotating axis is synchronous with the receiving end voltage v_r. So, $v_{rd} = |v_r|$, $v_{rq} = 0$. Equation (16) can be reorganized as the following form:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_{1d} + v_{sed} - v_{rd} + \omega L i_q \\ v_{1q} + v_{seq} - \omega L i_d \end{bmatrix} \quad (31)$$

Denote:

$$\begin{cases} u_1 = \dfrac{1}{L}(v_{1d} + v_{sed} - v_{rd} + \omega L i_q) \\ u_2 = \dfrac{1}{L}(v_{1q} + v_{seq} + \omega L i_d) \end{cases} \tag{32}$$

Then, the equation (31) can be written as:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\dfrac{R}{L} & 0 \\ 0 & -\dfrac{R}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} \tag{33}$$

Let:

$$\begin{cases} u_1 = (\dfrac{K_i}{s} + K_p)(i^*_d - i_d) + \omega L i_q \\ u_2 = (\dfrac{K_i}{s} + K_p)(i^*_q - i_q) + \omega L i_d \end{cases} \tag{34}$$

where i^*_d is the d axis reference, thus the active component reference of the CUPFC series current. i^*_q is the reactive component of the series current. Values of those two variables are computed in equation (10).

Then, the voltage reference of the output of the series converter is:

$$\begin{bmatrix} v^*_{sed} \\ v^*_{seq} \end{bmatrix} = \begin{bmatrix} k_{pse} + \dfrac{k_{ise}}{s} & 0 \\ 0 & k_{pse} + \dfrac{k_{ise}}{s} \end{bmatrix}\begin{bmatrix} i^*_d - i_d \\ i^*_q - i_q \end{bmatrix} + \begin{bmatrix} v_{1d} - v_{rd} - \omega i_q \\ -v_{1q} + \omega i_d \end{bmatrix} \tag{35}$$

The series converter control diagram is shown in Figure 2.31.

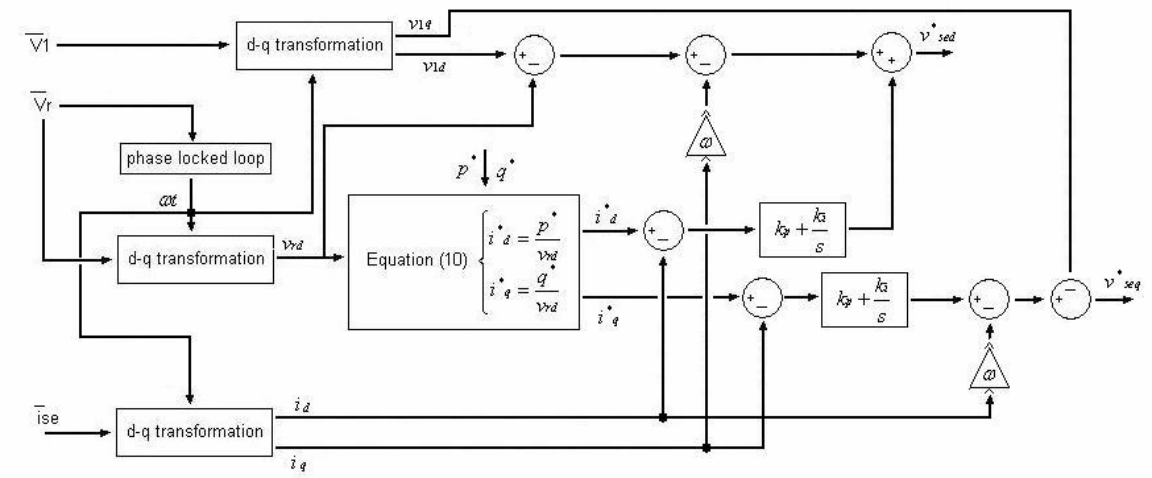


Figure 2.31 Series converter control

2.4.4 Shunt device control

In the transformation, the rotary d-q axis is synchronized to the connection point voltage v_1. So, $v_{1d} = |v_1|$, $v_{1q} = 0$. Reorganize equation (19) into the following form:

$$\frac{d}{dt}\begin{bmatrix} i_{shd} \\ i_{shq} \end{bmatrix} = \begin{bmatrix} -\frac{R_{sh}}{L_{sh}} & 0 \\ 0 & -\frac{R_{sh}}{L_{sh}} \end{bmatrix}\begin{bmatrix} i_{shd} \\ i_{shq} \end{bmatrix} + \frac{1}{L_{sh}}\begin{bmatrix} v_{1d} - v_{shd} + \omega L_{sh} i_{shq} \\ v_{shq} - \omega L_{sh} i_{shd} \end{bmatrix} \tag{36}$$

Denote:

$$\begin{cases} u_1 = \frac{1}{L_{sh}}(v_{1d} - v_{shd} + \omega L_{sh} i_{shq}) \\ u_2 = \frac{1}{L}(v_{1q} + v_{shq} - \omega L_{sh} i_{shd}) \end{cases} \tag{37}$$

Then, the equation (36) can be written as:

$$\frac{d}{dt}\begin{bmatrix} i_{shd} \\ i_{shq} \end{bmatrix} = \begin{bmatrix} -\frac{R_{sh}}{L_{sh}} & 0 \\ 0 & -\frac{R_{sh}}{L_{sh}} \end{bmatrix}\begin{bmatrix} i_{shd} \\ i_{shq} \end{bmatrix} + \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} \tag{38}$$

Let:

$$\begin{cases} u_1 = (\dfrac{K_{ish}}{s} + K_{psh})(i^*_{shd} - i_{shd}) + \omega L_{sh} i_{shq} \\ u_2 = (\dfrac{K_{ish}}{s} + K_{psh})(i^*_{shq} - i_{shq}) + \omega L_{sh} i_{shd} \end{cases} \tag{39}$$

where i^*_{shd} is the d axis reference, thus the active component reference of the CUPFC series current. i^*_{shq} is the reactive component of the series current. Values of those two variables are computed in equation (10).

The reference of the output of the shunt converter is:

$$\begin{bmatrix} v^*_{shd} \\ v^*_{shq} \end{bmatrix} = \begin{bmatrix} k_{psh} + \dfrac{k_{ish}}{s} & 0 \\ 0 & k_{psh} + \dfrac{k_{ish}}{s} \end{bmatrix} \begin{bmatrix} i^*_{shd} - i_{shd} \\ i^*_{shq} - i_{shq} \end{bmatrix} + \begin{bmatrix} v_{1d} + \omega i_{shq} \\ -\omega i_{shd} \end{bmatrix} \tag{40}$$

The shunt converter control diagram is illustrated in Figure 2.32.

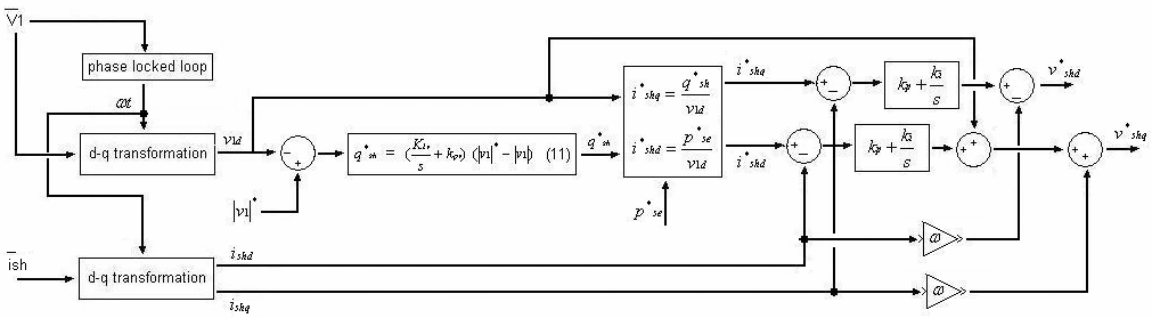


Figure 2.32 Shunt converter control

2.5 Control of the proposed DUPFC

The proposed DUPFC system mainly focuses on steady-state transmission line power flow control. At the same time, the voltage profile along the transmission line can be monitored and controlled according to the transmission system requirement. The control of the proposed DUPFC system is based on the control schemes proposed for the CUPFC control. The shunt converter of every DUPFC unit works in VAR control mode, providing or absorbing predefined reactive power computed by the system control block. The series converter of the DUPFC units work in voltage injection mode, which inject voltages of certain

magnitude and phase angle calculated and distributed by higher control blocks. The vector-based d-q transformation is used to facilitate the direct control of the real and reactive current.

The control of the DUPFC is depicted as in Figure 2.33. The system control block computes the real and reactive power reference P_{ref} and Q_{ref}, the voltage magnitude reference V_{kref} for k_{th} bus along the transmission line, based on the operator's input and the measured power system data.

The functional control block calculates the necessary shunt reactive power and series injected voltage reference. The reference signals are calculated the same as in the CUPFC control in 2.4.1.

The shunt reactive power and series voltage distribution block distributes the total shunt reactive power to all the DUPFC units installed on the transmission line. It also distributes the series injected voltage to all the units. This distribution block should be the major control part of the whole DUPFC system. A proper algorithm should be designed to control and coordinate individual DUPFC units, to balance load between units, and to protect individual devices from overloading.

The converter control block accomplishes the local device control. It monitors the local electric variables, including the voltage at the point of connection, the shunt converter current, and the dc capacitor voltage. It uses the series injected voltage reference from the reference distribution block to produce proper gating signals for the series converter. It computes the active power the series device exchanges with the transmission line. It uses the assigned reactive power reference from the reference distribution block and the active power request from the series device to calculate the shunt device voltage reference. Then, it produces proper gating signals for the shunt converter.

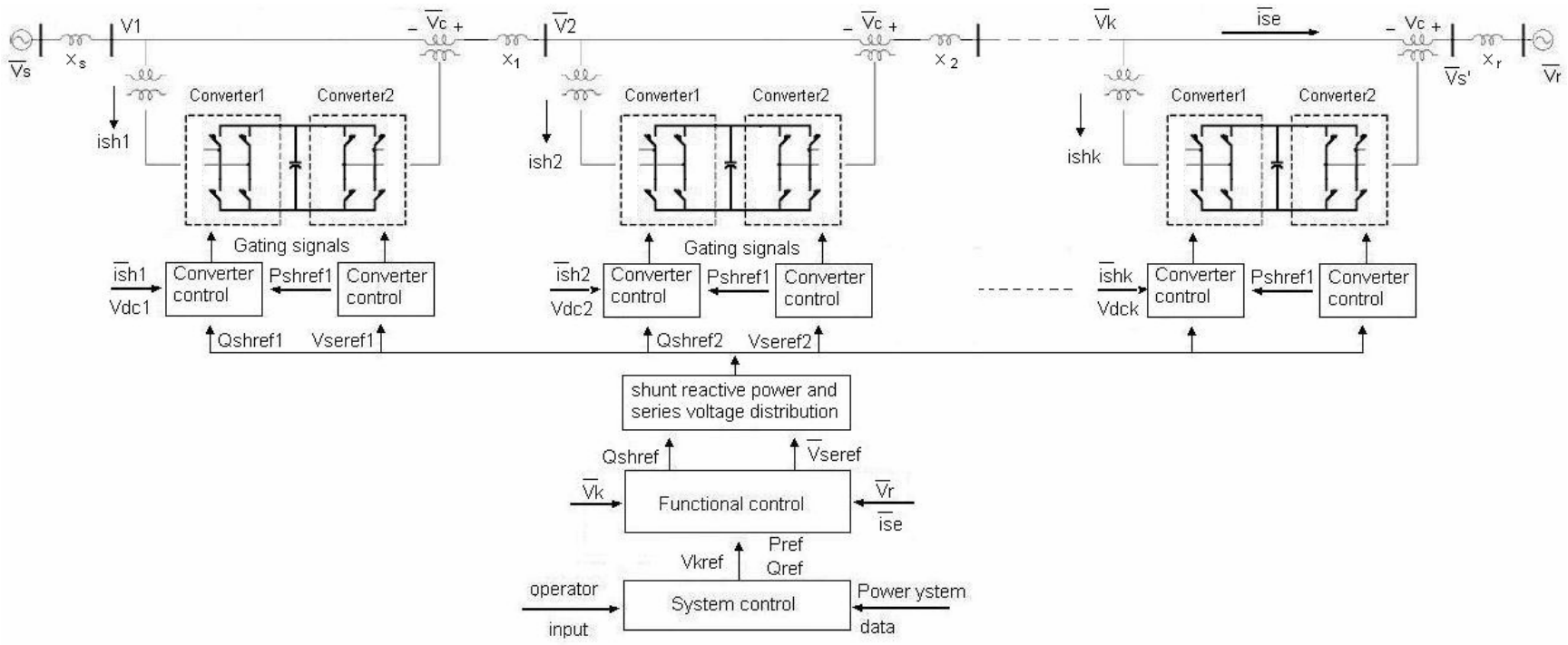


Figure 2.33 Control of the proposed DUPFC

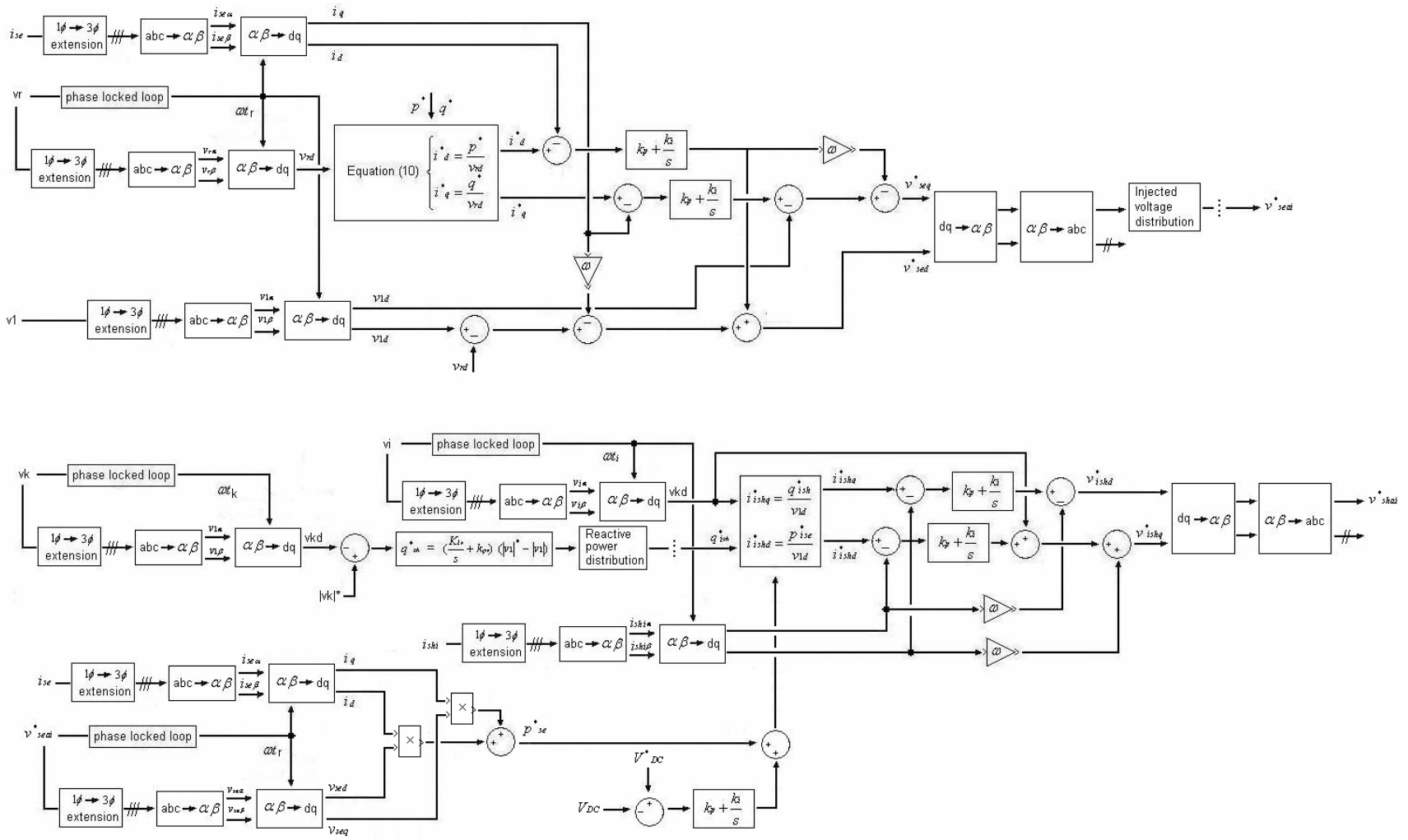


Figure 2.34 Detailed control algorithm of the proposed DUPFC

CHAPTER 3 SIMULATION RESULTS

In this section, the DUPFC model is created and simulated on Matlab/Simulink. A single unit unified power flow controller is simulated in section 3.1. And a control scheme of the distributed unified power flow controller is simulated in section 3.2. All the simulations are based on single-phase per-unit system.

3.1 Basic two-bus transmission line simulation

3.1.1 Basic transmission line model

A basic two-bus transmission line system is modeled in Simulink as in Figure 3.1. The transmission line is modeled as two sections, Tran_line_1 and Tran_line_2, for the sake of demonstrating two models of the transmission line.

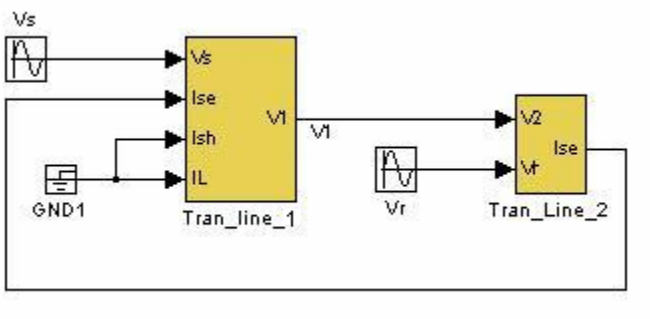


Figure 3.1 Basic two-bus transmission line system model

According to circuit theory, a section of transmission line can be modeled as a resistor and an inductor in series for simplicity. In the first line section, the equation for the input and output voltages, and the current through the transmission line can be written as:

$$v_s - v_1 = Ri_s + L\frac{di_s}{dt} \quad (1)$$

where v_s and v_1 are the input and out voltage respectively. R_{se} and L_{se} are transmission line resistance and inductance. i_s is the current through the sending end bus, and thus the current through the transmission line.

In Laplace form:

$$v_s(S) - v_1(S) = i_s(S)(R_{se} + sL_{se}) \quad (2)$$

So, the output of the transmission model is:

$$v_1(S) = v_s(S) - i_s(S)(R_{se} + sL_{se}) \quad (3)$$

In simulation, differentiation is vulnerable to noise. To increase the immunity and stability of the simulation model, a modified transfer function is used for the model of the inductance. The first transmission line section is modeled as Tran_line_1 as shown in Figure 3.2. The Ish, and IL are currents through shunt device and load connected to bus Vs. For the basic transmission model, they are temporarily connected to the ground.

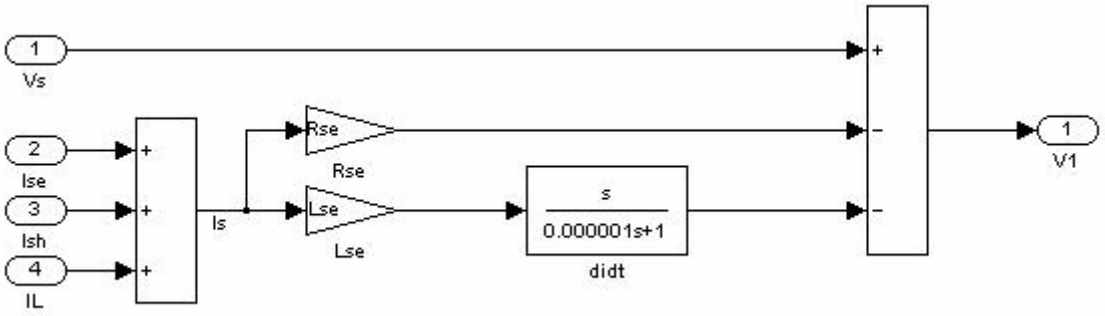


Figure 3.2 Transmission line section 1 model

For the transmission line section 2, the relationship between the voltages and the current is described as:

$$\frac{d}{dt} i_{se} = \frac{v_2 - v_r}{Lse} - \frac{R_{se}}{L_{se}} i_{se} \quad (4)$$

In Laplace form, equation (4) can be written as:

$$s i_{se}(s) + \frac{R_{se}}{L_{se}} i_{se}(s) = \frac{1}{L_{se}} (v_2(s) - v_r(s)) \quad (5)$$

where v_2 and v_r are the voltages across the transmission line. R_{se} and L_{se} are transmission line resistance and inductance. i_{se} is the current through the transmission line, and thus the current flowing into the receiving end bus. The second transmission line section is modeled as in Figure 3.3.

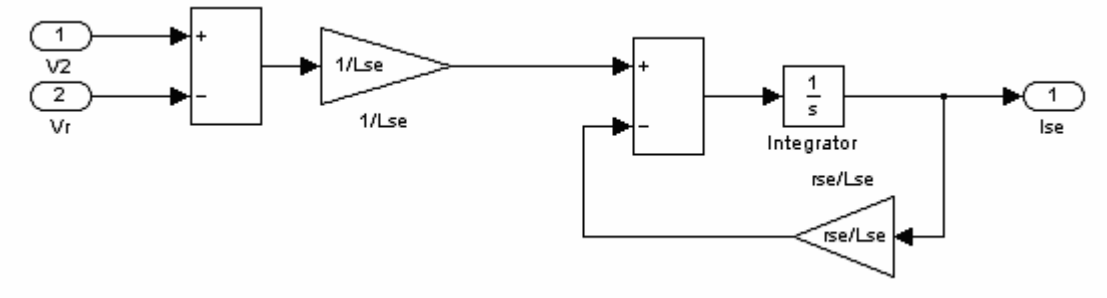


Figure 3.3 Transmission line section 2 model

3.1.2 Basic transmission line simulation

The two-bus transmission line is simulated as in Figure 3.4. In this simulation, the transmission line is divided into three sections, each having a per-unit resistance of 0.05 pu, and per-unit inductance of 0.1 pu. The first section models for the Thevenin equivalent impedance of the sending end bus. The third one models for the Thevenin equivalent impedance of the receiving end bus. The single phase variables are delayed to construct the three phase system. The construction block is shown in Figure 3.5. The instantaneous voltage magnitude and real and reactive power are measured, based on d-q transformation as derived in 2.3.1 and 2.3.2. The voltage and power measurement functional blocks are illustrated as in Figure 3.6 and Figure 3.7.

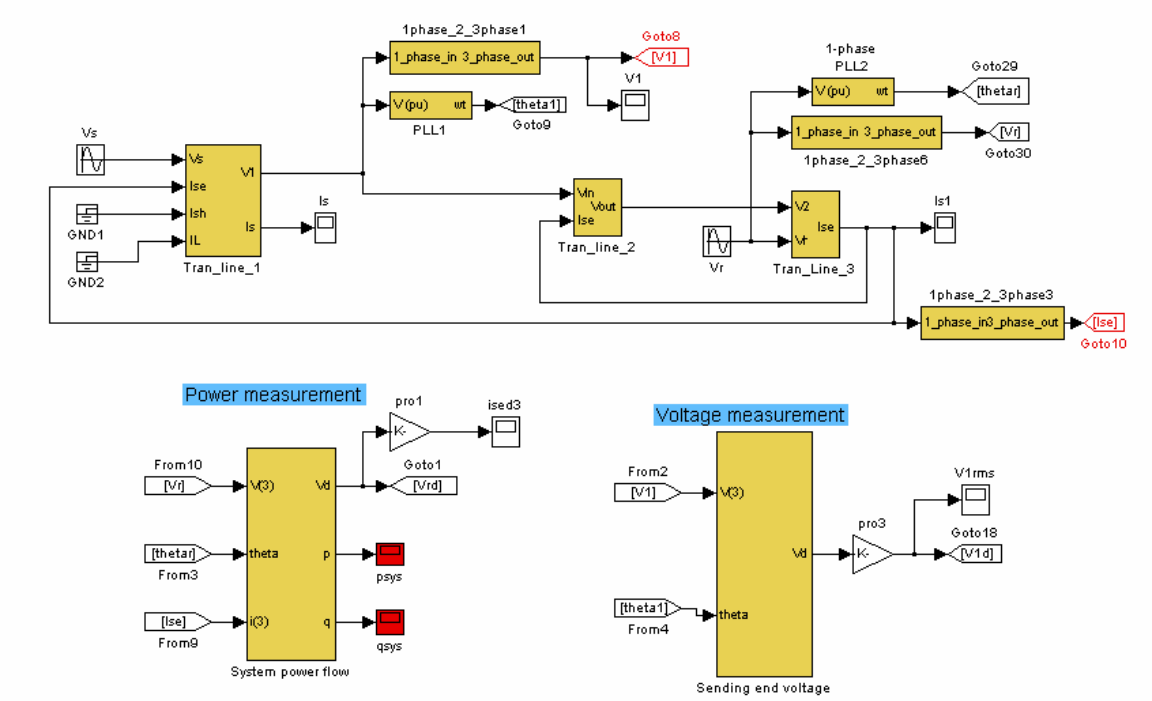


Figure 3.4 Basic two-bus system simulation block diagram

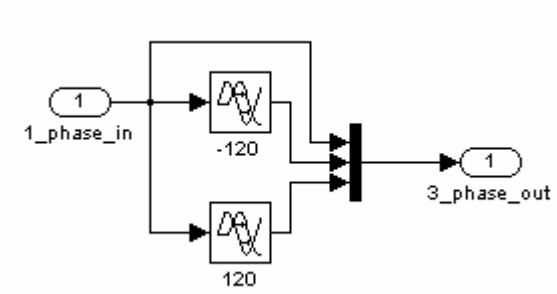


Figure 3.5 Three phase construction block

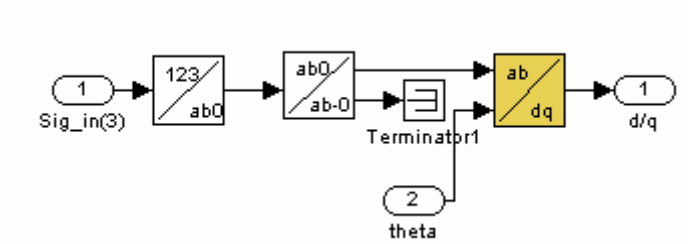


Figure 3.6 d-q transformation for voltage magnitude measurement

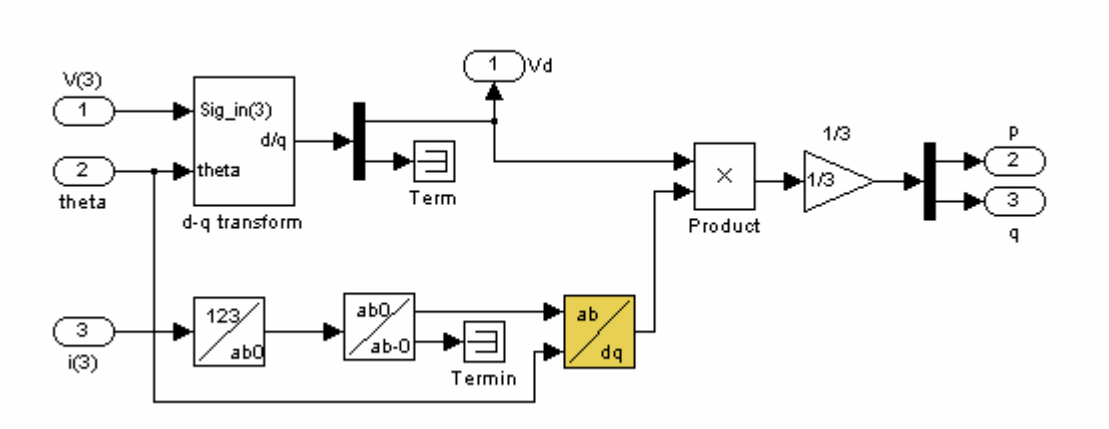


Figure 3.7 d-q transformation for real and reactive power measurement

The power circuit parameters are listed as in Table 3.1. Figure 3.8 depicts the real power flow at the receiving end bus. The reactive power at the receiving end bus is illustrated in Figure 3.9. The voltage magnitude at the sending end is shown in Figure 3.10. It can be seen that the real and reactive power transferred from the sending end to the receiving end bus are fixed as long as the parameters of the power system are fixed. To change the power flow along the transmission line, it is necessary to change the sending end and receiving end bus voltages, which is a normal practice. It is difficult to change the transmission line impedance after the transmission line has been set up. It is also noted that due to the construction delay of the three phase system from the single phase signals, the measured variables are not stable at the start-up of the simulation.

Table 3.1 two bus transmission line circuit parameters

V_1	V_r	R (per section)	xL (per section)
$1.1\angle 20^0$	$0.9\angle 0^0$	0.05	0.1

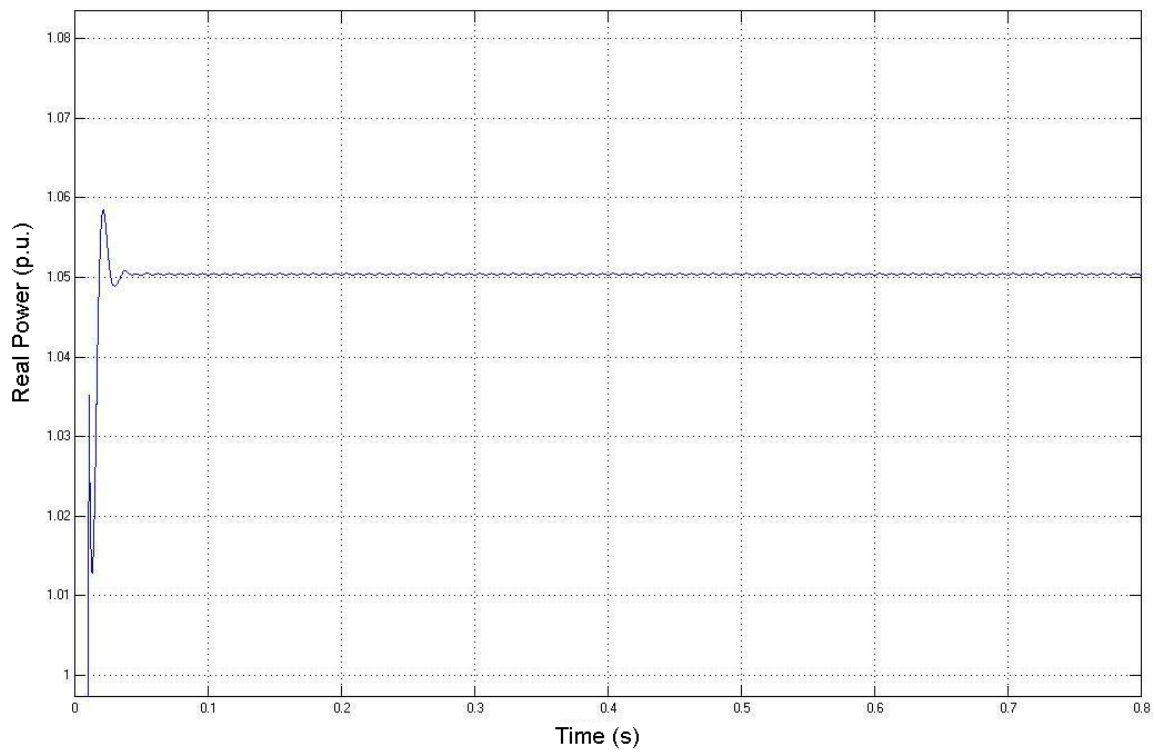


Figure 3.8 Real power flow to the receiving end bus for the basic two-bus system

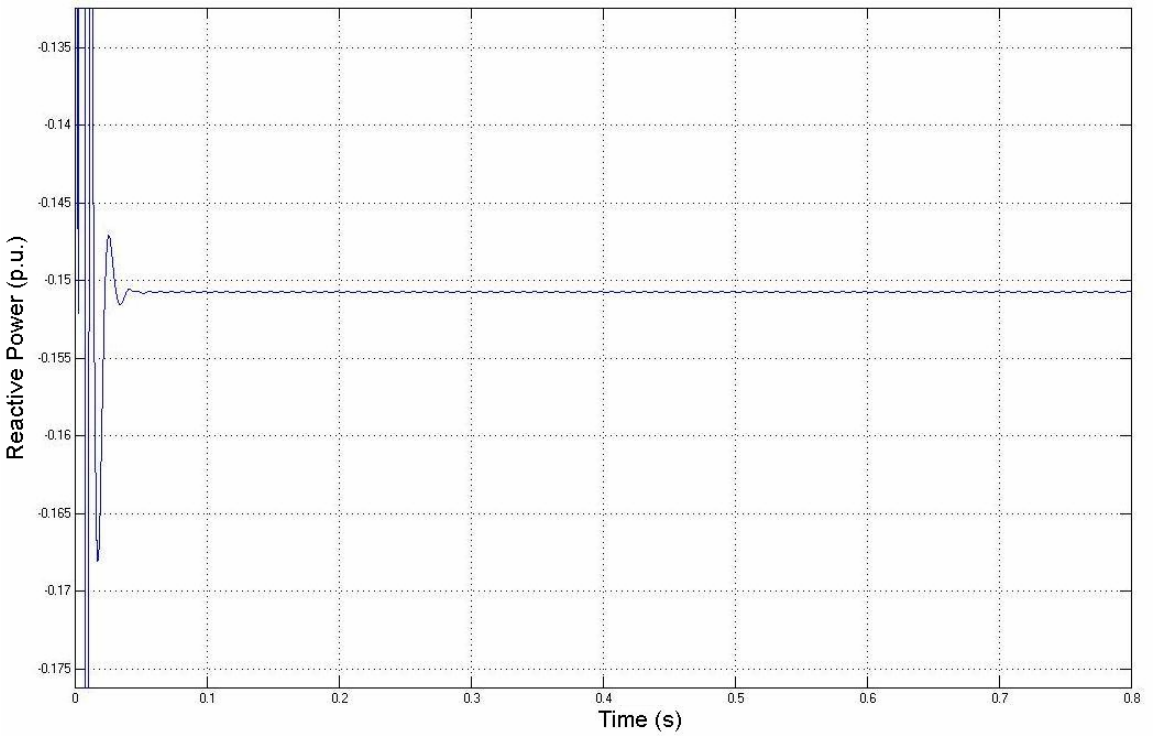


Figure 3.9 Reactive power flow at the receiving end bus

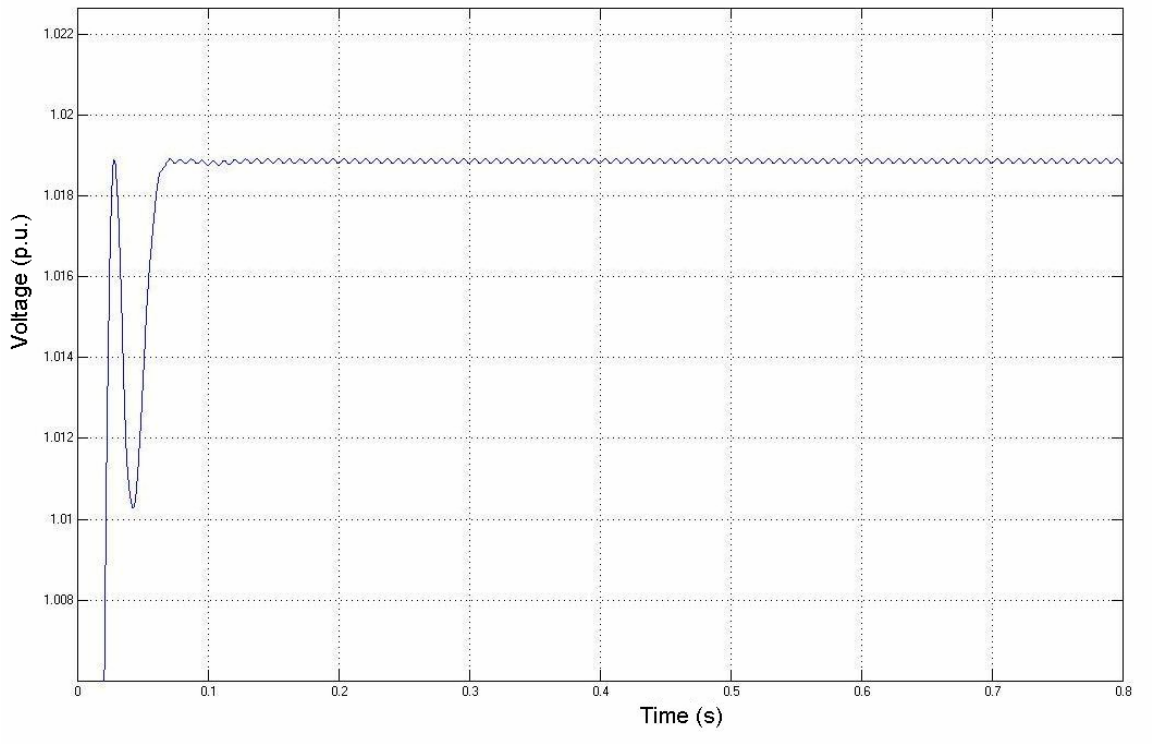


Figure 3.10 Sending end bus voltage

The sections 3.2 and 3.3 will demonstrate how the CUPFC and the proposed DUPFC system alter the transmission line profile, and thus the transmitted power.

3.2 Simulation of a CUPFC

3.2.1 Simulink model of a centralized unified power flow controller

A centralized unified power flow controller was inserted into the transmission line between the first and the second transmission line section as in Figure 3.11. Figure 3.12 shows the computation of the series and the shunt converter current reference. In calculating the series converter current reference, the d-axis component of the voltage is the receiving end voltage magnitude. While calculating the shunt converter reference, the d-axis component of the voltage is the voltage magnitude at the connection point. Figure 3.13 illustrates the shunt converter real and reactive power coordination. The real power requested by the shunt converter is the summation of the request from the series converter and the

DC capacitor. The reactive power request is decided by the voltage magnitude at the point of connection, as shown in Figure 3.14.

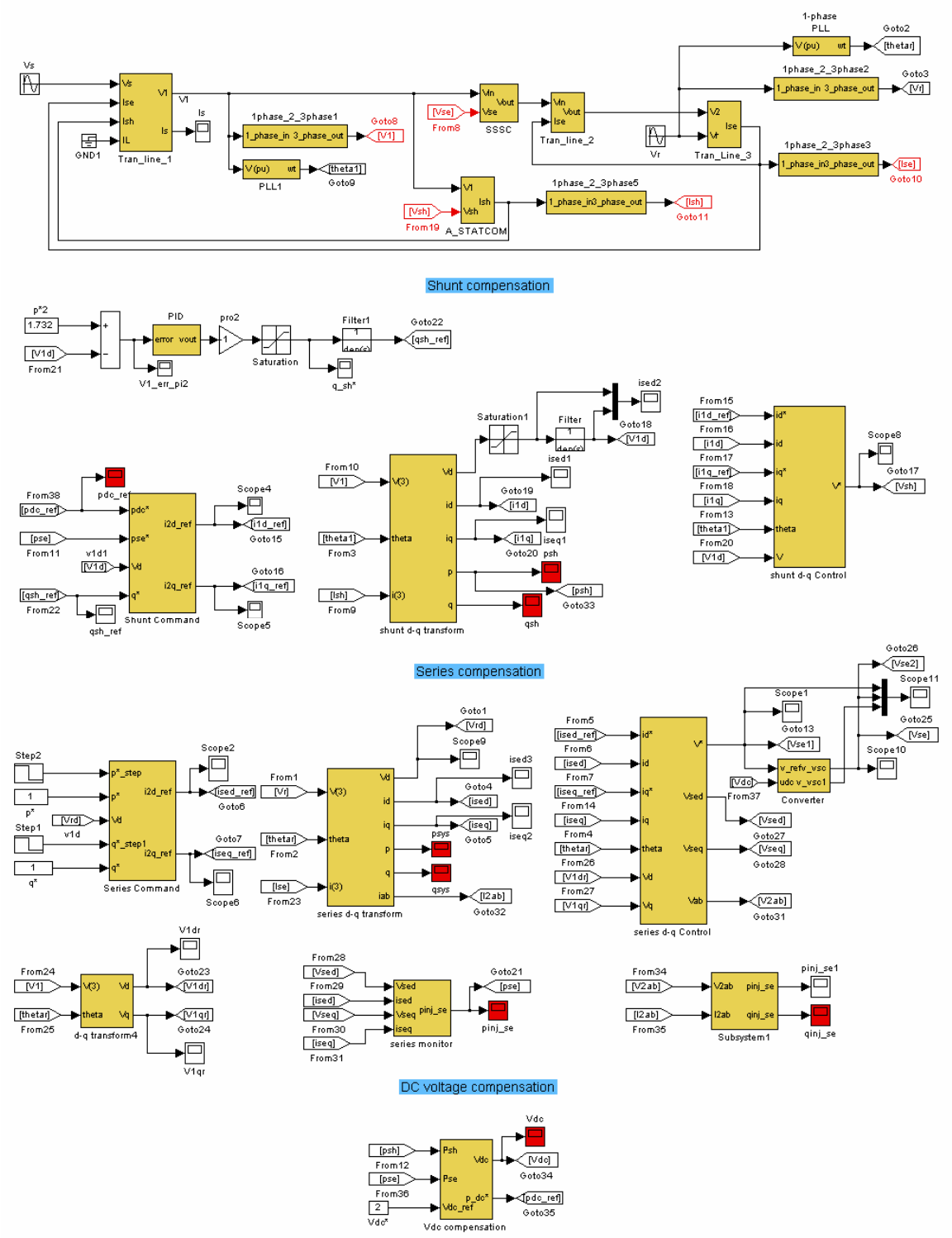


Figure 3.11 CUPFC Simulink model

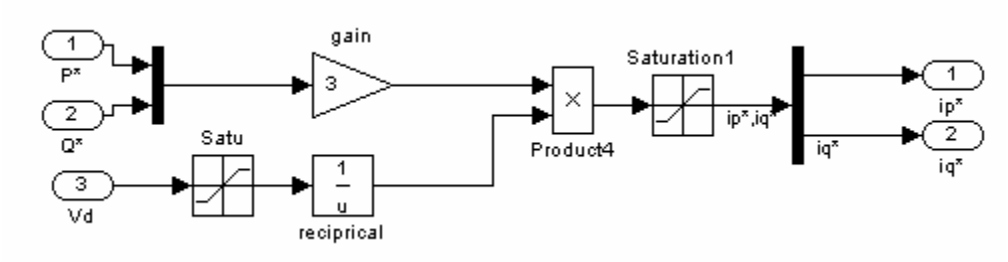


Figure 3.12 Series and shunt converter current reference

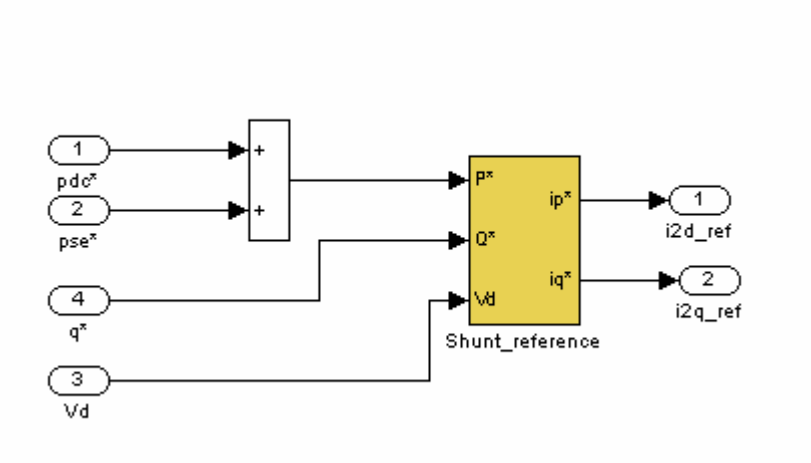


Figure 3.13 Shunt converter power coordination

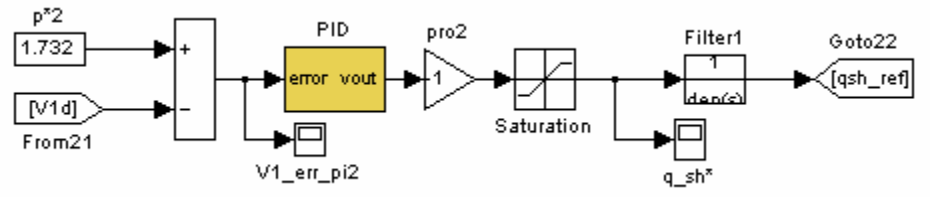


Figure 3.14 Shunt converter reactive power reference

The series converter real and reactive power commands are from the system operator, which is depicted in Figure 3.15.

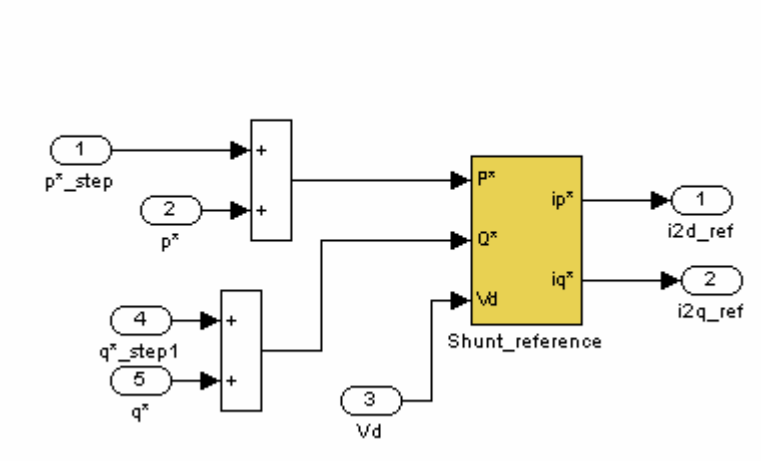


Figure 3.15 Series converter power coordination

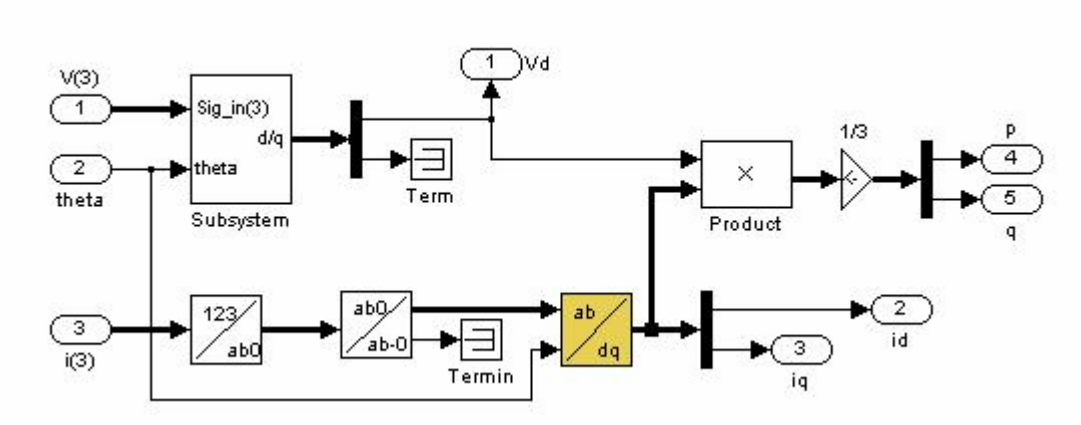


Figure 3.16 Shunt converter voltage and current d-q transformation

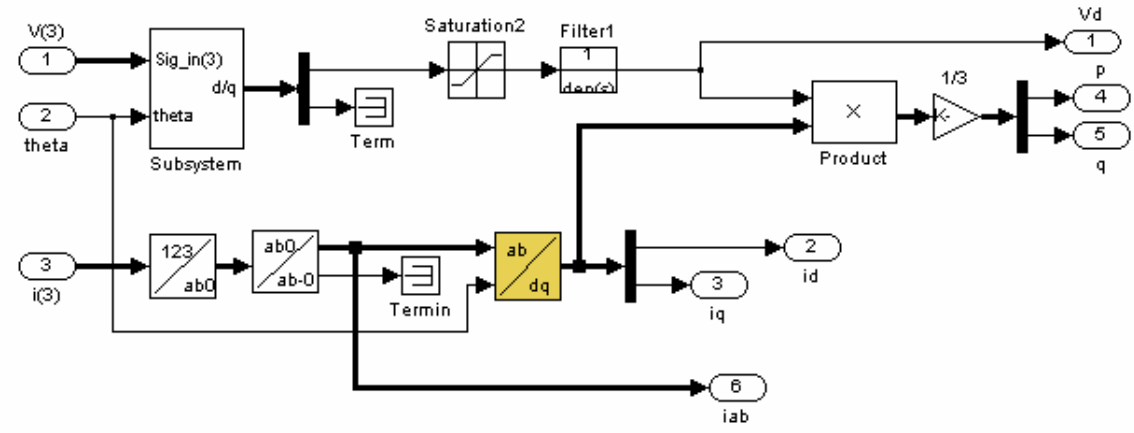


Figure 3.17 Receiving end voltage and line current d-q transformation

The voltage at the point of connection, where the shunt converter is connected, and the shunt converter current are sampled and transformed into d-q rotating axis system as shown in Figure 3.16. The receiving end voltage and the transmission line current are sampled and transformed into d-q rotating axis system as in Figure 3.17. The shunt converter and the series converter real and current controls are depicted as in Figure 3.18 and Figure 3.19 respectively. The shunt and the series converters are modeled as simple SPWM converter as in Figure 3.20. The outputs of the shunt and the series converter control blocks are used as reference signal to be compared with triangle wave to produce the shunt and series voltages to the transmission system. Figure 3.21 illustrates the DC voltage control block.

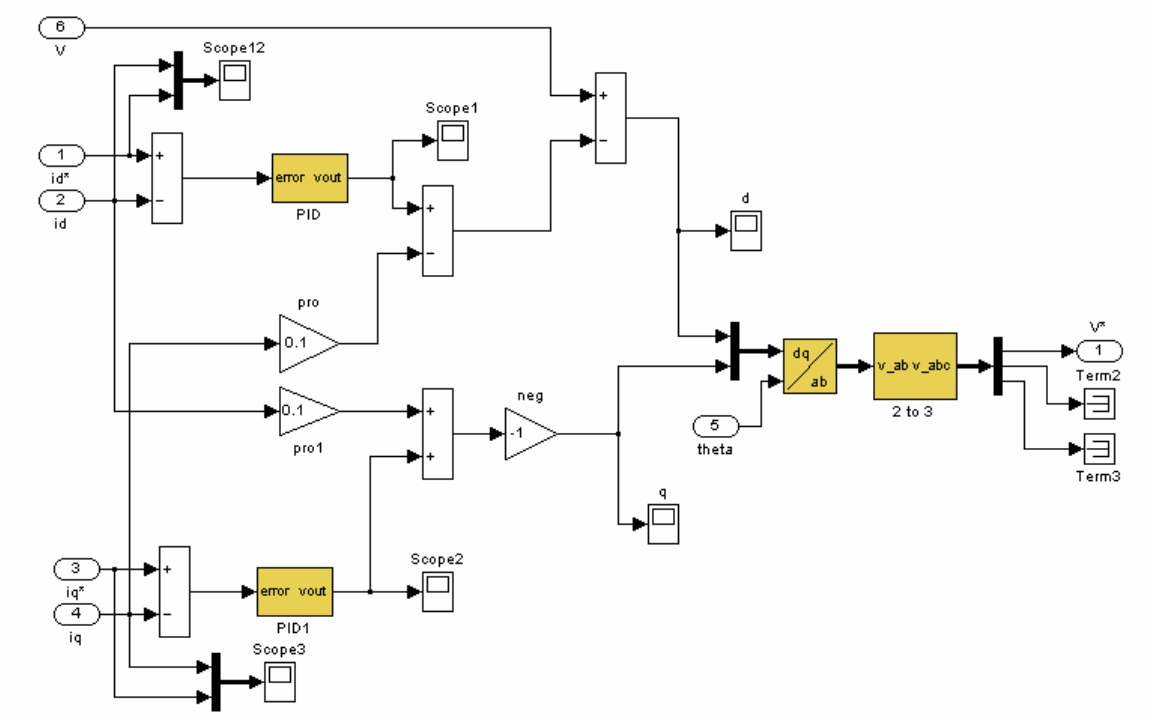


Figure 3.18 Shunt converter control

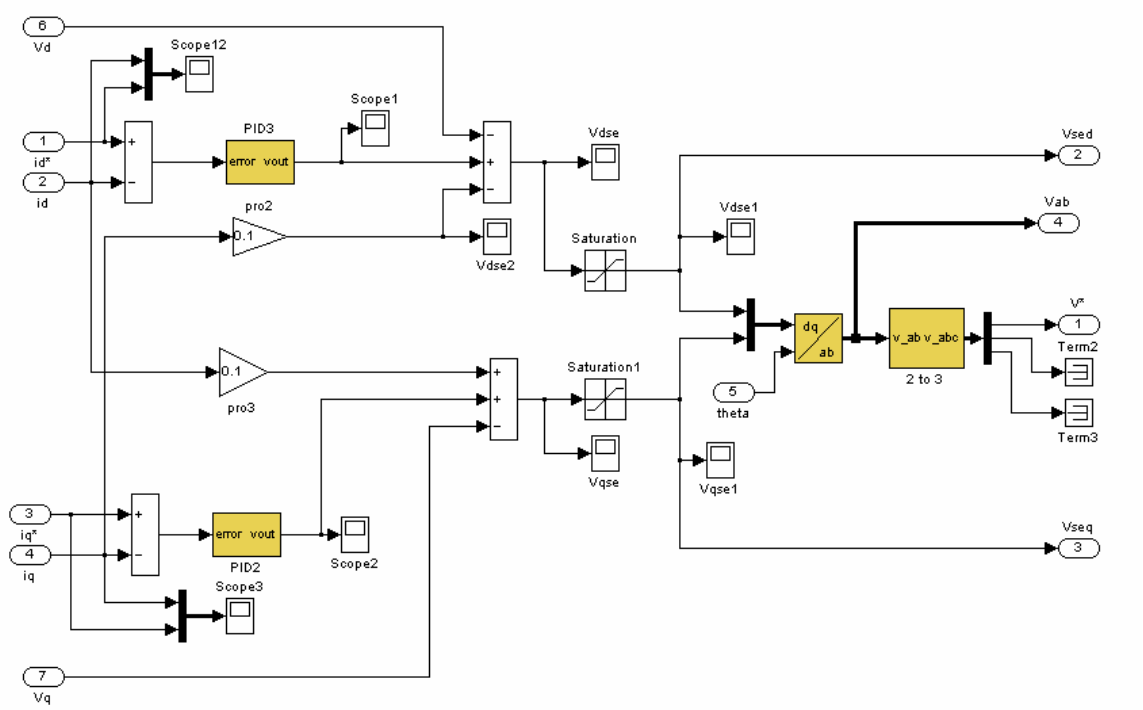


Figure 3.19 Series converter control

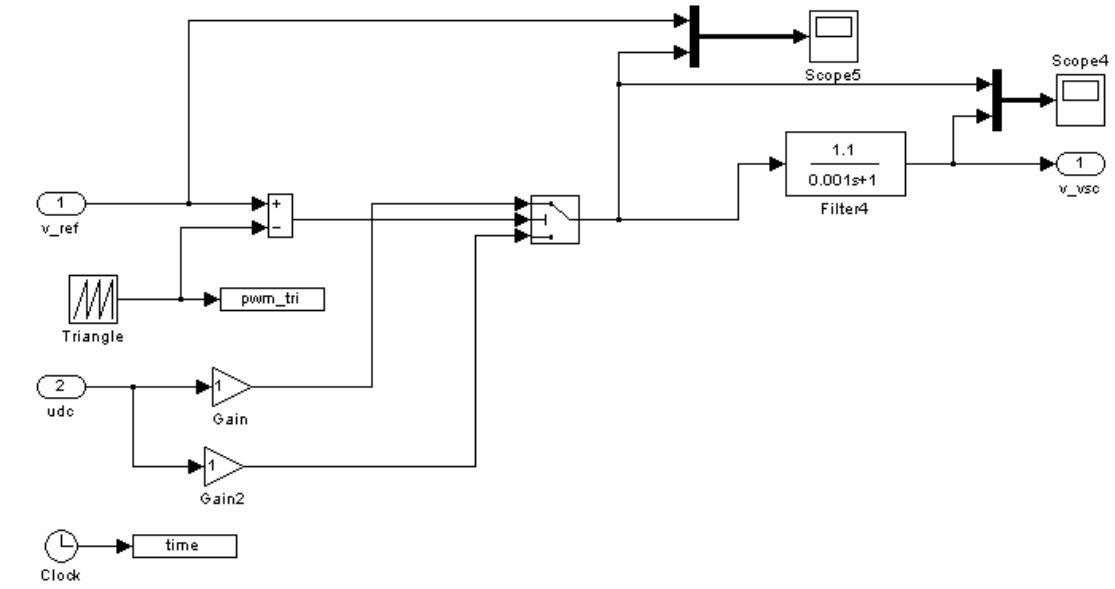


Figure 3.20 SPWM converter

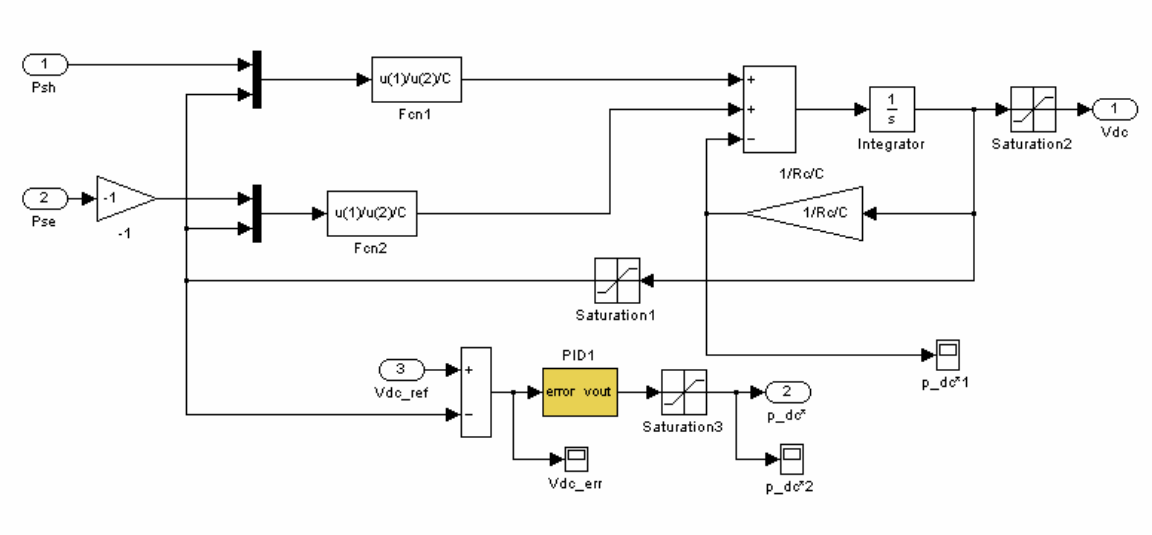


Figure 3.21 DC capacitor voltage control block

3.2.2 Simulation of the centralized unified power flow controller

The basic circuit parameters are kept unchanged. The parameters are listed in Table 3.2. In the table, R_L and xL_L are per unit line resistance and inductance per section. R_{sh} and xL_{sh} are per unit resistance and inductance of the shunt converter. The closed-loop control parameters are listed in Table 3.3 to Table 3.5. kpv1, kiv1, and kdv1 are the proportional, integral, and derivative gain of the PID controller for the sending end voltage control. kp_{DC}, ki_{DC}, and kd_{DC} are the proportional, integral, and derivative gain of the PID controller for the DC voltage control. kp_{se} and ki_{se} are the proportional and integral gain for the series converter control. kp_{cse} is the cross-coupling proportional gain for the series converter ontroller. kp_{sh} and ki_{sh} are the proportional and integral gain for the shunt converter control. kp_{csh} is the cross-coupling proportional gain for the shunt converter controller.

Table 3.2 Circuit parameter for two-bus system with the CUPFC

V_1	V_r	R_L	xL_L	R_{sh}	xL_{sh}
$1.1\angle 20^0$	$0.9\angle 0^0$	0.05	0.1	0.05	0.1

Table 3.3 Control parameters for the sending end voltage and the DC capacitor voltage control in the two-bus system with the CUPFC

kp_{v1}	ki_{v1}	kd_{v1}	kp_{DC}	Ki_{DC}	Kd_{vDC}
1	50	0.03	5	15	0.005

Table 3.4 Control parameters for the series converter in the two-bus system with the CUPFC

kp_{se}	ki_{se}	kp_{cse}
0.5	10	0.1

Table 3.5 Control parameters for the shunt converter control in the two-bus system with the CUPFC

kp_{sh}	ki_{sh}	kp_{csh}
0.5	20	0.1

The above mentioned CUPFC is simulated in different cases. Figure 3.22 shows the transmitted real and reactive power in one of the cases. Initially, the real and reactive powers are both controlled to be 1.0 pu. At the time of 0.6 second, the reactive power command changes from 1.0 pu to 0.0 pu. At the time instant of 1 second, the real power command changes from 1.0 pu to 0.0 pu. The system successfully controls the transmission line real and reactive powers follow the change. The response time is about 200ms. Figure 3.23 depicts the sending end bus voltage magnitude when the real and reactive power changes. The series injected voltage is illustrated in Figure 3.24. Figure 3.25 shows the shunt converter output voltage. Figure 3.26 depicts the transmission line current. Figure 3.27 illustrates the DC capacitor voltage.

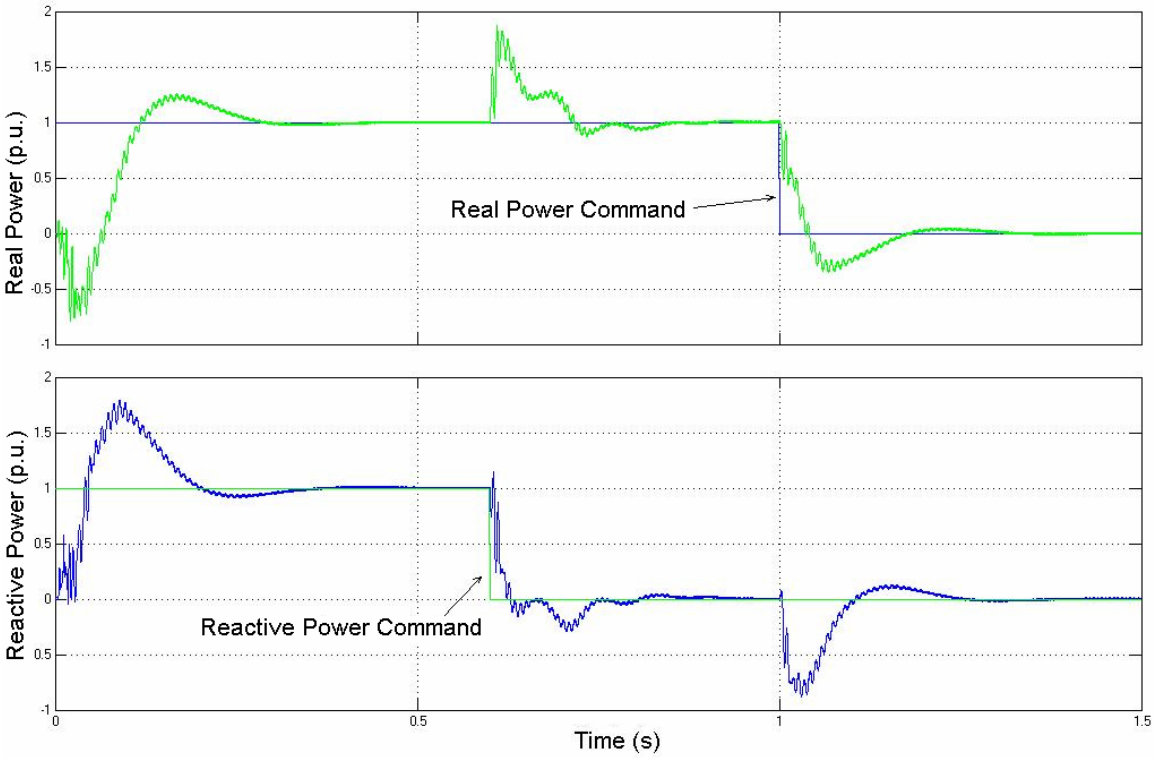


Figure 3.22 Transmitted real and reactive power with CUPFC

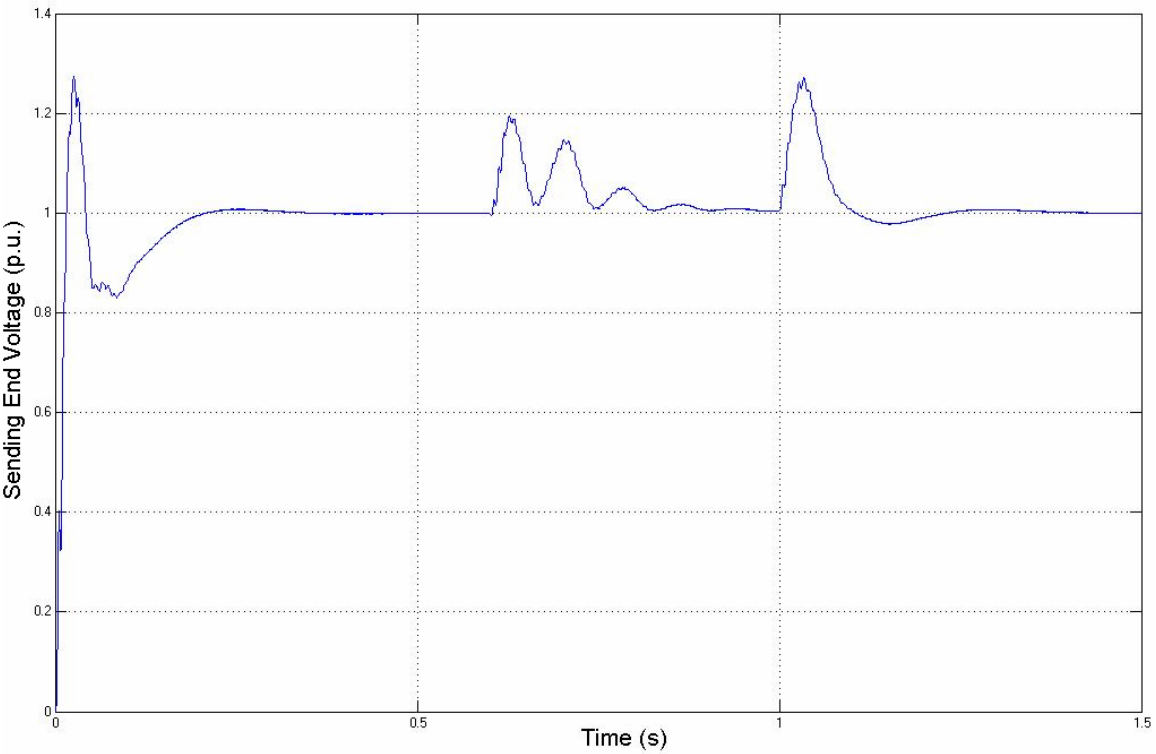


Figure 3.23 Sending end bus voltage with CUPFC

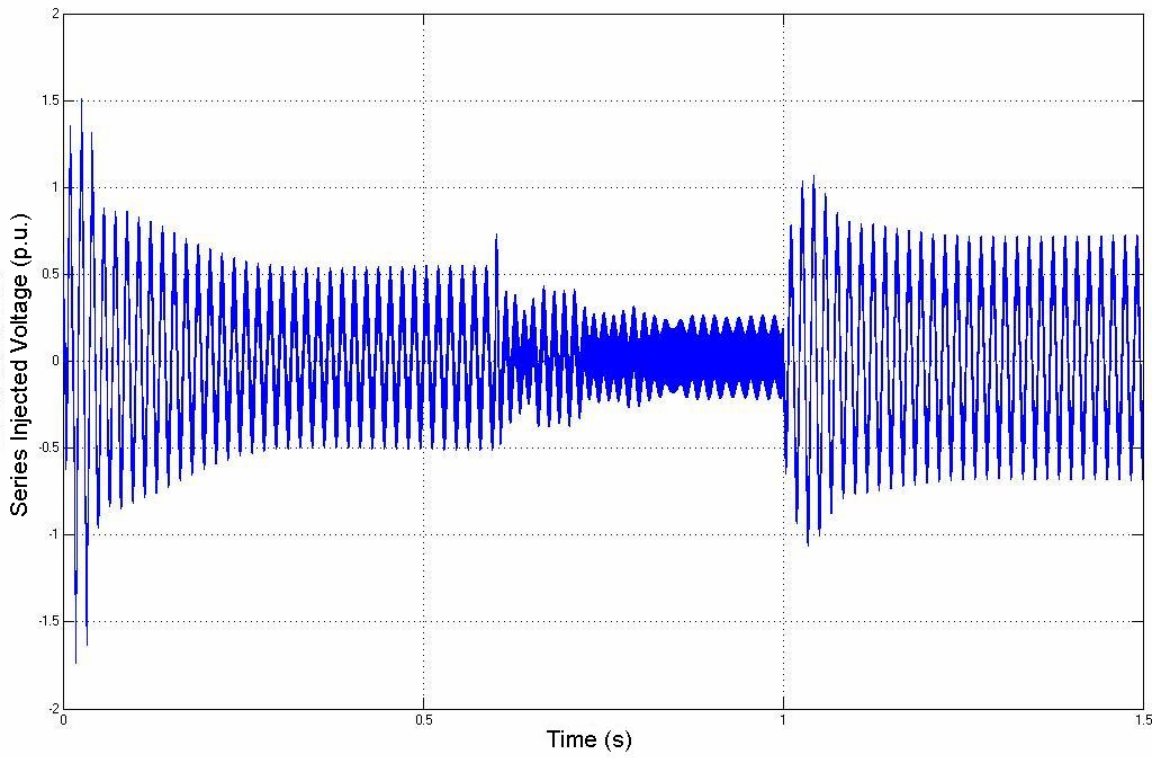


Figure 3.24 Series injected voltage with CUPFC

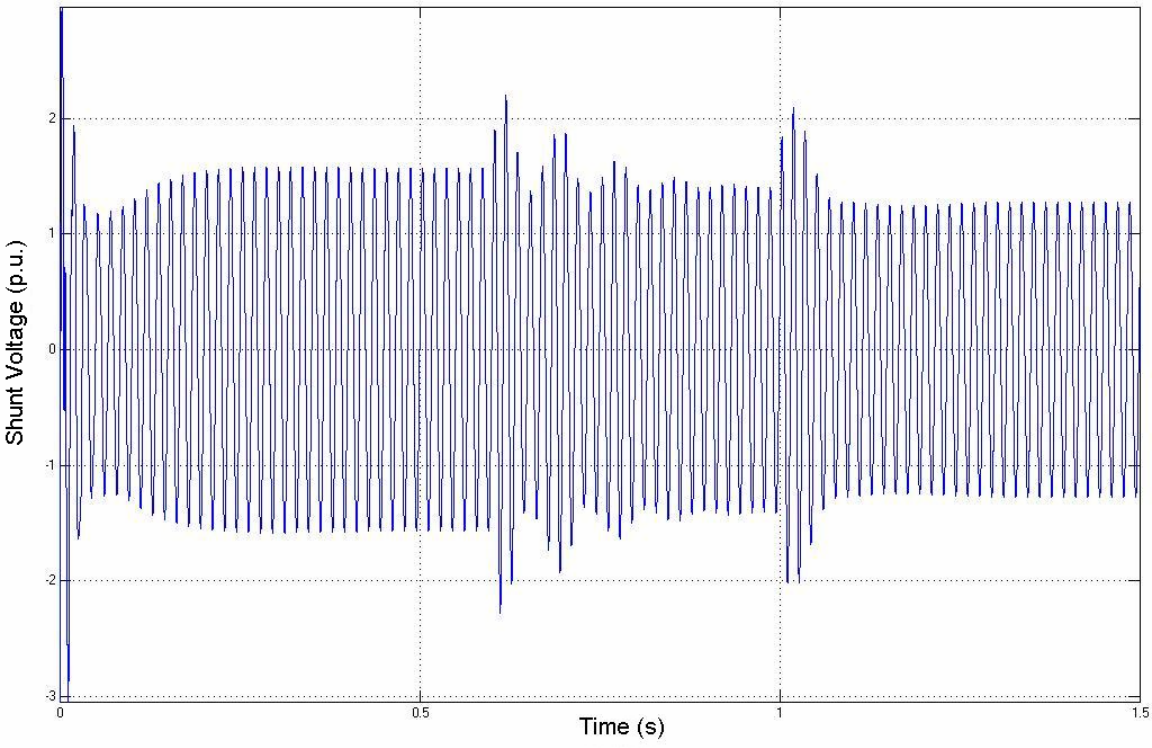


Figure 3.25 Shunt converter output voltage with CUPFC

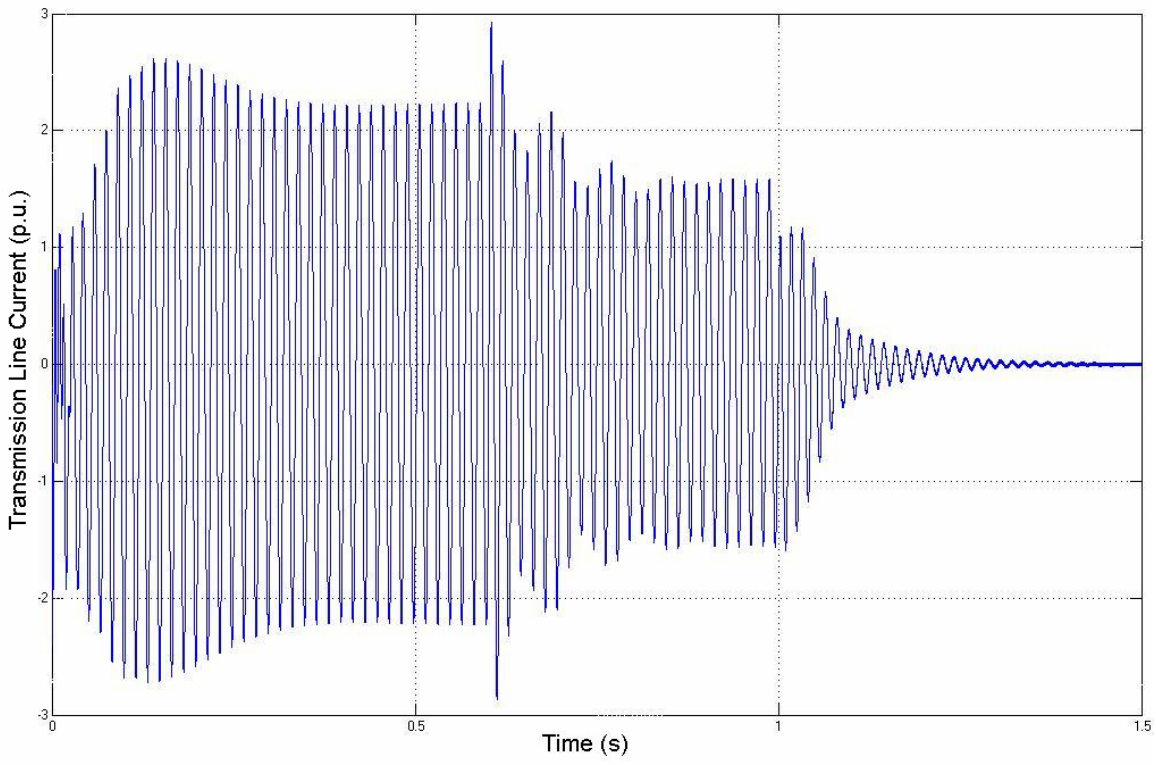


Figure 3.26 Transmission line current with CUPFC

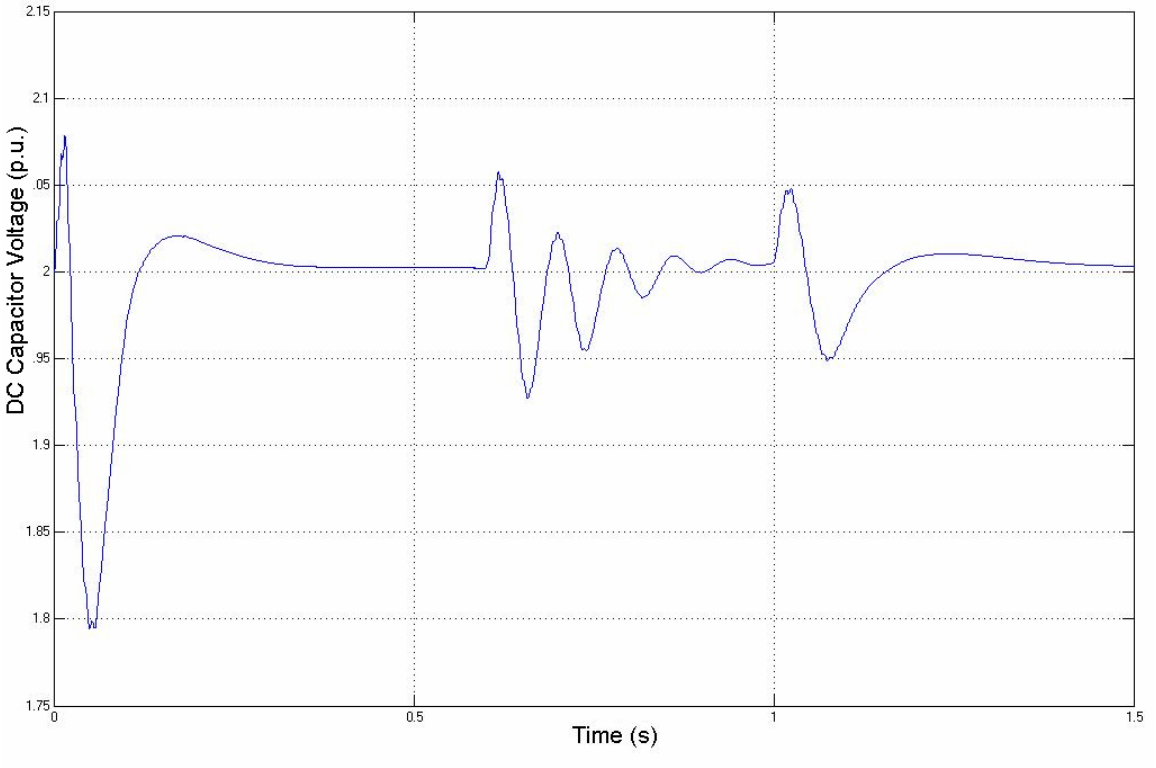


Figure 3.27 DC capacitor voltage with CUPFC

Figure 3.28 shows the real and reactive power in the second case. The transmitted real and reactive powers are initially controlled to be 1.0 pu. At the time of 0.5 second, the reactive power command changes from 1.0 pu to -0.5 pu. At the time instant of 1 second, the real power command changes from 1.0 pu to -0.5 pu. The system successfully controls the transmission line real and reactive powers to follow the change. The response time is about 500ms. Figure 3.29 depicts the sending end bus voltage magnitude when the real and reactive power changes in this case. It is obvious, with bigger change in the real and reactive power command, transient process is longer, and it takes longer for the system to reach steady state. Figure 3.30 shows the series injected voltage. Figure 3.31 depicts the shunt converter output voltage. The transmission line current is illustrated in Figure 3.32. Figure 3.33 shows the DC capacitor voltage in this simulation case.

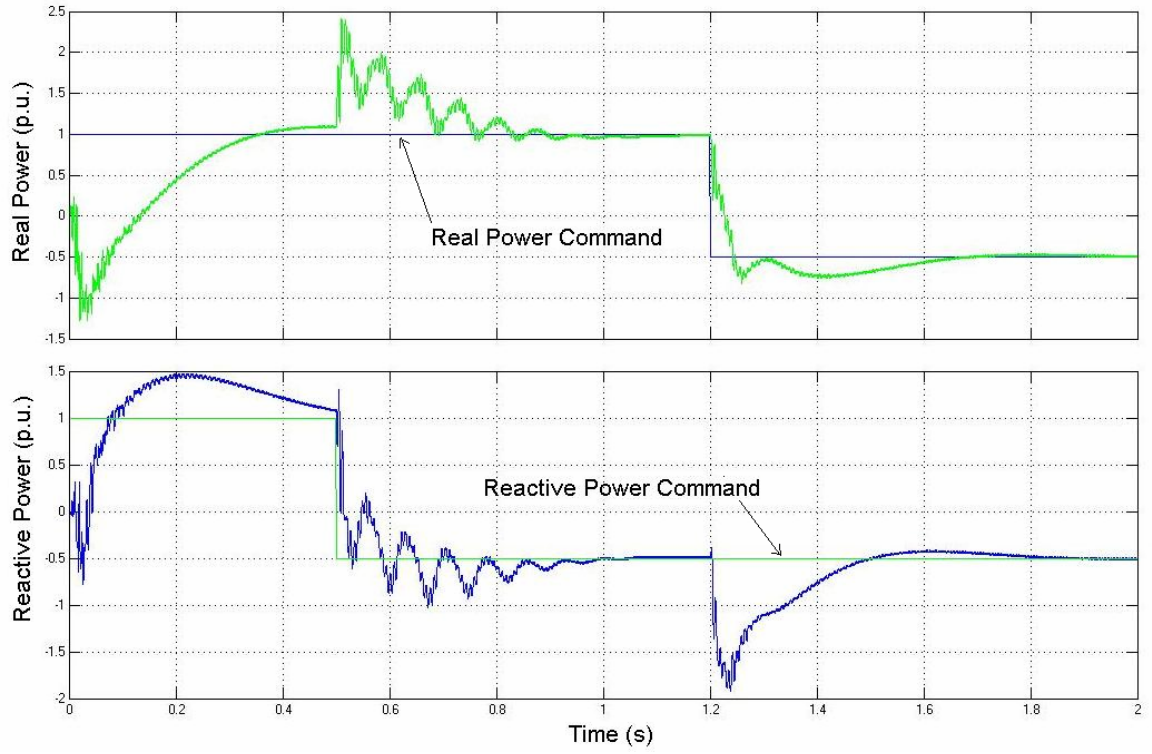


Figure 3.28 Transmitted real and reactive power with CUPFC (case 2)

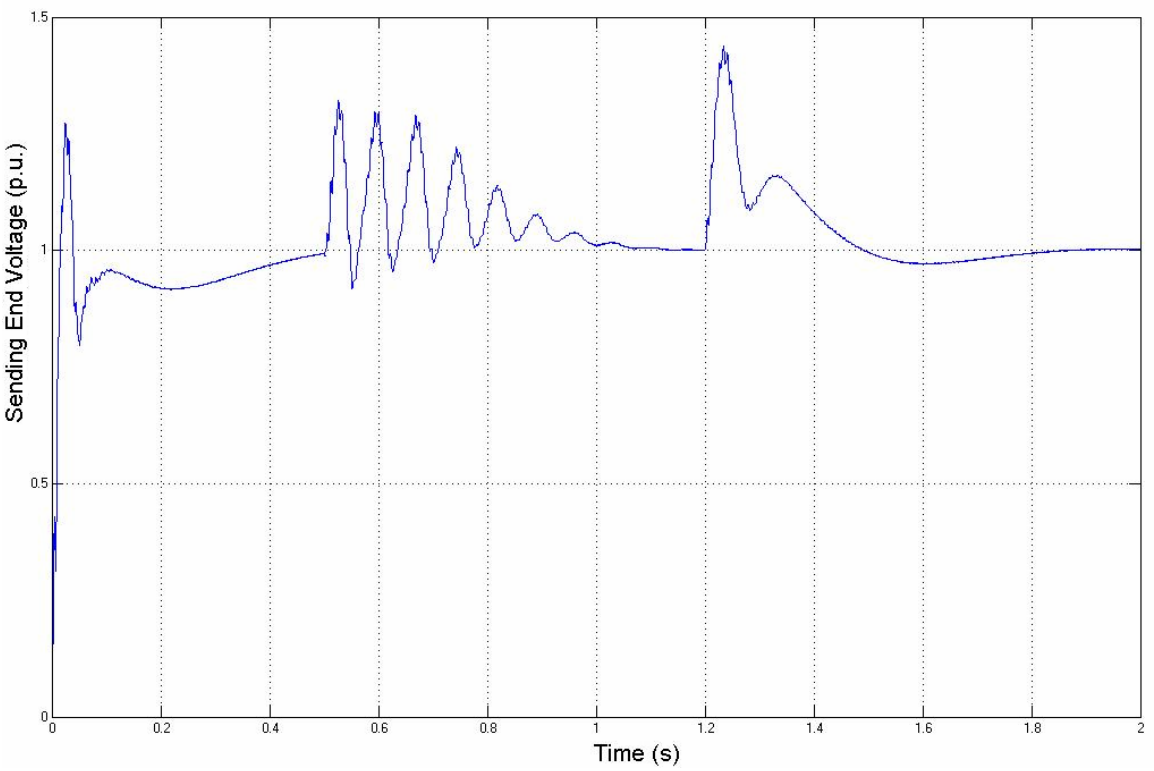


Figure 3.29 Sending end bus voltage with CUPFC (case 2)

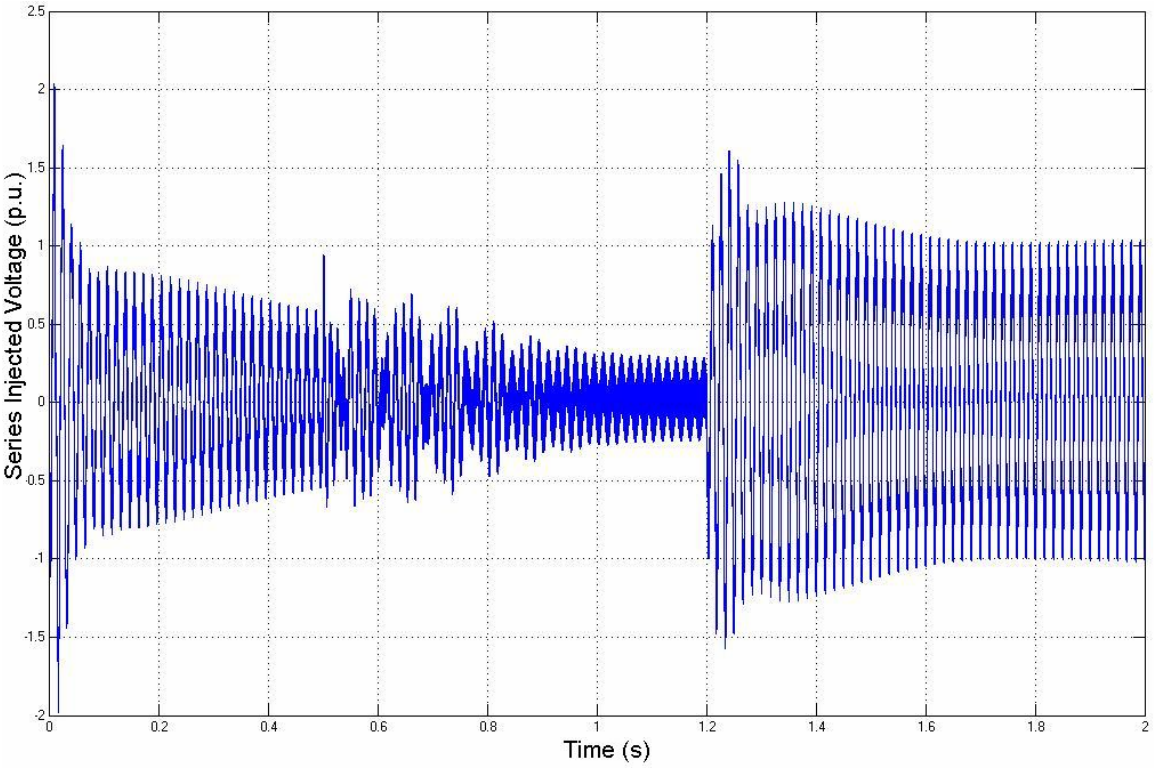


Figure 3.30 Series injected voltage with CUPFC (case 2)

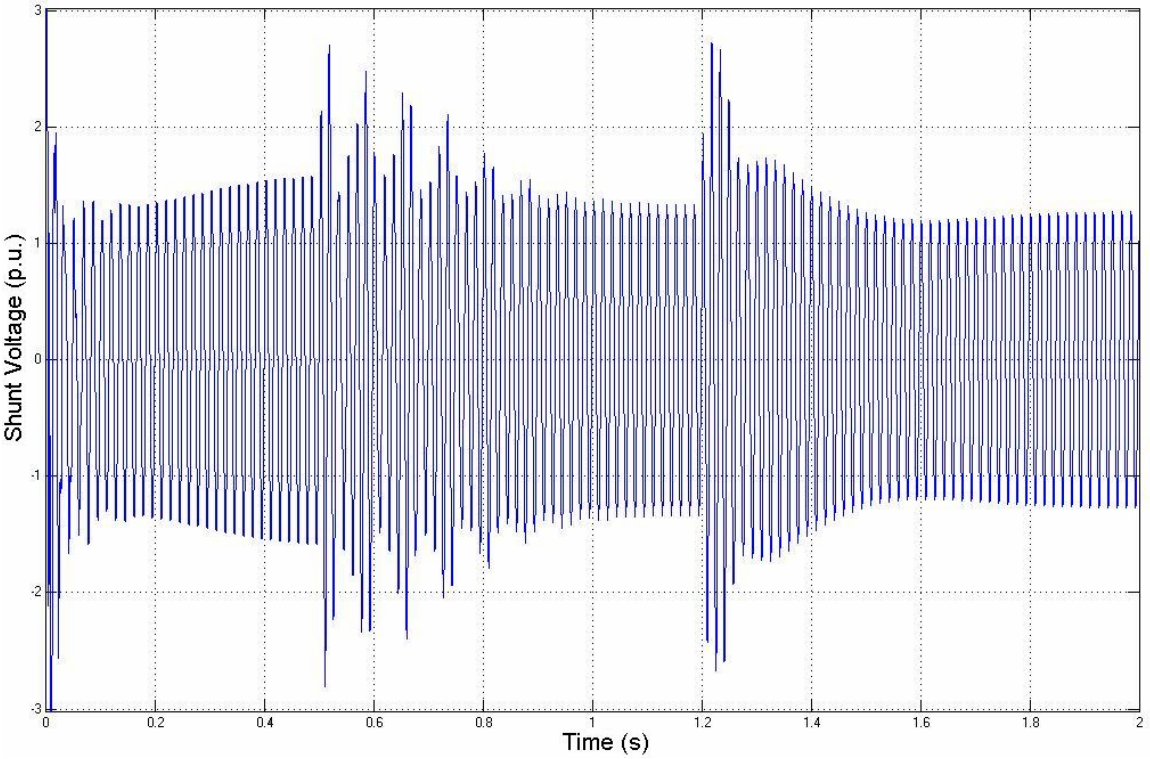


Figure 3.31 Shunt converter output voltage with CUPFC (case 2)

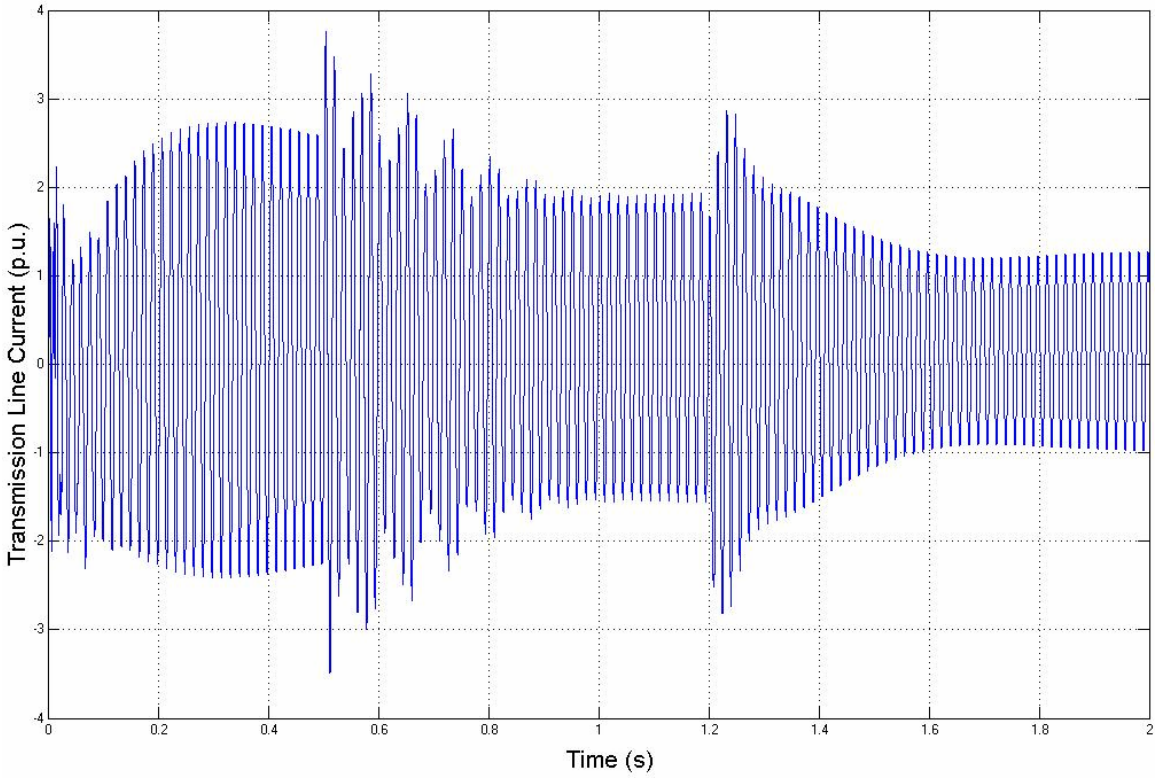


Figure 3.32 Line current with CUPFC (case 2)

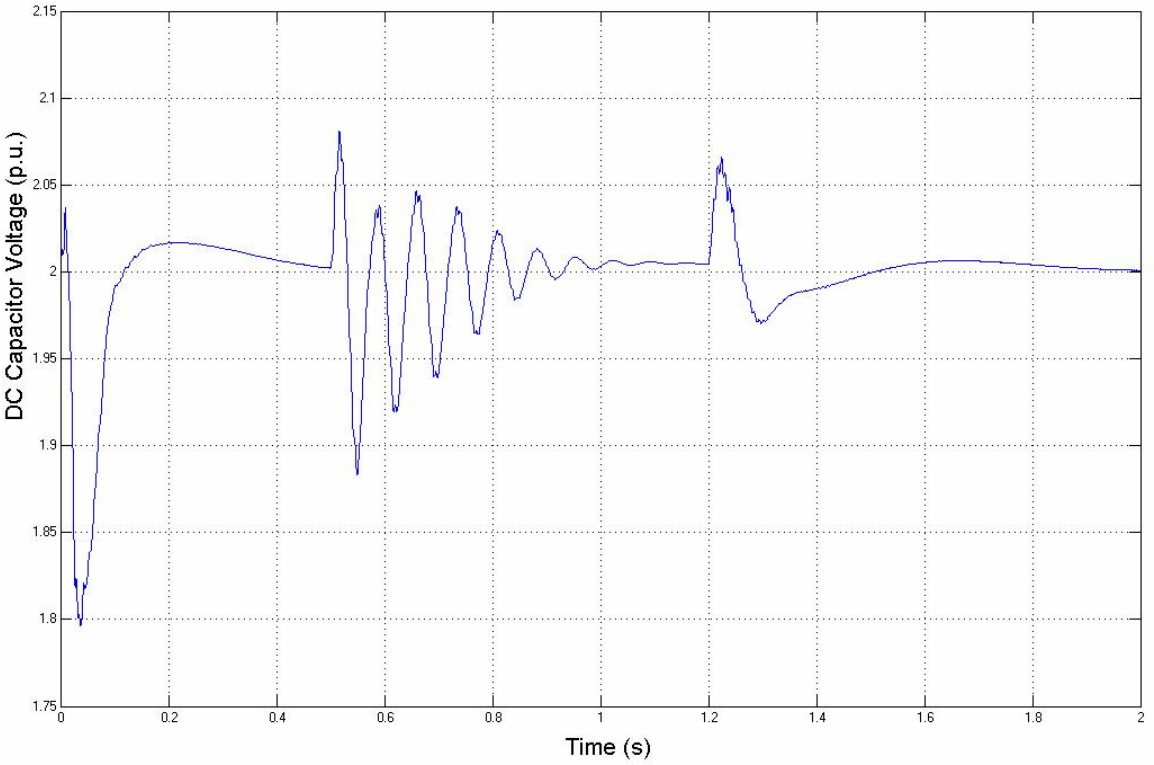


Figure 3.33 DC capacitor voltage with CUPFC (case 2)

3.3 Simulation of the DUPFC

Control of the DUPFC is developed based on the control of the CUPFC. The Simulink model is based on the control algorithm demonstrated in Figure 2.33 and Figure 2.34.

3.3.1 Simulink model of a distributed unified power flow controller

The DUPFC is modeled by Simulink. Three units are put into the transmission line between four line sections. The model is shown in Figure 3.34. The transmission line real and reactive powers are controlled by controller illustrated in Figure 3.35. Output of the controller is the series injected voltage reference. In this DUPFC case, the voltage reference is the total voltage needed to inject into the transmission line. The voltage reference is distributed to every UPFC unit. In this simulation model, the voltage reference is distributed to every unit equally. The sending end voltage magnitude is controlled by a PID controller. Output of the PID

controller is the reactive power needed from the shunt converters. The reactive power need is distributed to three DUPFC units. In this simulation model, the reactive power is equally assigned to every unit, as depicted in Figure 3.36.

For every DUPFC unit, the real power is coordinated between the series converter and the shunt converter. The real power injected into the transmission line by the series converter is calculated as in Figure 3.37. In the diagram, Vse_i is the series voltage injected by i^{th} series converter. And Ise_i is the line current in i^{th} section where the DUPFC unit is operating. Due to currents injected by the shunt converters, line currents in different sections are different. Figure 3.38 demonstrates the relationship of the line and shunt currents. It can be seen that:

$$\begin{cases} i_{se3} = i_{se} + i_{sh3} \\ i_{se2} = i_{se3} + i_{sh2} \\ i_{se1} = i_{se2} + i_{sh1} \end{cases} \quad (6)$$

This current relationship is integrated in the model as shown in Figure 3.34.

The line current control is depicted in Figure 3.39. The control scheme is the same as in the CUPFC line current control. For every DUPFC unit, the shunt converter control scheme is the same as in the CUPFC. The difference is that the real power need is from the calculation of the series converter in the same unit.

Since the focus of the project is the feasibility of the distributed unified power flow controller on the system level, the converter switching is not included in the model. The output of the inverter is assumed to be the same as the converter voltage reference. This is in fact a fundamental frequency model simulation of the system as is used in [110] and [111].

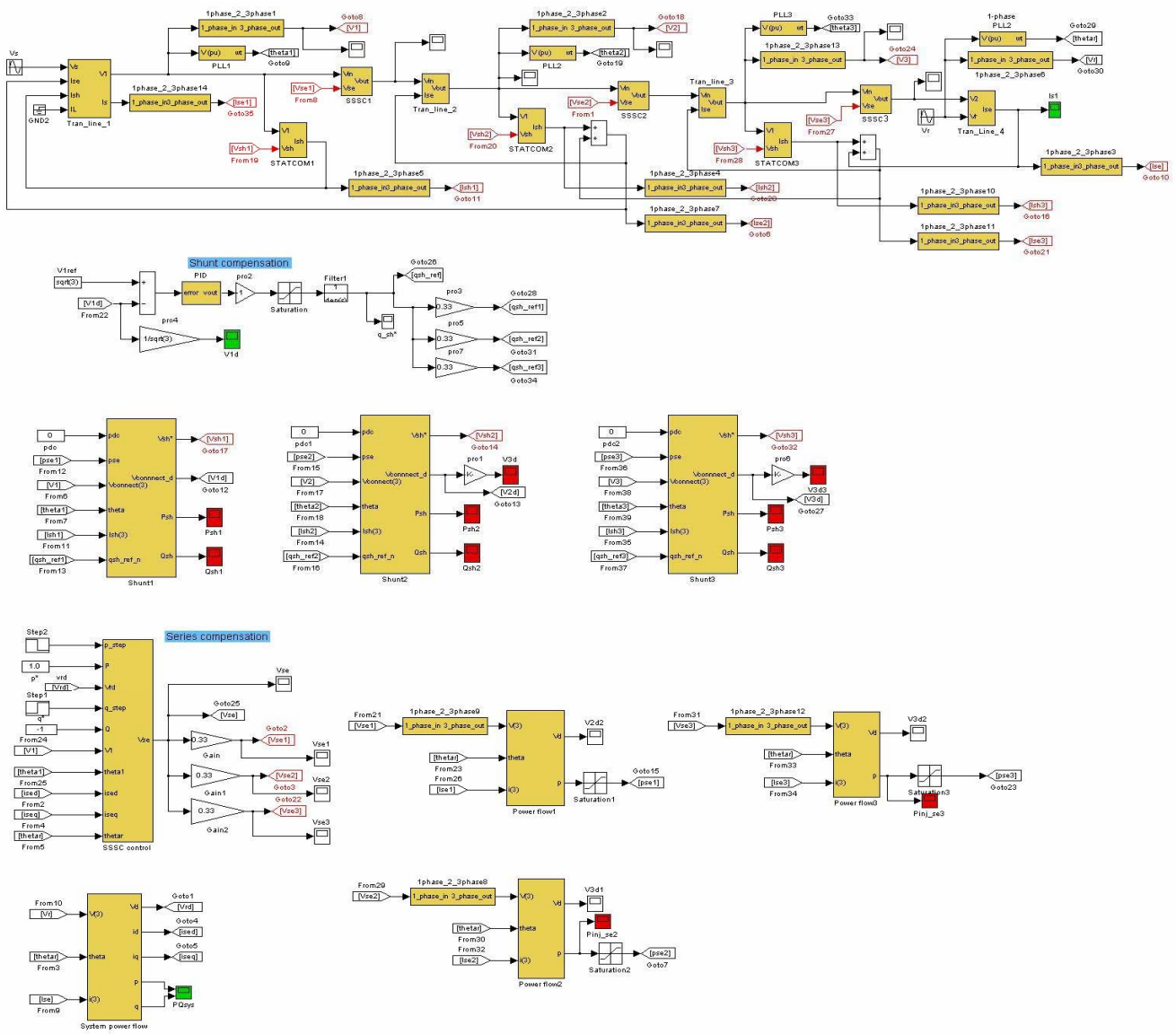


Figure 3.34 Simulink model of the DUPFC

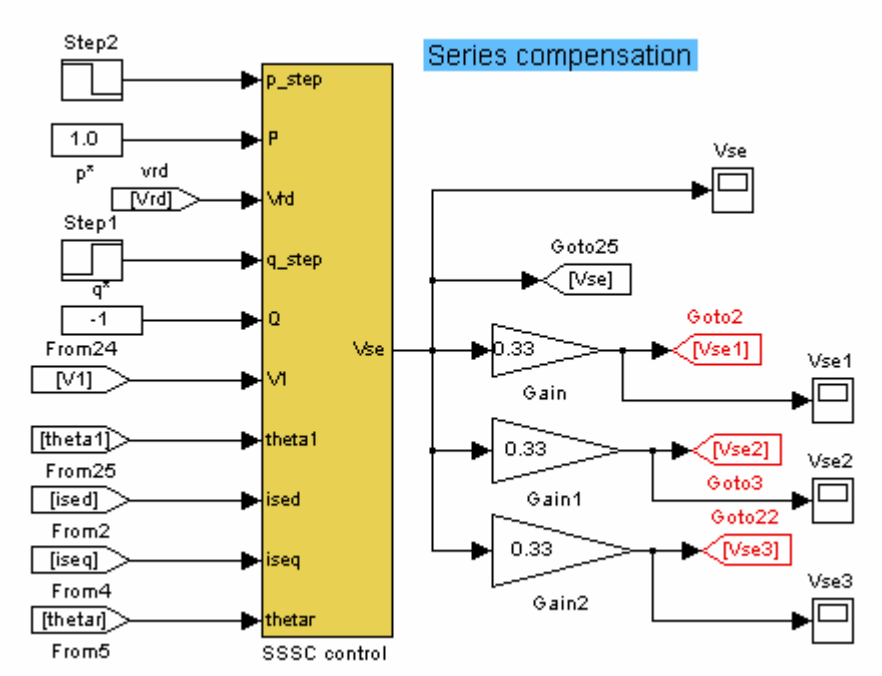


Figure 3.35 Transmission line power flow control

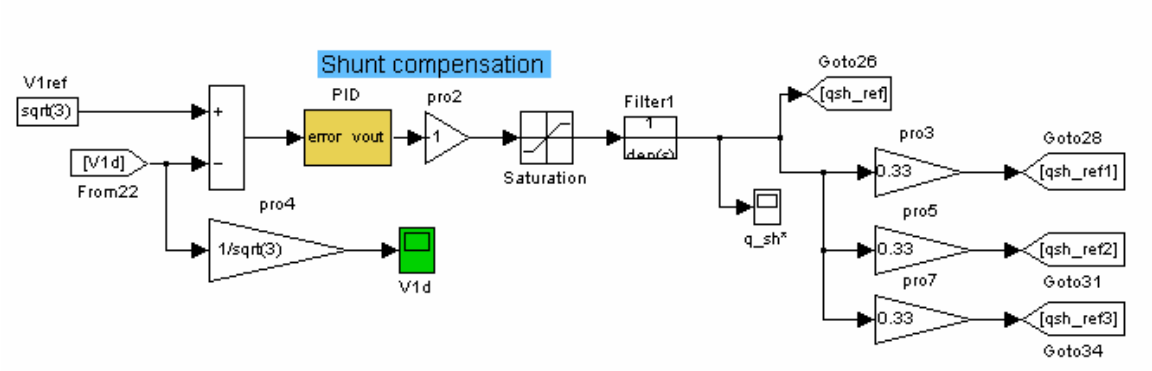


Figure 3.36 Sending end voltage control and reactive power distribution

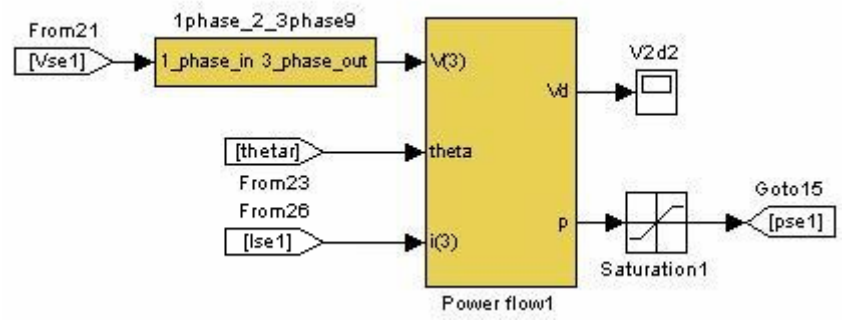


Figure 3.37 DUPFC unit real power request calculation

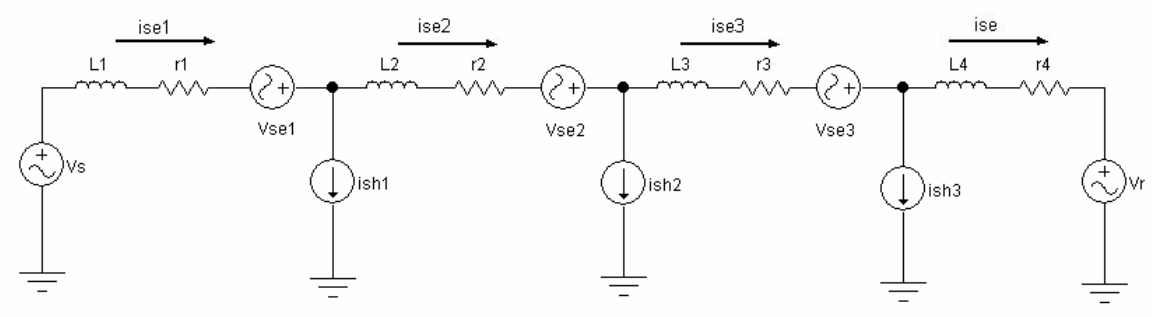


Figure 3.38 Current relationship in the DUPFC

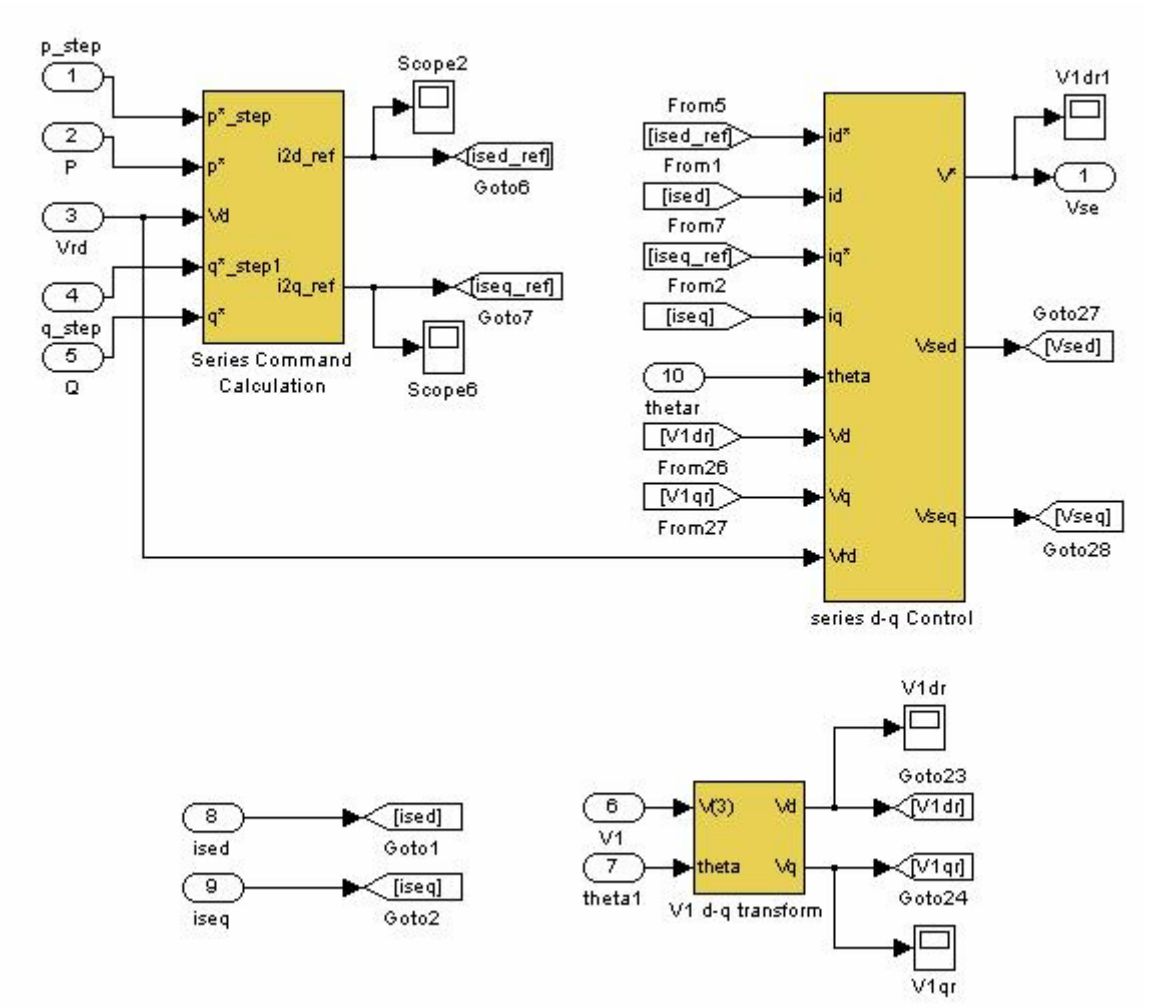


Figure 3.39 Line current control

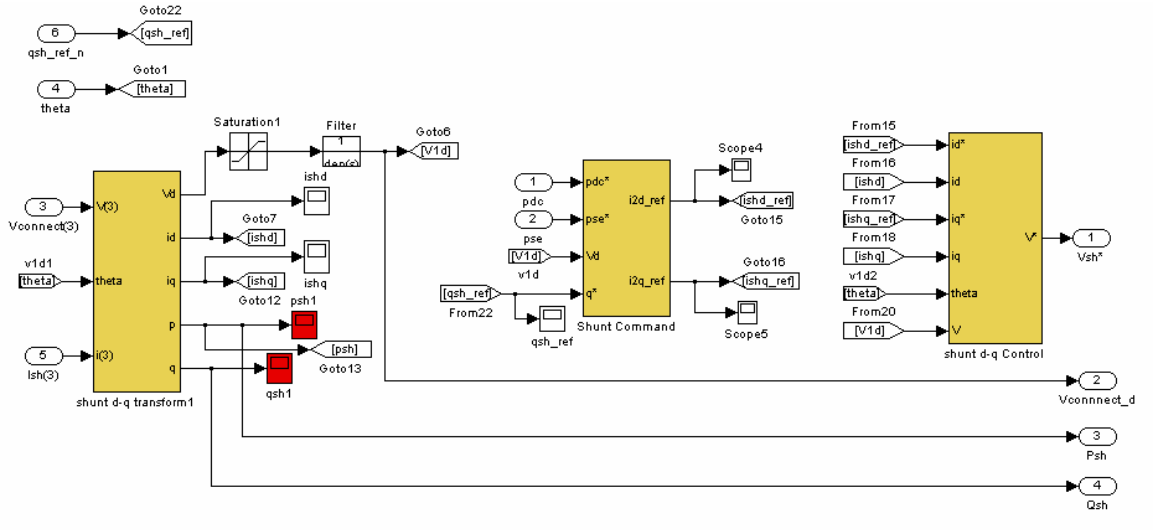


Figure 3.40 DUPFC unit shunt converter control

3.3.2 Simulation of the distributed unified power flow controller

The circuit parameters are listed as in Table 3.6. In the table, RL and xLL are per unit line resistance and inductance per section. Rsh and xLsh are per unit resistance and inductance of the shunt converter. The closed-loop control parameters are listed in Table 3.7 to Table 3.9. kpv1, kiv1, and kdv1 are the proportional, integral, and derivative gain of the PID controller for the sending end voltage control. kp_{se} and ki_{se} are the proportional and integral gain for the series converter control. kp_{cse} is the cross-coupling proportional gain for the series converter controller. kp_{sh} and ki_{sh} are the proportional and integral gain for the shunt converter control. kp_{csh} is the cross-coupling proportional gain for the shunt converter controller.

Table 3.6 Circuit parameter for two-bus system with the DUPFC

V_1	V_r	R_L	xL_L	R_{sh}	xL_{sh}
$1.1\angle 20^0$	$0.9\angle 0^0$	0.05	0.1	0.05	0.1

Table 3.7 Control parameters for the sending end voltage control in the two-bus system with the DUPFC

kp_{v1}	ki_{v1}	kd_{v1}
1	50	0.05

Table 3.8 Control parameters for the series converter in the two-bus system with the DUPFC

kp_{se}	ki_{se}	kp_{cse}
5	50	0.2

Table 3.9 Control parameters for the shunt converter control in the two-bus system with the DUPFC

kp_{sh}	ki_{sh}	kp_{csh}
0.5	20	0.2

The DUPFC system is simulated. Initially, the transmitted real power is 1.0 pu. And the transmitted reactive power is -1.0 pu. At the time instant of 0.7 sec, the real power command changes from 1.0 pu to -1.0 pu. At the time instant of 1.0 sec, the transmitted reactive power command changes from -1.0 pu to 1.0 pu. The sending end voltage is controlled to be 1.0 pu. Figure 3.41 shows the transmitted real and reactive power. Figure 3.42 illustrates the sending end voltage magnitude. It is obvious that the transmitted power and sending end bus voltage are controlled to follow their commands. Figure 3.43, Figure 3.44 and Figure 3.45 depicts the shunt converter voltages in different DUPFC unit. The shunt converter 3 is close to the receiving end bus. The shunt converter 1 is close to the sending end bus, and the shunt converter 2 is in the middle. Outputs of the shunt converters are adjusted their voltages according to the voltage at their respective connection points. Figure 3.46 shows the series injected voltage in every DUPFC unit.

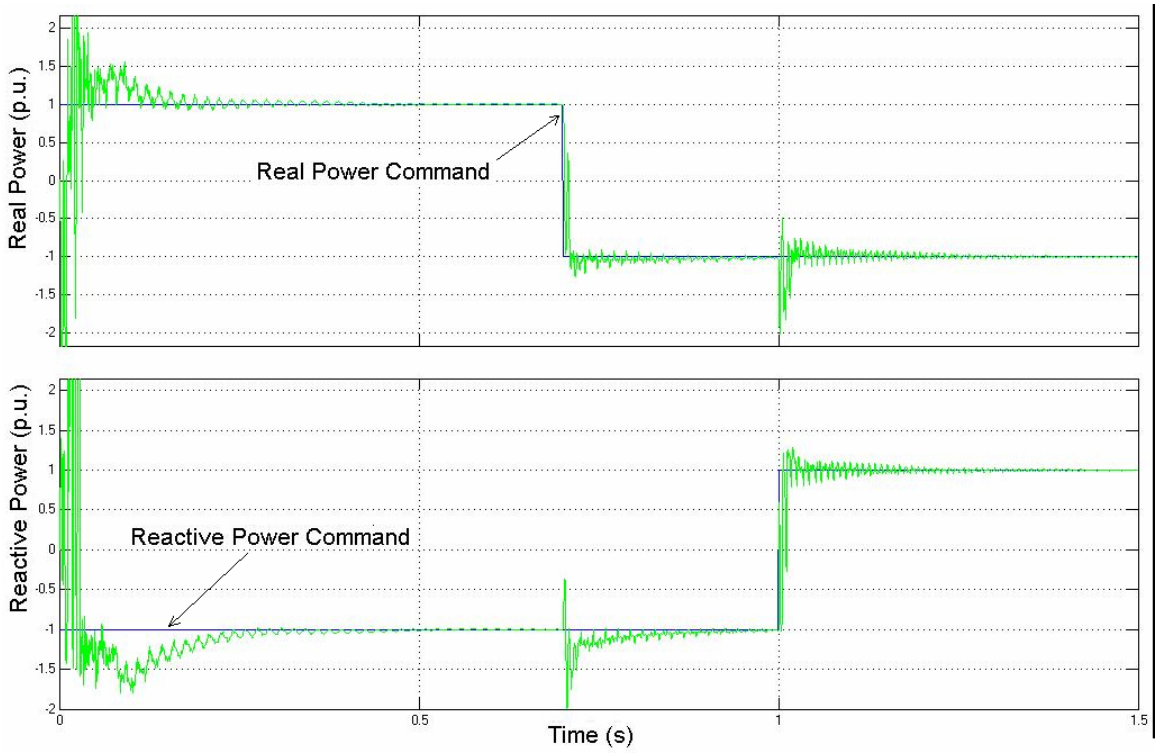


Figure 3.41 Transmitted real and reactive power with DUPFC

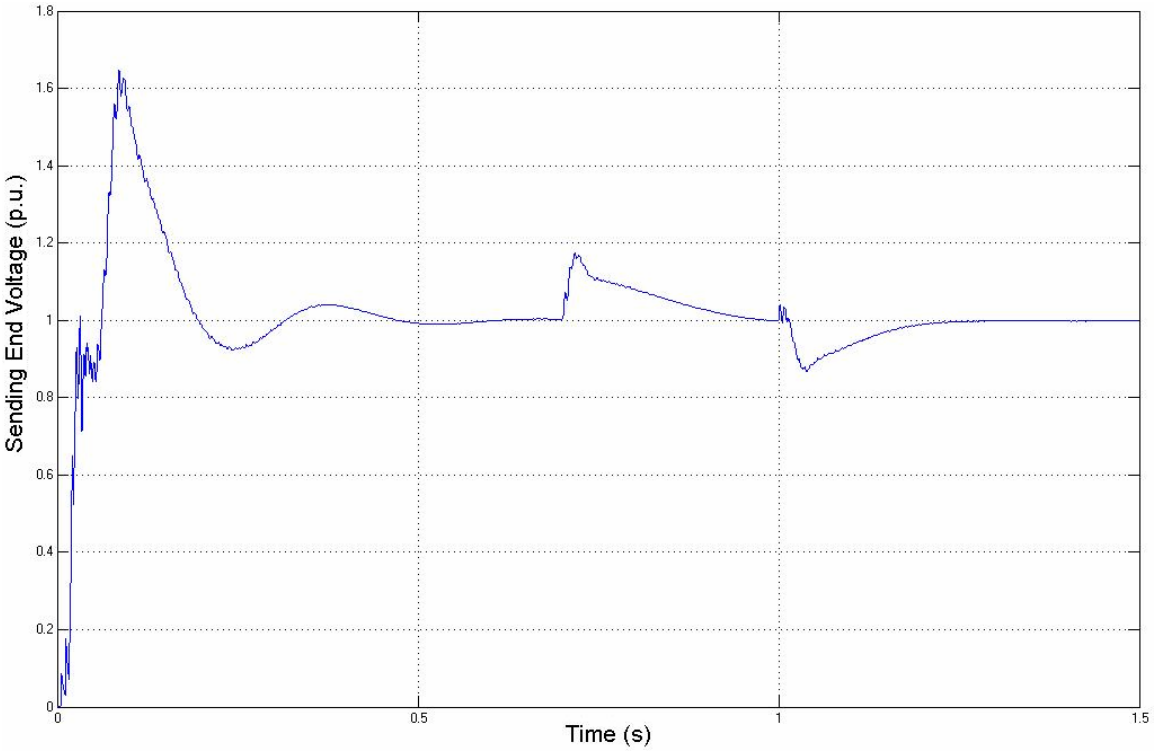


Figure 3.42 Sending end voltage magnitude

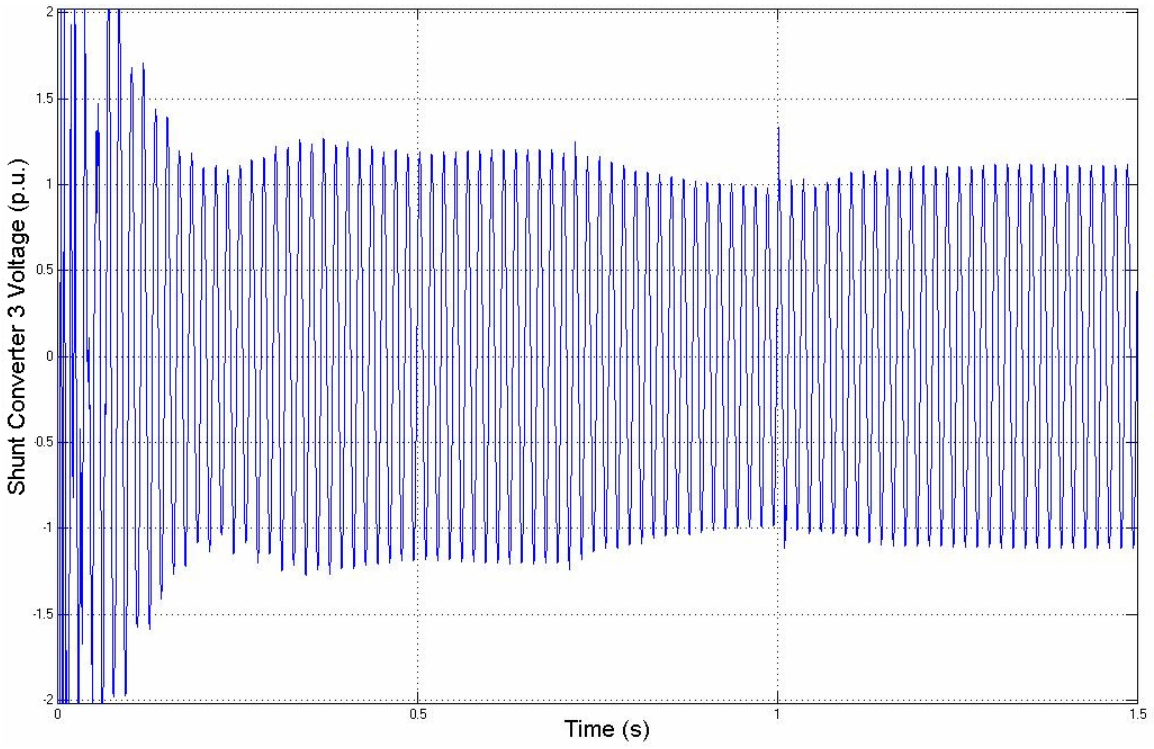


Figure 3.43 Shunt converter 3 voltage

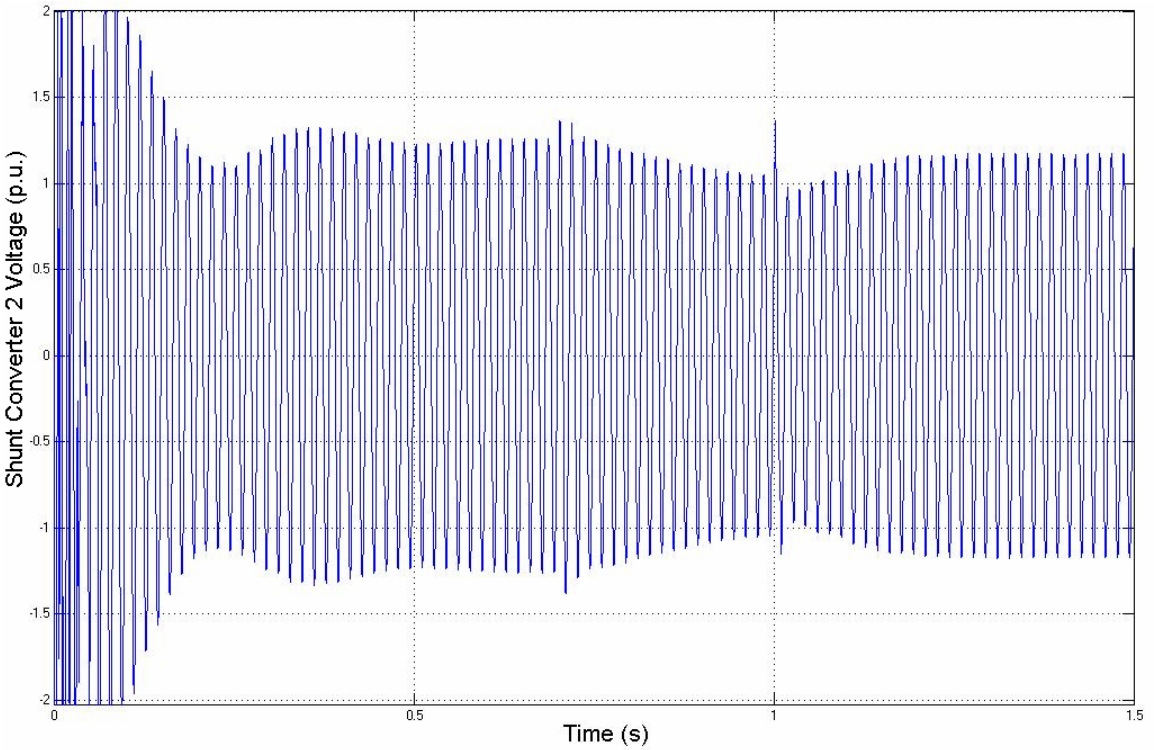


Figure 3.44 Shunt converter 2 voltage

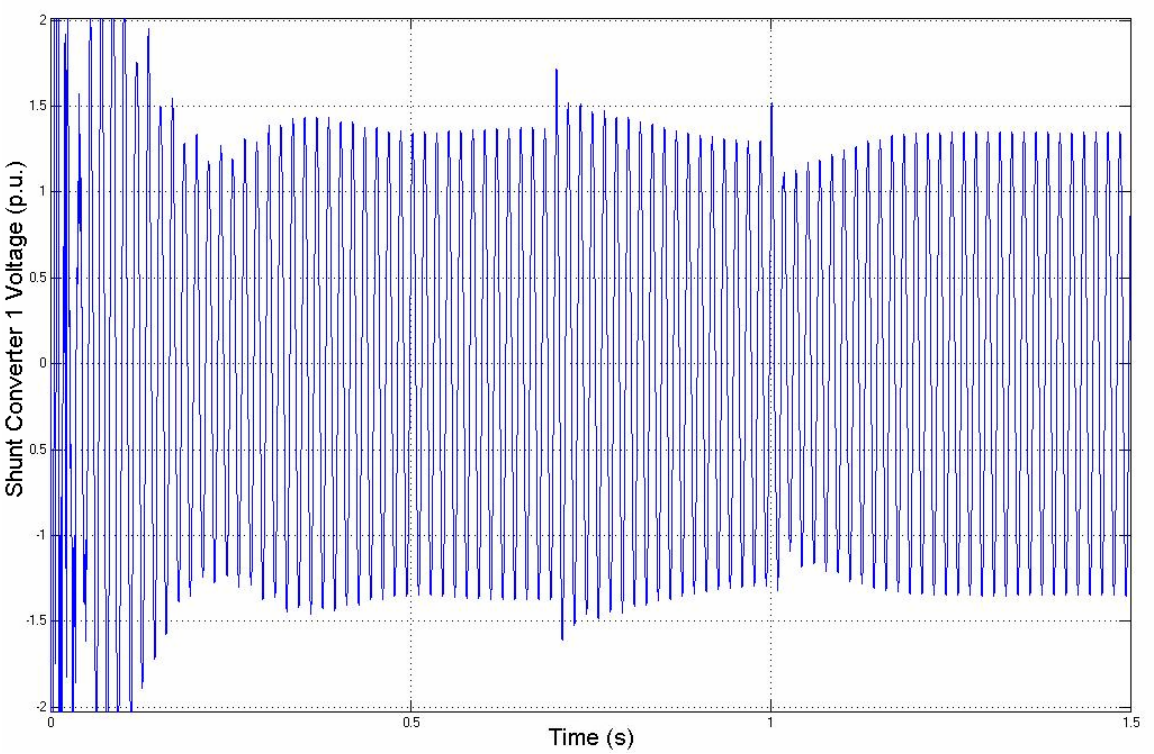


Figure 3.45 Shunt converter 1 voltage

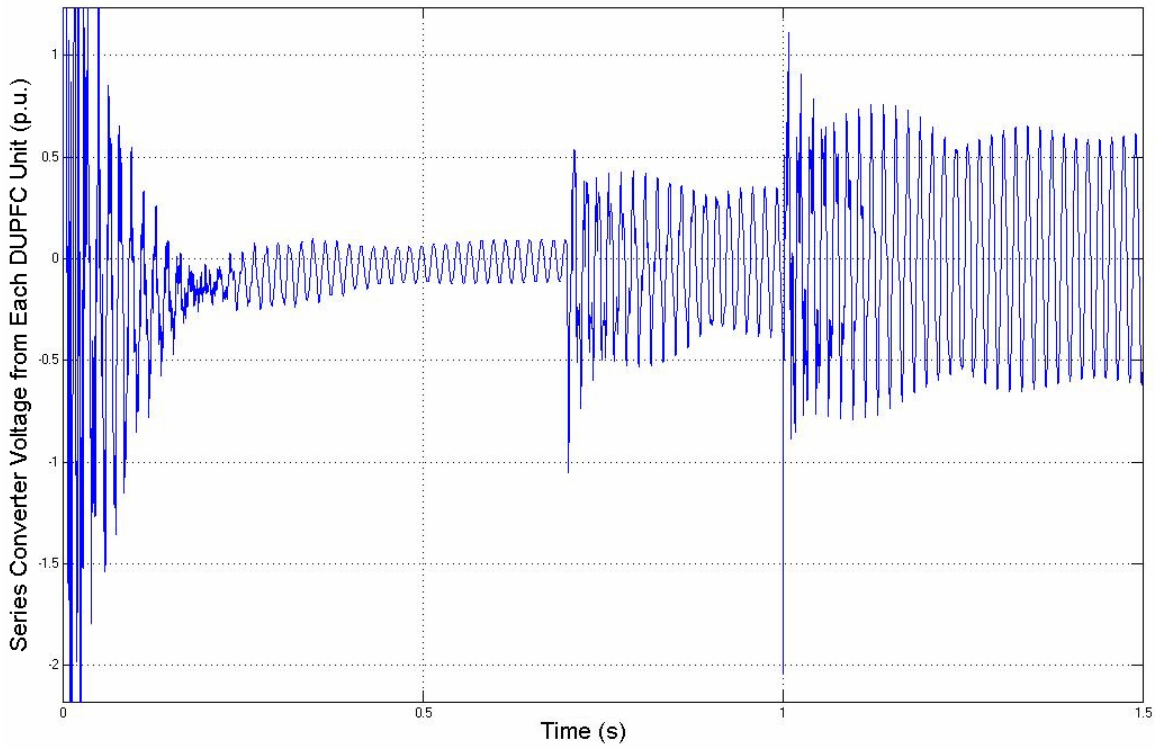


Figure 3.46 Series converter voltage

CHAPTER 4 IMPLEMENTATION AND EXPERIMENTAL RESULTS

4.1 Hardware Configuration

To verify the DUPFC concept, a two-unit system with 500 VA rating was built. For the flexibility and reliability of the digital circuit, the control algorithm is implemented on a fixed point Digital Signal Processor (DSP). The block diagram of the lab model is shown in Figure 4.1.

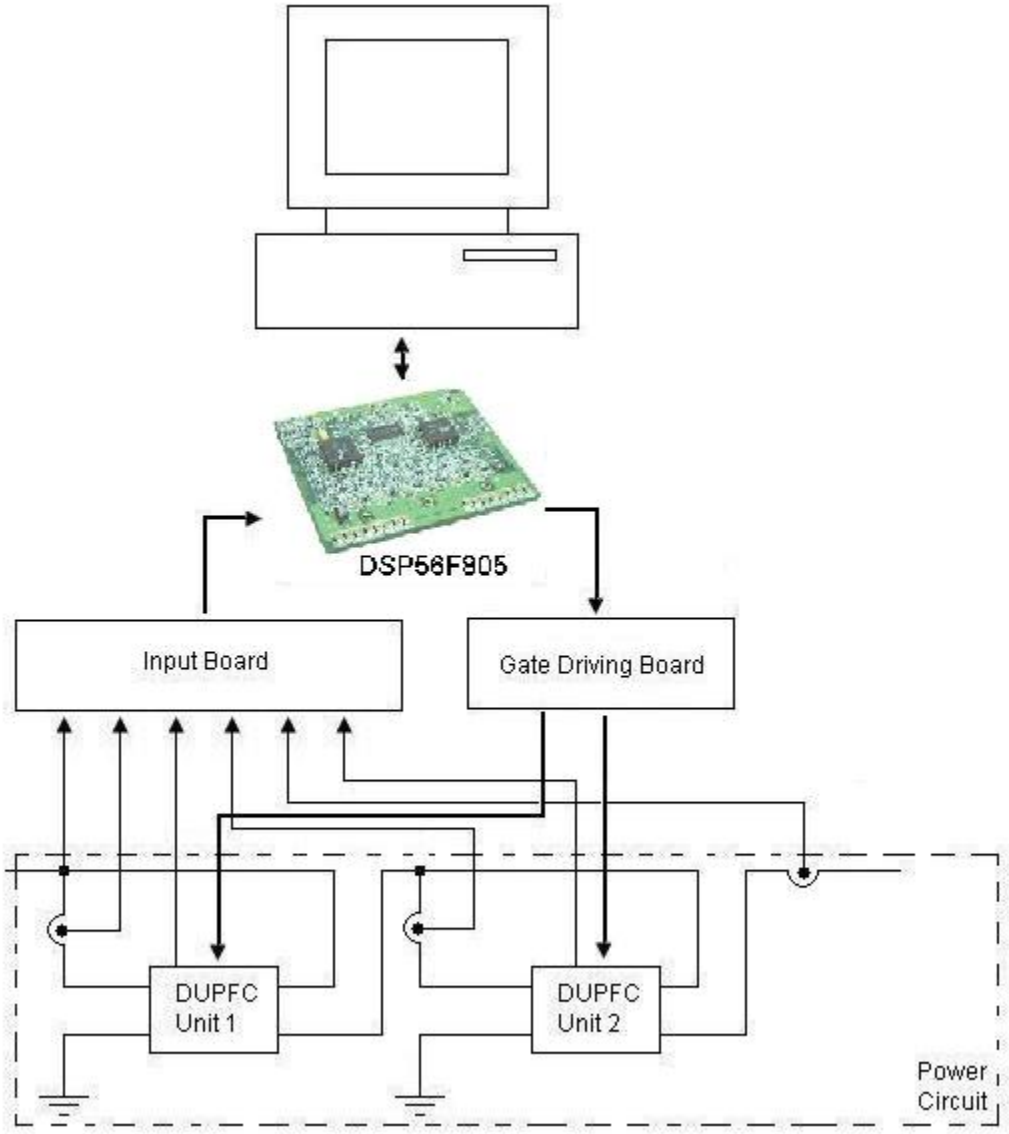


Figure 4.1 Block diagram of the DUPFC lab model

The system consists of four functional blocks: the power circuit, the DSP board, the input board, and the gate driving board. A personal computer is used to program and debug the DSP software. The input board monitors the voltages and the currents in the DUPFC units. It transfers the signals into voltage signals in appropriate voltage level for the DSP board. The DSP board samples signals from the input board through ADC interface port. The proposed control algorithm is implemented in the DSP board. Then, the DSP board produces gating signals for switching devices in the power circuit. The gate driving board receives the gating signals from the DSP board. It amplifies the logic level of the gating signals and provides enough driving capability for the switching devices.

4.1.1 Power circuit

The power circuit is shown in Figure 4.2. Transmission line is divided into two sections. A 3.3mH inductor is used at each section of the transmission line to simulate the inductive effect of the line. Resistance of each of the inductors is measured to be 0.7 ohm. Two DUPFC units are built to control the power flow in the transmission line. Full bridge inverter is used for each of the DUPFC units. MOSFET IRFP350 (VDS=400V, ID=10A) from the International Rectifier® is used as the switching device. An RC snubber circuit is used for each of the switching devices to help switching reverse recovery transient. Two 15uF capacitors are used to remove harmonics from the inverter. Two isolation transformers with turns-ratio of 1:1 are used as the series transformers for the DUPFC units. A third isolation transformer with turns-ratio of 1:1 is used as the shunt transformer for the second DUPFC unit. Two switches are used to connect or disconnect the second unit. When the switch S1 is switched off, and the switch S2 is on, the shunt device of the second DUPFC unit is cut off from the circuit. The series device is shorted through S2. This circuit setup is equivalent to the CUPFC case, where only one unit of the UPFC is operating. When the switch S1 is switched on, and the switch S2 is off, the second DUPFC unit is put into operation along with the first DUPFC unit. Thus, the system has two DUPFC units in operation, which is the DUPFC case.

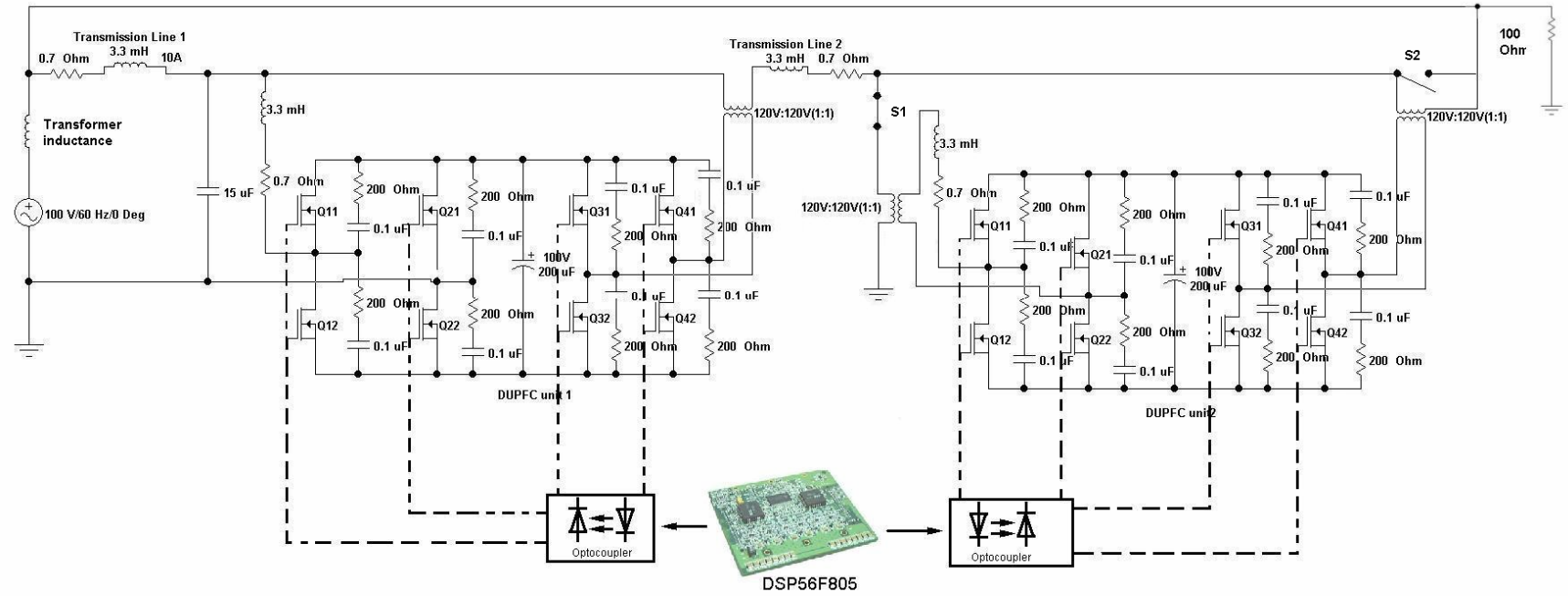


Figure 4.2 Power circuit diagram

4.1.2 DSP56F805EVM board

With considerations of development convenience, performance and cost, the fixed-point digital signal processor DSP56F805 from Motorola is selected. The DSP56F805 is a member of the DSP56800 core-based family of digital signal controllers. It combines the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals on a single chip. The DSP56F805 integrates many peripherals designed particularly for the applications of different motor control, voltage inverters, power line modem, uninterruptible power supplies, automotive control, HVAC applications, fuel management systems, and various industrial control applications.

The 56800 core is based on a Harvard-style architecture consisting of three execution units: the MAC and Arithmetic Logic Unit (ALU) unit, the program counter unit, and the Address Generation Unit (AGU). Those three units operate in a pipelined style, allowing as many as six operations per instruction cycle. The DSP56F805 DSP controller includes 32,252 words (16-bit) of Program Flash, 4K words of Data flash, 512 words of Program RAM, 2K words of Data RAM, and 2k words of Boot Flash. It can execute up to 40 million instructions per second (MIPS) at 80MHz core frequency. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP-and MCU-style applications. The instruction set is also highly efficient for C compilers, enabling rapid development of optimized control applications.

The DSP56F805 has abundant peripheral blocks. It has eight 12-bit Analog-to-Digital Converters (ADC), four quad timer modules, two of them are dedicated general-purpose quad timers with 6 pins, 14 dedicated general purpose IO (GPIO) pins, and 18 multiplexed GPIO pins. The DSP also includes two Pulse Width Modulator (PWM) modules with sufficient output drive capability to directly

drive standard opto-isolators. It also has parallel, serial communication interface module (SPI and SCI), and a scalable Controller Area Network (CAN) [112].

The DSP56F805EVM is an evaluation board based on the DSP56F805 chip. It includes a 56F805 chip, peripheral expansion connectors, external memory and a CAN interface. It is an excellent platform for real-time software and hardware development. The block diagram of the board is shown in Figure 3.2.

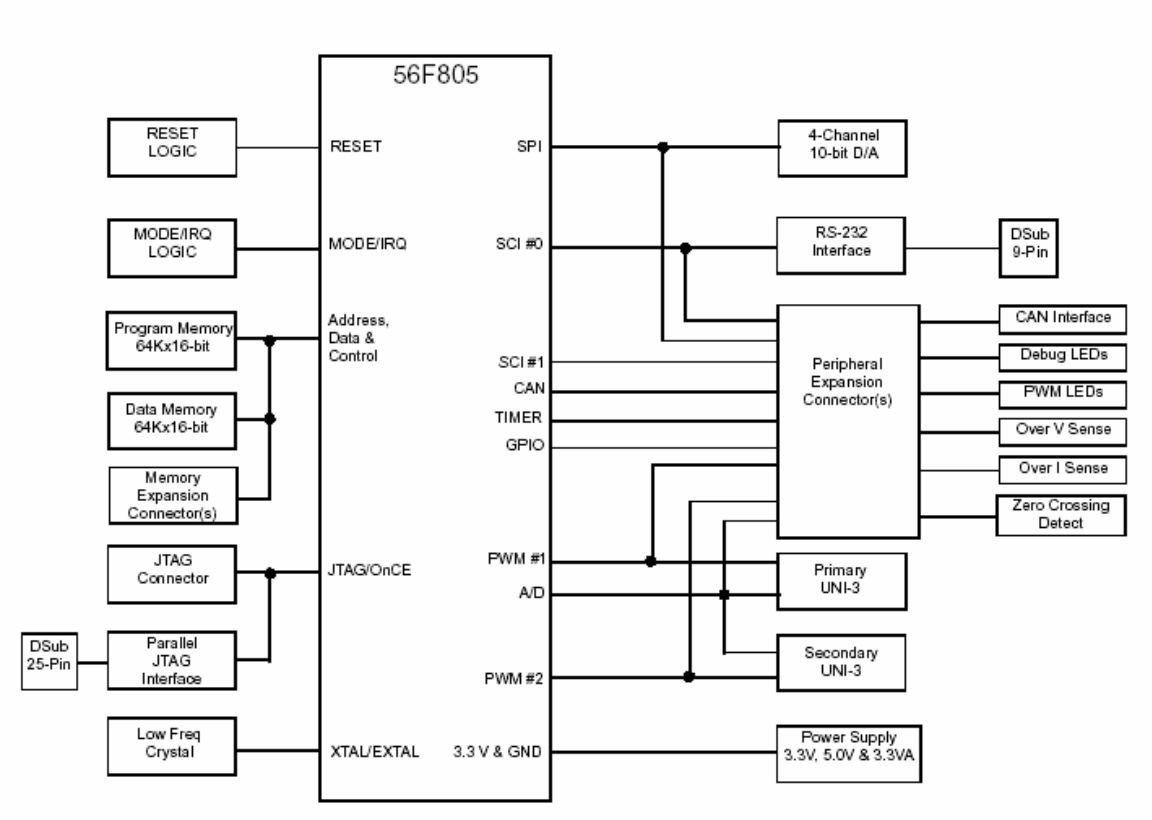


Figure 4.3 Block diagram of the DSP56F805EVM

A developer can use the DSP56F805EVM as a software platform. The user can develop and simulate routines, download the software to on-chip or on-board RAM, run it, and debug it using a debugger via the JTAG/OnCE (On Chip Emulation) port. The board also provides the ability to examine and modify all user accessible registers, memory and peripherals through the OnCE port with the provided software tools.

As a hardware platform, the DSP56F805EVM is flexible, which enables the user to connect external hardware peripherals. At the same time, the on-board peripherals can be disabled, so that the user can reassign the peripherals according to the particular application needs. [113]

4.1.3 Gate driving board

The MOSFET gate driving circuit uses IR2110 from the International Rectifier ®. The IR2110 has floating channel design for bootstrap operation. For each phase leg of the inverter, only one IR2110 IC is needed. The source of the upper MOSFET is floating above the phase leg voltage. Thus, only one DC power supply is necessary for each inverter bridge. Since all the lower MOSFET in a DUPFC unit has the same ground reference, which is the negative node of the DC capacitor, only one DC power supply is needed for each of the DUPFC. In the traditionally used driving circuit, in which every upper switching device needs an isolated DC power supply, at least 5 separate DC power supplies are needed for one DUPFC unit, considering that four lower switching devices can share a same DC power supply. This HVIC design greatly simplifies the gate driving board. Figure 4.4 shows the switching device gating circuit configuration for one inverter. Figure 4.5 illustrates the gating circuit board schematic for one DUPFC unit. It is worthy to mention that the bootstrap diode in the peripheral circuit for the IR2110 should be able to sustain the DC bus voltage. And it should be a fast recovery diode.

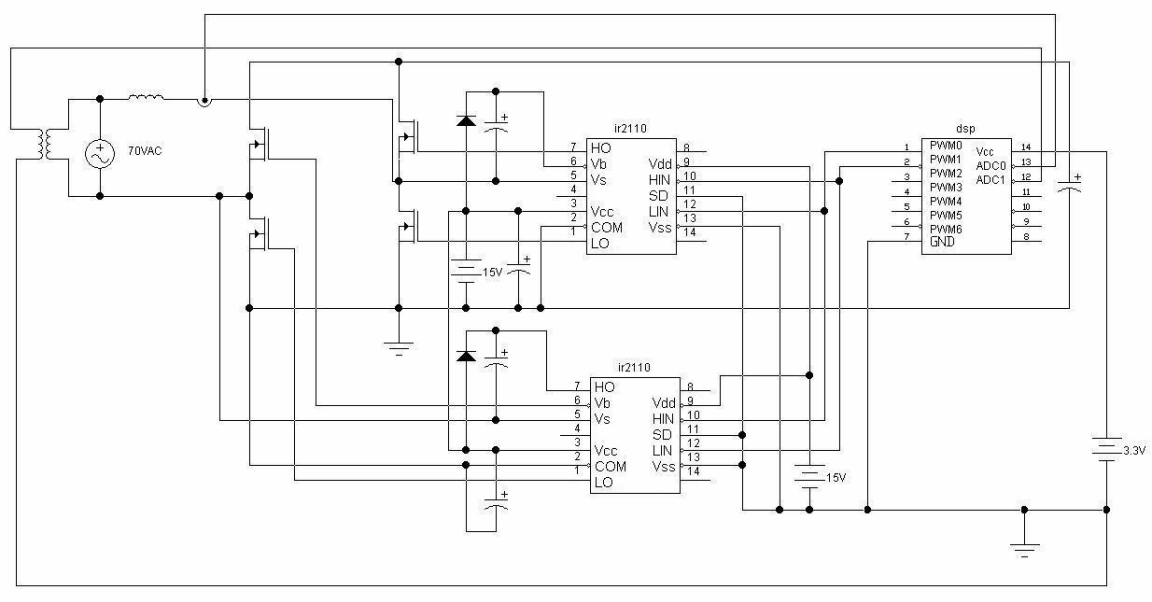


Figure 4.4 Gate driving circuit configuration for each inverter

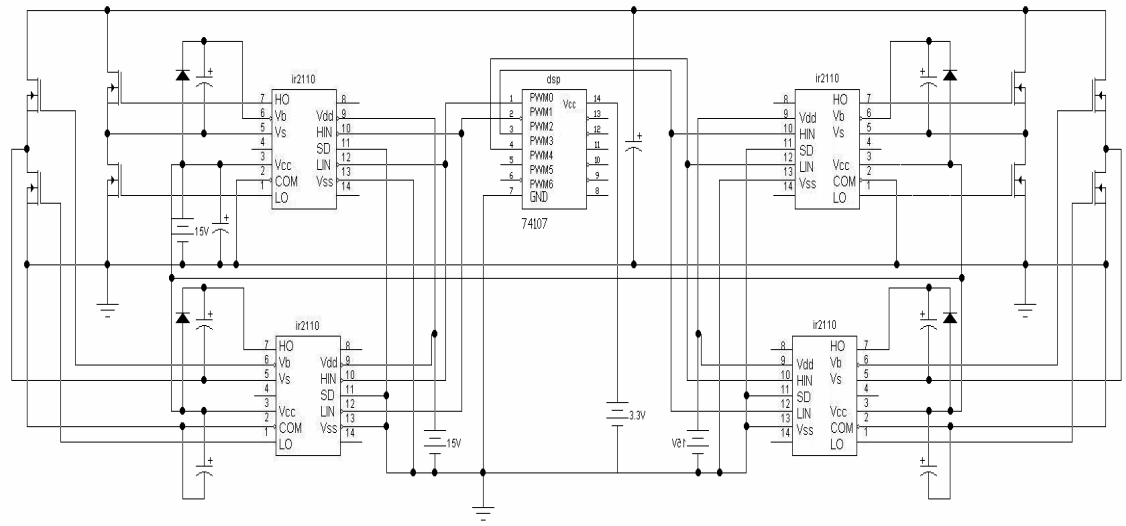


Figure 4.5 Gating circuit schematic for one DUPF unit

4.1.4 Interface board

To implement the closed-loop control algorithm of the UPFC, voltages and currents are sensed at various points in the system. The single-phase AC supply voltages are sensed using potential transformers, scaled properly and conditioned using a low-pass filter to get rid of any distortion. The shunt converter currents (ish1 and ish2) and series converter current (ise,) are sensed using Hall-effect

current sensors. One of the DC capacitor bank voltages is sensed using series connected resistor-divider. The other DC capacitor bank voltage is sensed using high Common Mode Rejection (CMR) isolation amplifier - HCPL7800. The HCPL7800 provides stable and accurate signal amplification with high noise immunity. The functional diagram of the HCPL7800 is illustrated in Figure 4.6. The analog optocoupler in the chip provides effective isolation between the measured high voltage signal and lower power electrical circuit. All the scaling circuits are designed and tested to match the signal range of the ADC ports of the DSP. The circuit diagram of the interface board is depicted in Figure 4.7.

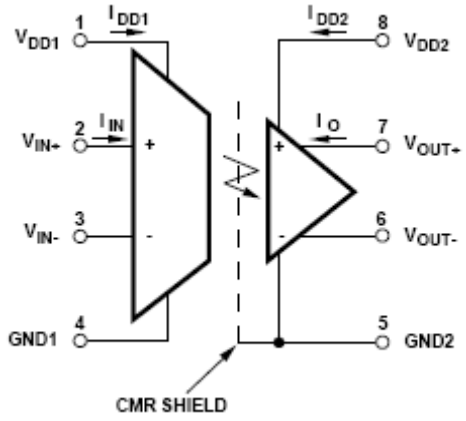


Figure 4.6 Functional diagrm of the HCPL7800 [114]

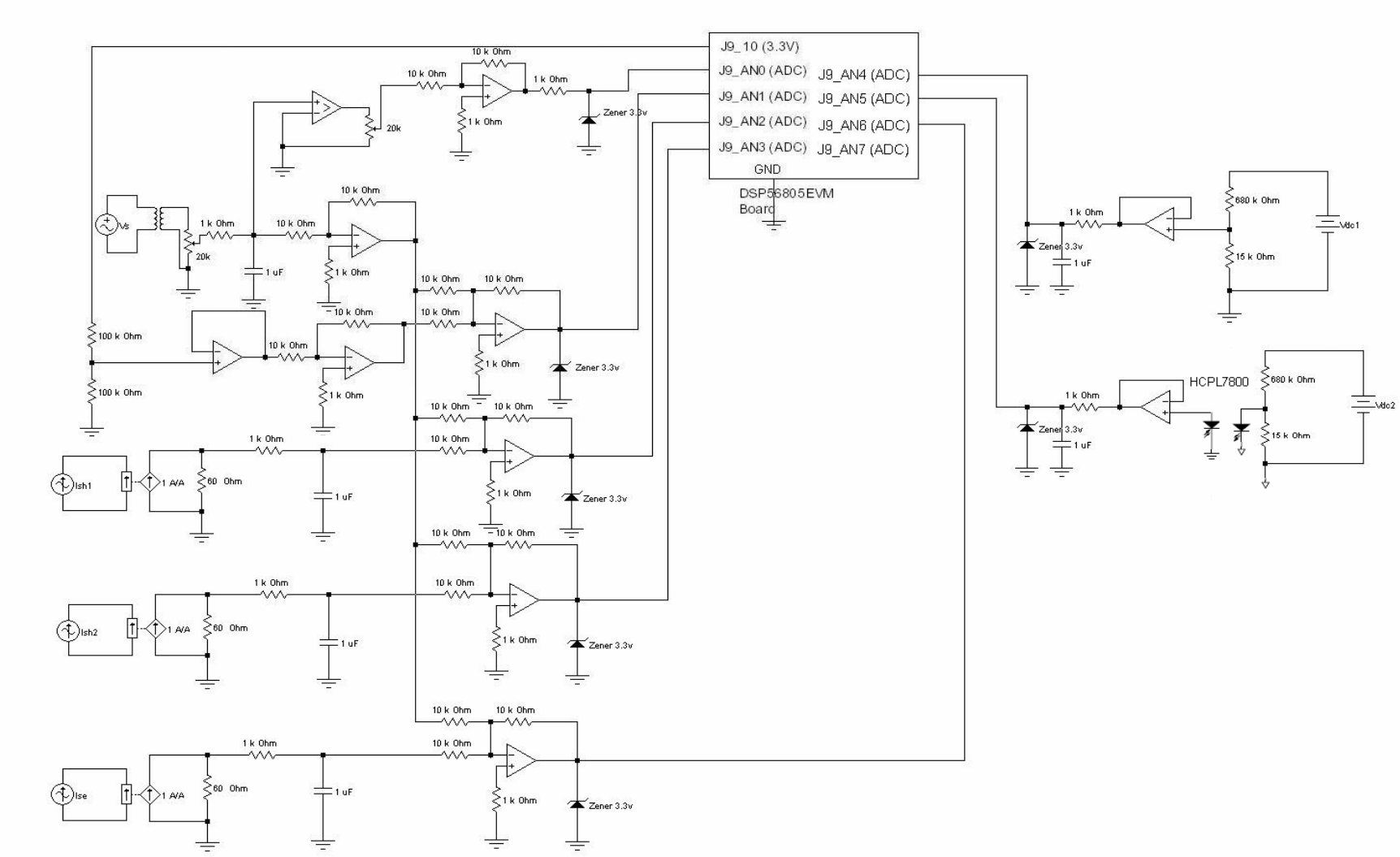


Figure 4.7 Diagram of the interface board

4.2 Software design

4.2.1 Code Warrior and Embedded Beans

The Code Warrior Integrated Development Environment (IDE) from Freescale Semiconductor© provides a set of convenient developing and debugging tools using a graphical user interface (GUI). In this IDE, projects and files can be managed and developed efficiently.

The Code Warrior also integrates a powerful embedded system development tool called the Processor Expert as a plug-in. This tool can generate codes automatically from the Embedded Beans. The Embedded Beans encapsulate the functions of the most commonly used elements, such as CPU core, CPU on-chip peripherals, standalone peripherals, and software algorithms. Like the objects in the Object Oriented Programming (OOP), the embedded beans have properties, methods, and events. With this developing tool, the embedded system developer only need to drag and drop needed beans in the Bean Inspector, like instantiating a object in OOP. By graphically setting up the parameters of the beans, the Processor Expert will automatically generate the necessary initializing and functioning codes. The Embedded Beans also facilitate the peripheral arrangement and setup. For every internal and external peripheral, there's a corresponded embedded beans available for application. The necessary setup for the peripheral is included in the bean. All the generated codes in the embedded beans are tested and verified. Thus, the tool saves a lot developing time for the programmers. The software developer can focus on higher level functionality of the program, not the detailed peripheral configuration. Figure 4.8 illustrates the snap shot of the development environment.

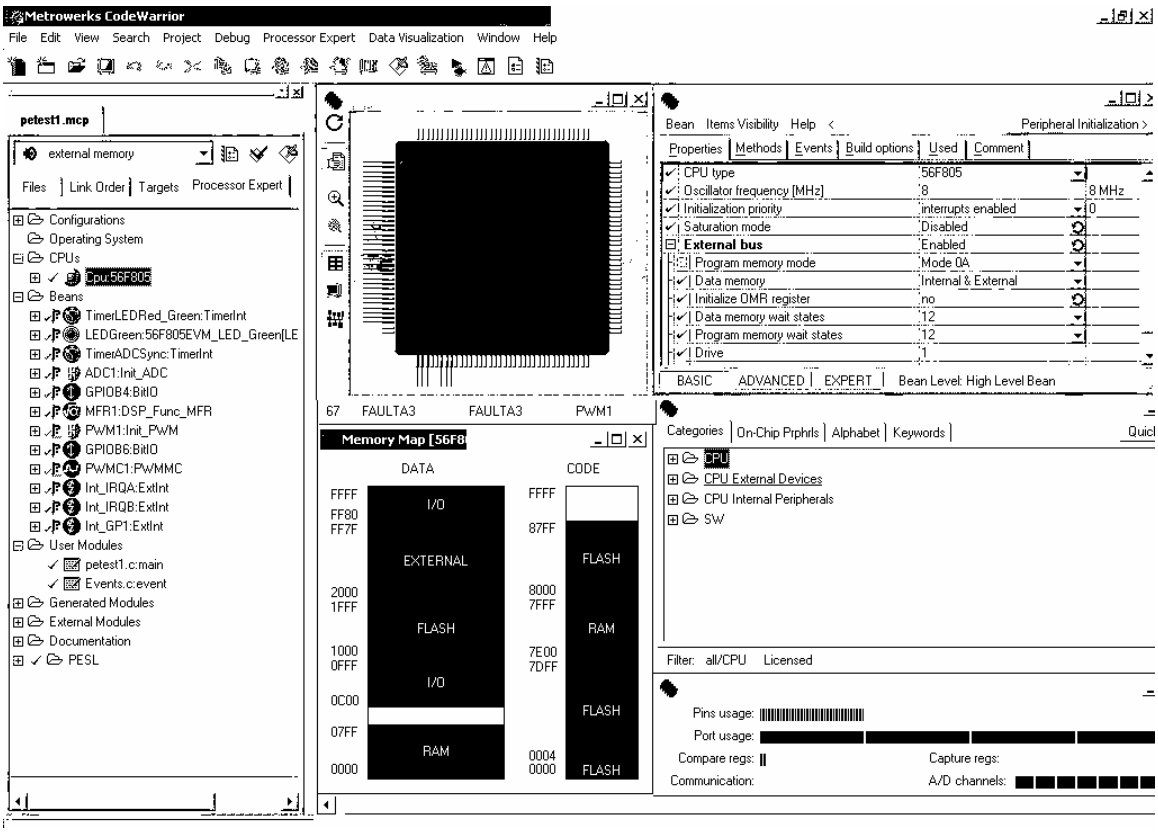


Figure 4.8 Code Warrior IDE with Processor Expert

4.2.2 Signal expression in the DSP56F805

The DSP56F805 is a fixed-point digital signal processor. All the variables in the software are expressed in 16 bit words or 32 bit long words. The 16 bit data can be expressed as signed or unsigned integer, or signed or unsigned fractional values. A 16 bit signed integer lies in the range from -32768(0x8000) to 32767(0x7fff). A 16 bit signed fractional value lies in the range of -1.0(0x8000) to 1.0-2-15(0x7fff). In the program, sampled data is scaled to be in expressible range for the 16 bit words. The peak value of the maximum possible input signal is scaled to be the maximum integer value. For example, the maximum source voltage peak value is rated to be 140 volts (100 Vrms). When the source voltage is 140 volts, the sampled voltage can be scaled to be 32768. Figure 4.9 depicts the sampling result for the 100 Vrms source voltage. It can be seen that the sampled voltage is not perfectly symmetric. The error may come from the transformer imperfection, or the ADC errors. Table 4.1 illustrates the relationship

between the integer numbers in the DSP and the real voltage and current measured values in this experimental setup.

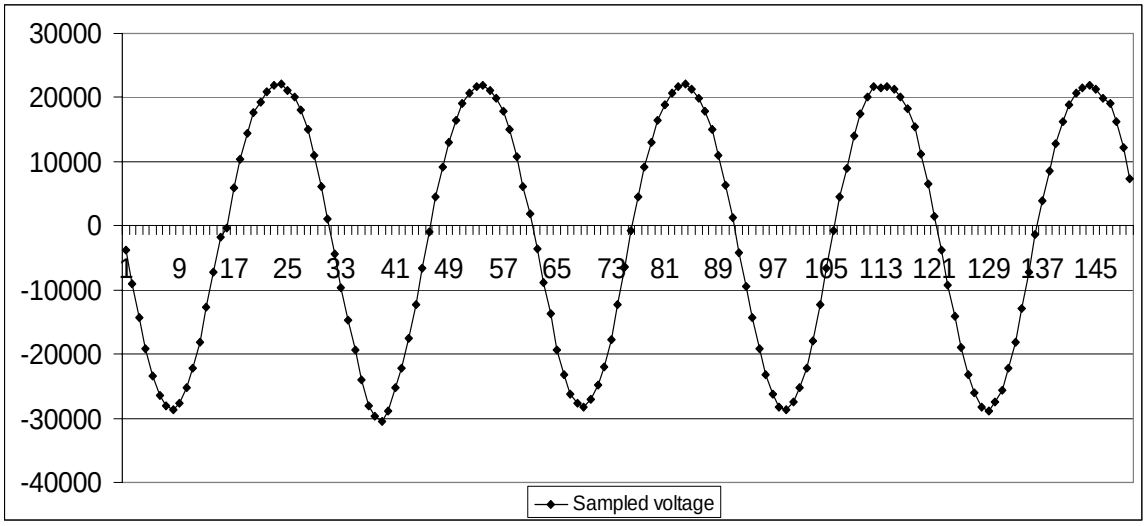


Figure 4.9 Signals are properly scaled

Table 4.1 Relationship between sampled signals and the real values

Voltage		**Current**	
Numbers in DSP	Real Value	Numbers in DSP	Real Value
30000	140 V	30000	20 A
10000	47 V	10000	6.6 A
5000	16.7 V	5000	3.3 A
0	0 V	0	0 A
-5000	-16.7 V	-5000	-3.3 A
-10000	-47 V	-10000	-6.6 A
-30000	-140 V	-30000	-20 A

4.2.3 Software design

The flow chart of the DSP program is shown in Figure 4.10. The main part of the program codes are listed in the appendix A.

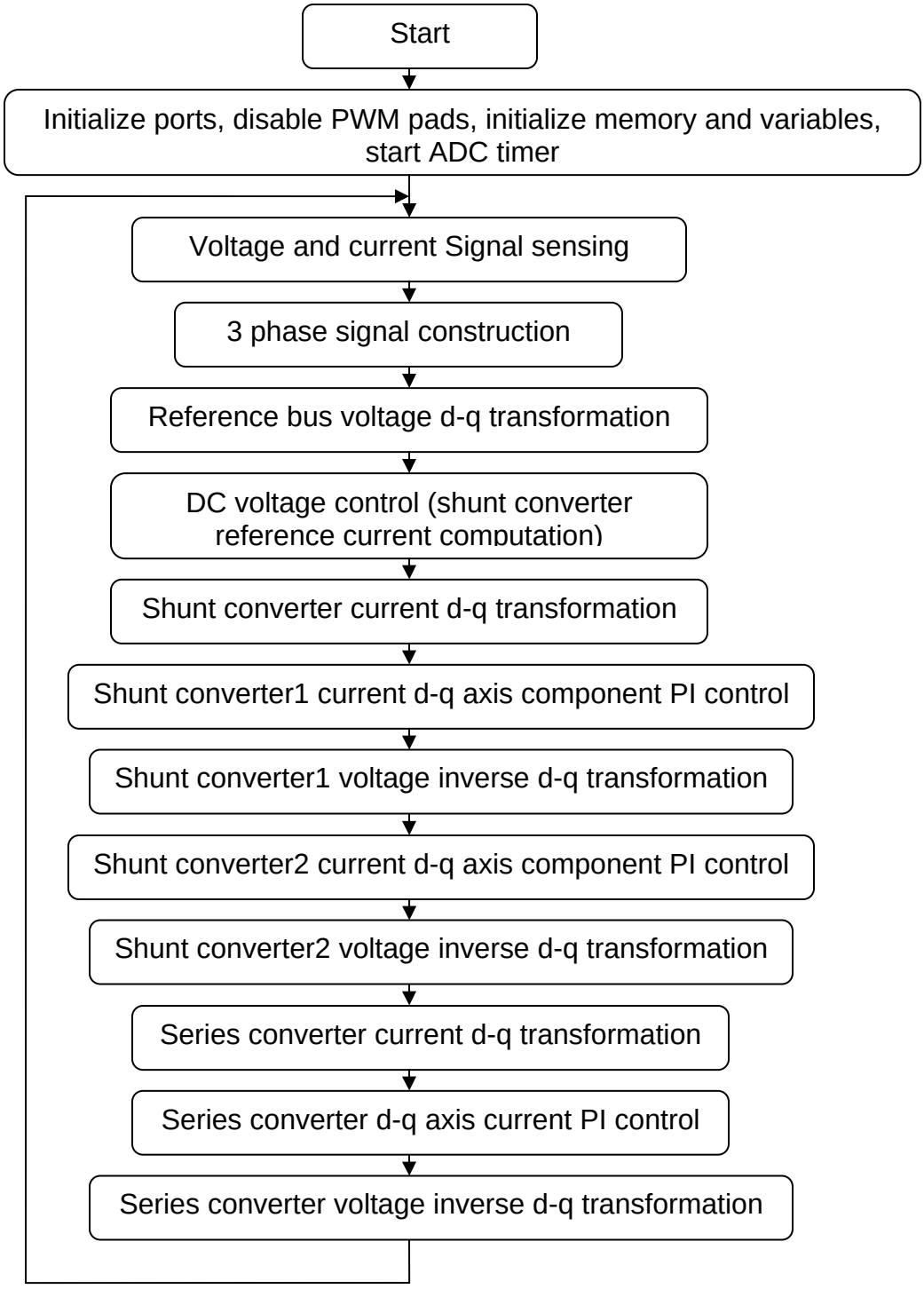


Figure 4.10 Flow chart of the DSP program

4.3 Experimental results

4.3.1 Construction of the three phase system from single-phase signals

The d-q transformation is based on three phase signals. The delay method is used to construct three phase signals from the sampled single phase signal. Figure 4.11 depicts the process to construct the three phase signals. Figure 4.12 illustrates the constructed three phase voltage from the single-phase source voltage at different voltage level. In the case of 100V, the sampled voltage signal has DC component. This DC component can bring harmonics in the d-q components of the signals.

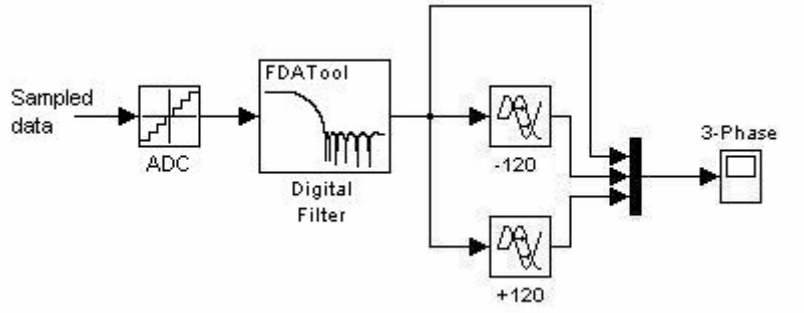
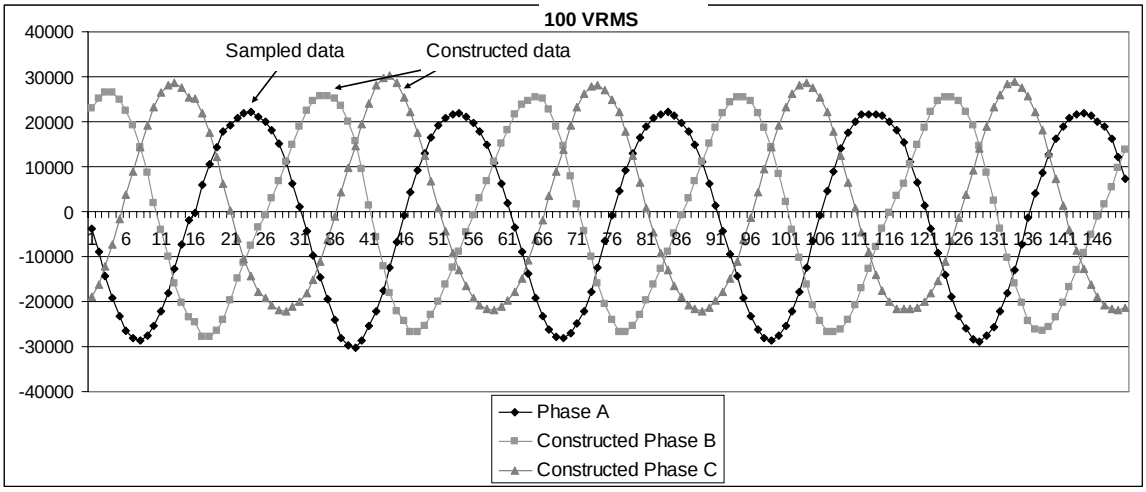
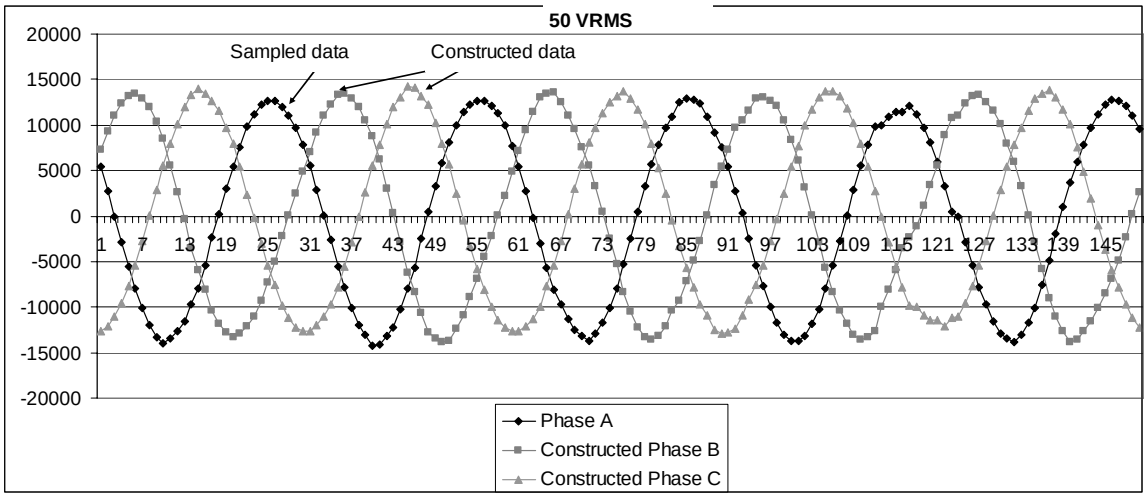


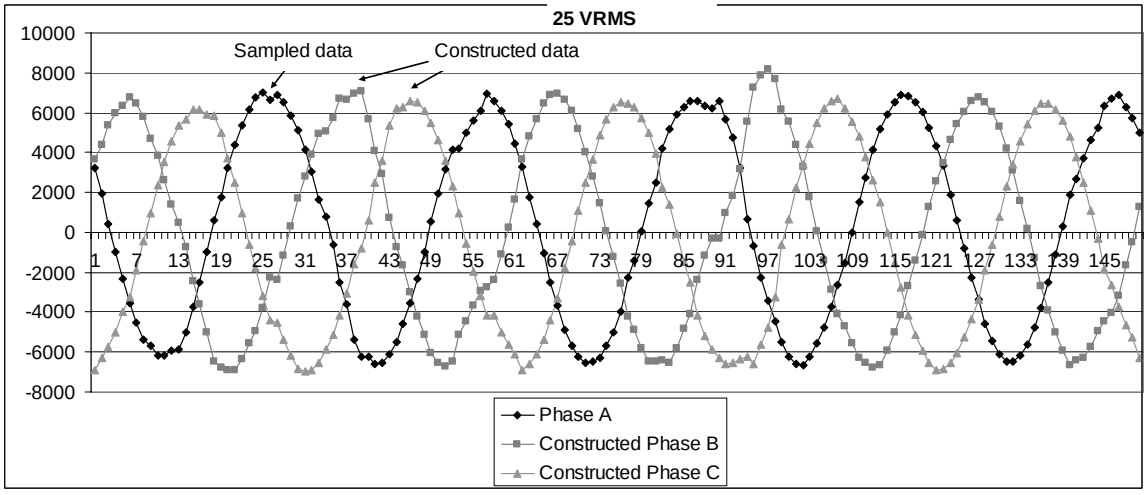
Figure 4.11 Three-phase construction from single-phase signals



(a)



(b)



(c)

Figure 4.12 (a) Constructed three-phase source voltage, V = $100V_{rms}$
(b) constructed three phase source voltage, V = $50V_{rms}$
(c) constructed three phase source voltage, V = $25V_{rms}$

4.3.2 Digital filter

To remove the noise in the sampled signals, it is critical to use proper digital filters in DSP application. A digital filter acts on the data after it has been sampled and digitized. In the DSP algorithm, a 4 point moving average filter was used to remove the noises from the sampled signals. A moving average filter is effective in removing random noise while keeping the sharpest response. [115] Figure 4.13

depicts the sampled source voltage before and after the moving average filter. The filter removes the noise in the sampled signal with acceptable phase delay.

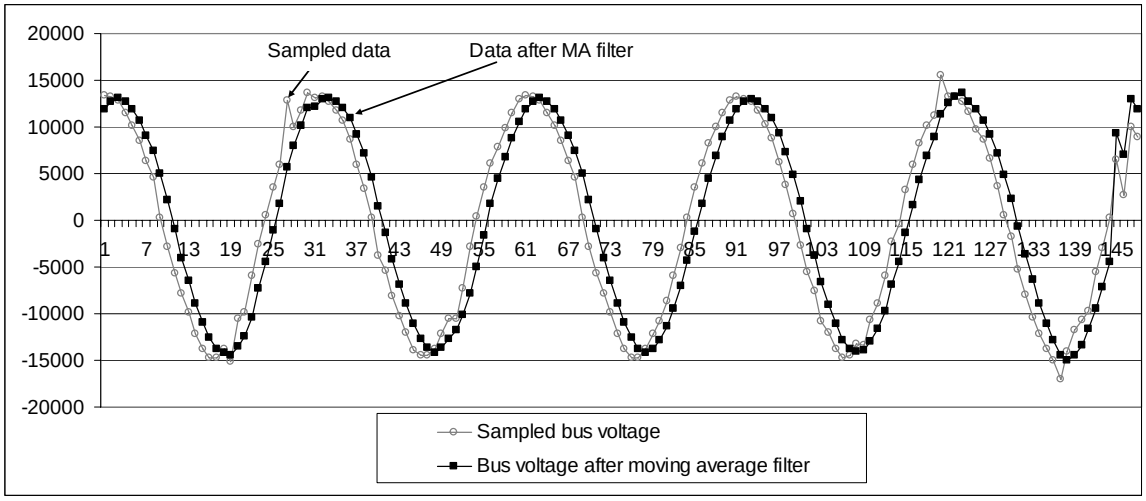


Figure 4.13 Sampled bus voltage data and data after the moving average filter

Since the control algorithm is based on proper calculated d-q quantities. Harmonics and noises will affect the performance of the controller. Theoretically, after d-q transformation, sinusoidal signals are transformed to DC variables. However, due to unbalance of three phase signals, sampling noise, quantization and digitization errors, and precision limitation of the fixed point DSP, it is unavoidable that harmonics and noises exist in the d-q quantities. To remove those harmonics, a first order low pass filter is used in the program.

For a first order low-pass filter,

$$\frac{dx}{dt} = \frac{-x}{T} + \frac{Vin}{T} \tag{1}$$

In discrete format,

$$\frac{x(t+\Delta t) - x(t)}{\Delta t} = \frac{-x(t)}{T} + \frac{Vin(t)}{T} \tag{2}$$

After some simple derivation, it can be obtained that

$$x(n) = (1 - \frac{\Delta t}{T})x(n-1) + \frac{\Delta t}{T}Vin(n) \quad (3)$$

where, x(n) is the current filter output. X(n-1) is the previous state. Δt is the DSP sampling period. $T = \frac{1}{f}$ is the period of the cut-off frequency. Vin(n) is the current sampled input signal.

After the d-q transformation, it is necessary to remove the second harmonic of the line frequency. So, the cut off frequency is chosen to be 120 Hz. In the DSP application, the sampling frequency is set to 1800 Hz. So, the filter function is calculated to be:

$$x(n) = 0.5811x(n-1) + 0.4189Vin(n) \quad (4)$$

Figure 4.14 shows the calculated d and q axis components of the source voltage of 50V with and without the first order digital filter. Obviously, the filter removes unnecessary harmonics and noise.

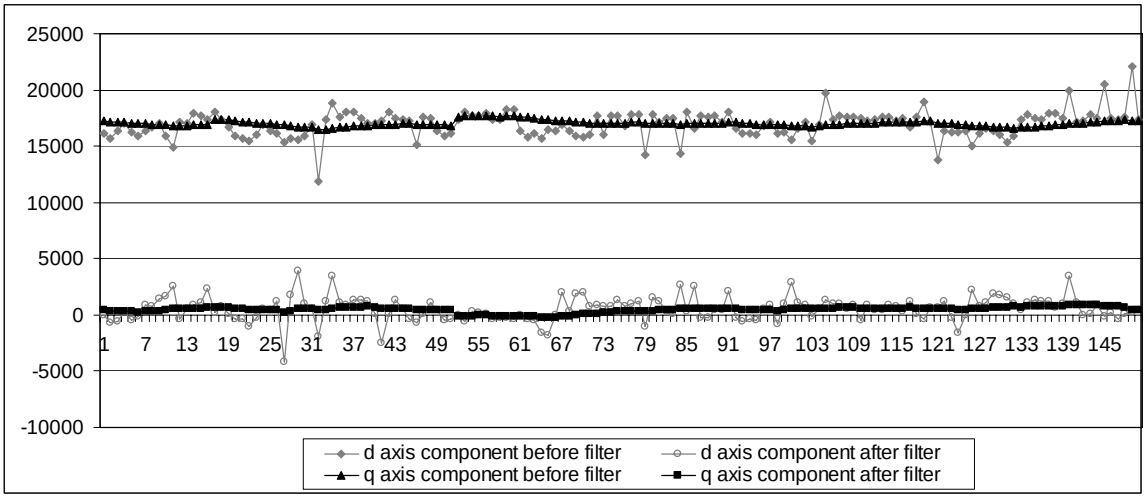


Figure 4.14 d-q components of the source voltage before and after the first order digital filter

4.3.3 Experimental result

In this section, two DUPFC units are built and tested. Closed-loop system for series converter, shunt converter, and the DC voltage control is implemented. Both the measured plots from the oscilloscope and the recorded data from the DSP are given. Both positive and negative real and reactive power flow are tested in different experimental setups.

4.3.3.1 Series converter closed-loop current control

The series converter closed-loop control algorithm is implemented as given in Figure 2.33. The AC bus voltage is adjusted to 100 volts. The DC voltages are controlled to be 180 volts, which is illustrated in section 4.3.4.3. The integral and proportional gains for the PI controller are selected as:

k_{ise} = 0x0100;

k_{pse} = 0x0100.

Case 1: positive reactive power flow

The d-q axis control command of the series converters current is set to $I_d = 0$, and $i_q = 10000$ ($I_{rms} = 6.6A$). The AC bus voltage and the series converter current are illustrated as in Figure 4.15. The synchronizing signal and the calculated d, q components of the series converter current are plotted as in Figure 4.16. The d, q components follows their respective commands well.

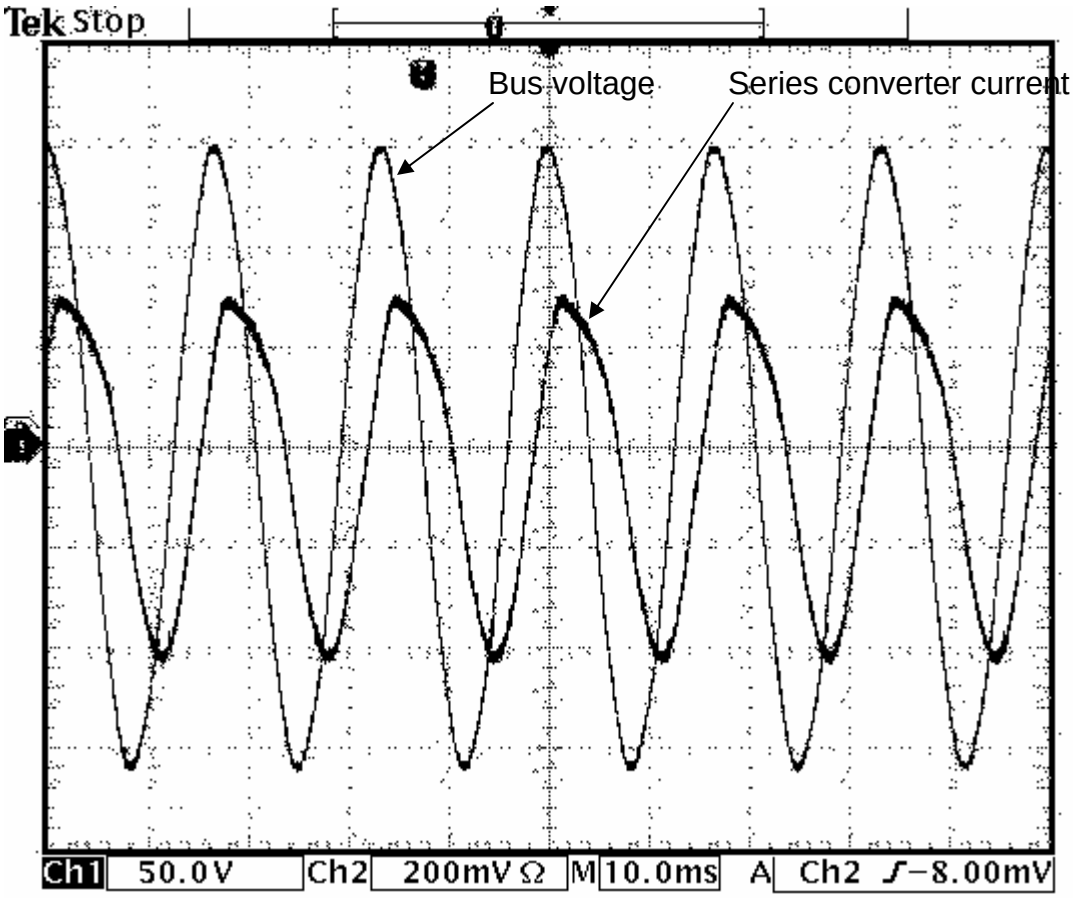


Figure 4.15 Bus voltage and the series converter current with lagging power factor

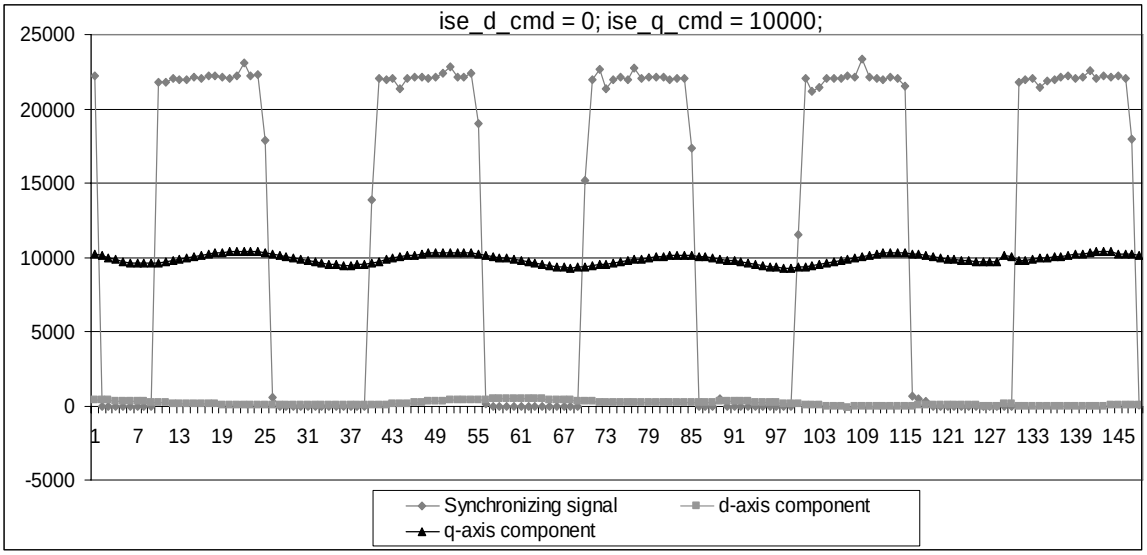


Figure 4.16 Series converter current d-q axis components with lagging power factor

Case 2: negative reactive power flow

In this case, the d-q axis control command of the series converters current is set to I_d = 0, and i_q = -10000 (I_{rms} = 6.6A). The bus voltage and the series converter current are illustrated in Figure 4.17. The synchronizing signal and the calculated d, q components of the series converter current are plotted as in Figure 4.18. The d, q components follows their respective command well.

Case 3: positive real power flow

The d-q axis control command of the series converters current is set to I_d = 13000, and I_q = 0 (I_{rms} = 8.8A). The bus voltage and the series converter current are illustrated in Figure 4.19. The synchronizing signal and the calculated d, q components of the series converter current are plotted as in Figure 4.20. In this case, the transmission line current has a small phase angle error. This error comes from analog and digital filters, sampling errors, and other factors in the system. However, the d, q components follows their respective command with negligible errors.

Case 4: negative real power flow

The d-q axis control command of the series converters current is set to I_d = -13000, and I_q = 0 (I_{rms} = 8.8A). The bus voltage and the series converter current are illustrated in Figure 4.21. The synchronizing signal and the calculated d, q components of the series converter current are plotted as in Figure 4.22. The d, q components follows their respective command well.

From the recorded data from the DSP, it can be seen that the controlled current components have harmonics of the fundamental frequency. This fluctuation can be from the measured phase angle error, measured signal error, and from the delay effect of the analog and digital low pass filters used in the hardware and software implementation.

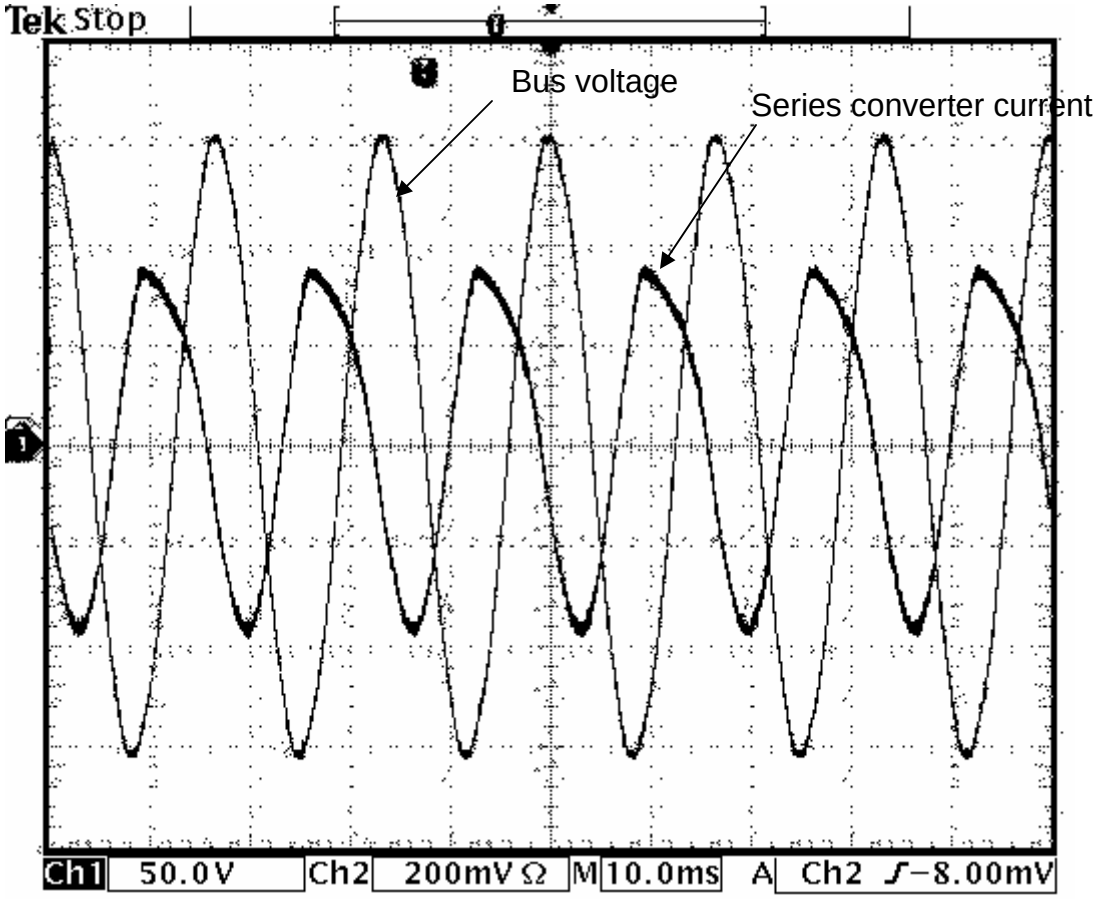


Figure 4.17 Bus voltage and the series converter current with leading power factor

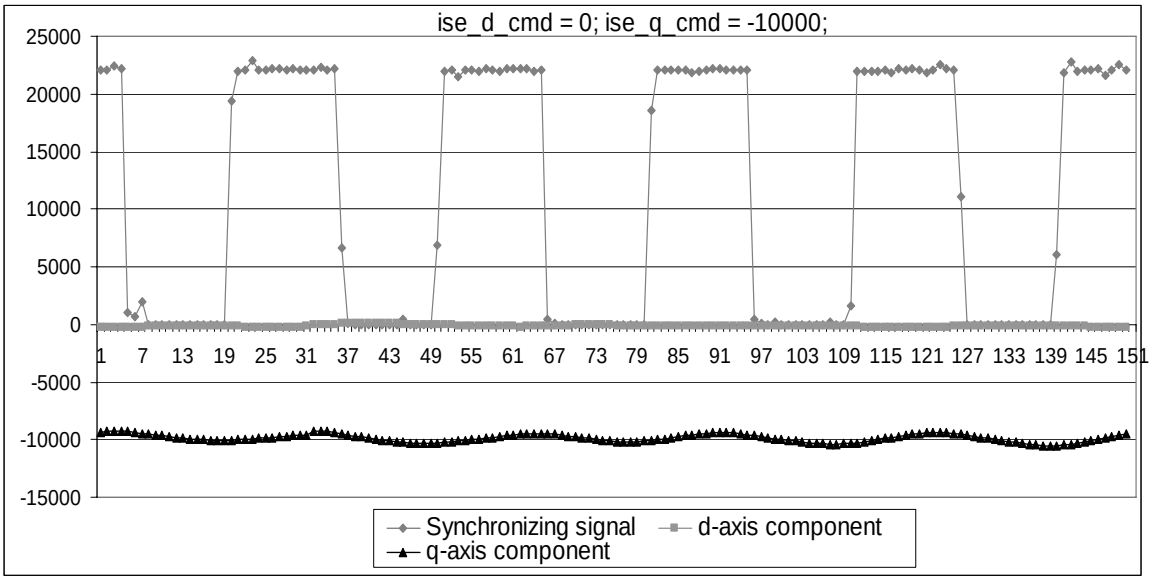


Figure 4.18 Series converter current d-q axis components with leading power factor

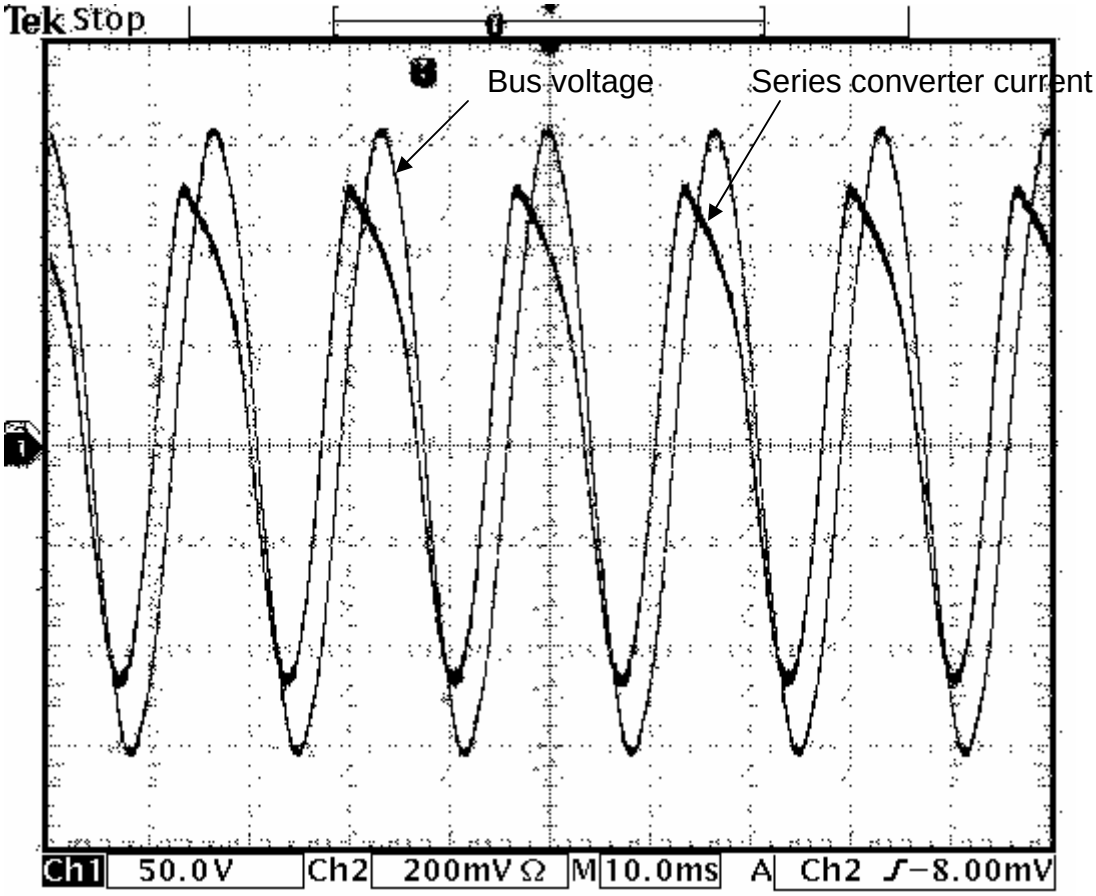


Figure 4.19 Bus voltage and the series converter current with positive real power flow

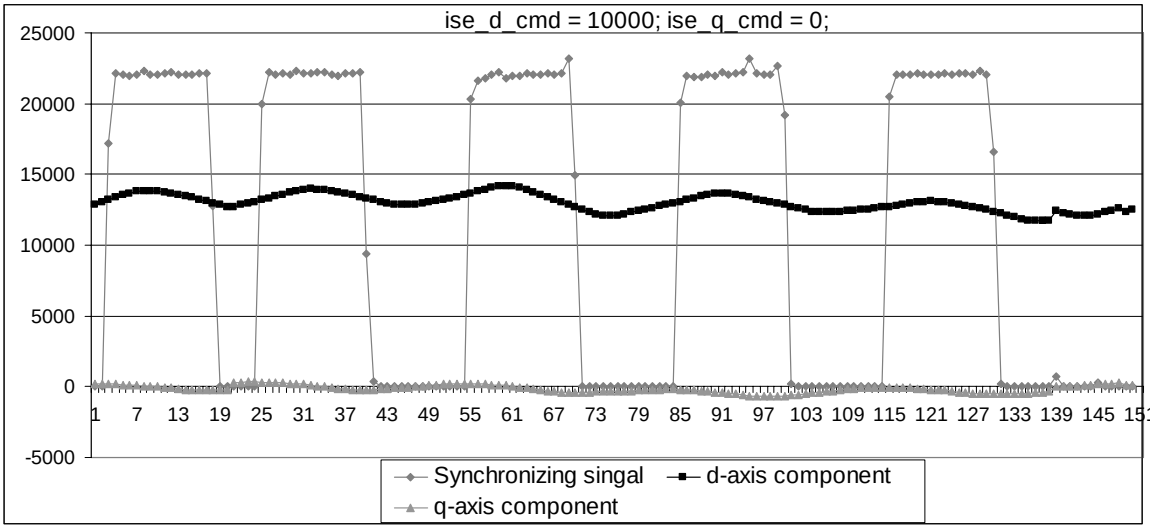


Figure 4.20 Series converter current d-q axis components with positive real power flow

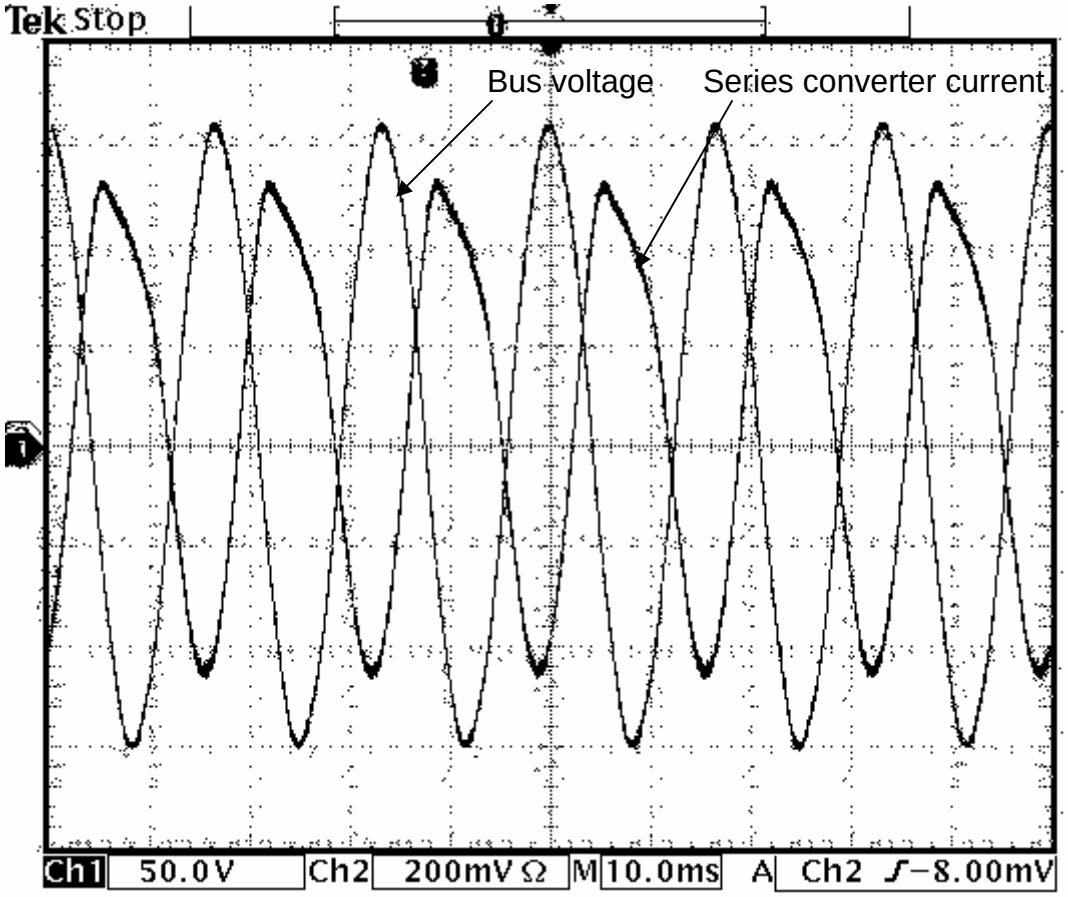


Figure 4.21 Bus voltage and the series converter current with negative real power flow

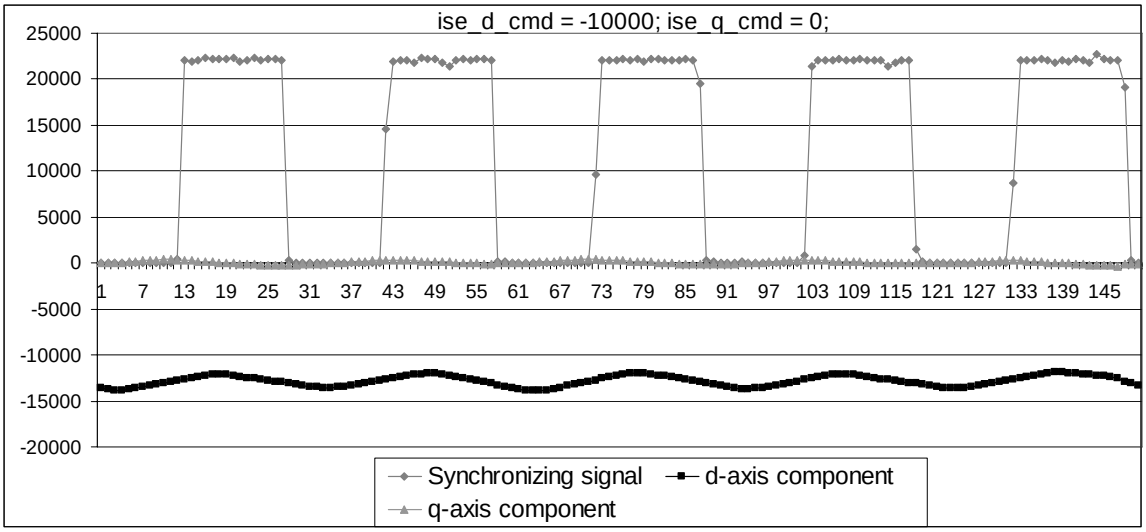


Figure 4.22 Series converter current d-q axis components with negative real power flow

4.3.3.2 Shunt converter closed-loop current control

The shunt converter closed-loop control algorithm is implemented as given in section 2.4.4. The PI controller parameters are selected as:

k_{ish} = 0x00E0;

k_{psh} = 0x0010.

Case 1: positive reactive power flow

The d-q axis control command of the shunt converter current is set to I_d = 0, and I_q = 5000 (I_{rms} = 3.3A). The source voltage and the shunt converter current are depicted in Figure 4.23. The synchronizing signal and the calculated d, q components of the shunt converter current are plotted as in Figure 4.24. The d, q components follows their respective command well.

Case 2: negative reactive power flow

The d-q axis control command of the shunt converter current is set to I_d = 0, and I_q = -5000 (I_{rms} = 3.3A). The source voltage and the shunt converter current are shown in Figure 4.25. The synchronizing signal and the calculated d, q components of the shunt converter current are plotted as in Figure 4.26. The d, q components follows their respective command well.

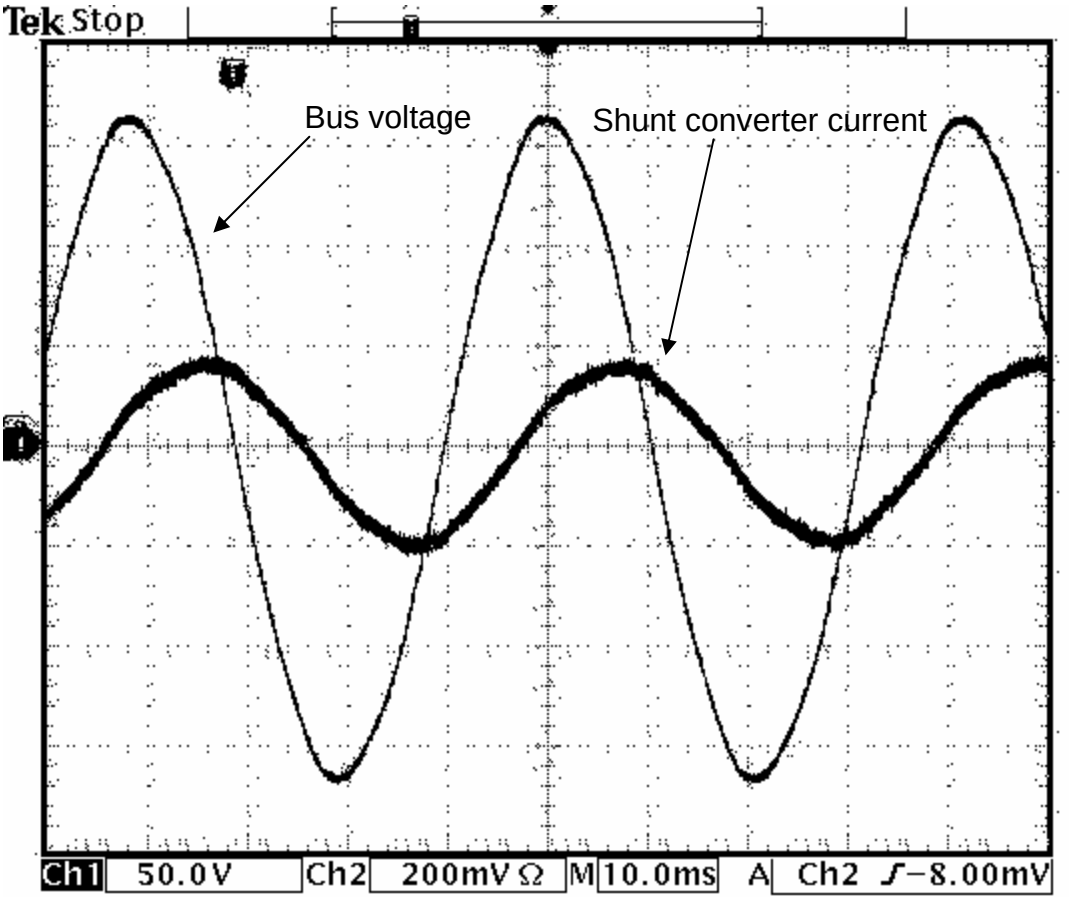


Figure 4.23 Bus voltage and the shunt converter current with lagging power factor

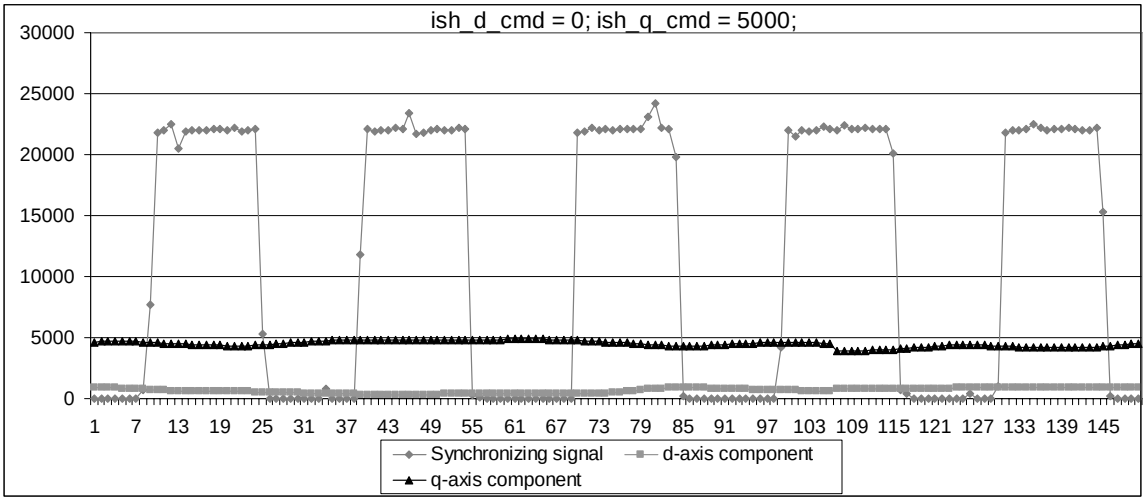


Figure 4.24 Shunt converter current d-q axis components with lagging power factor

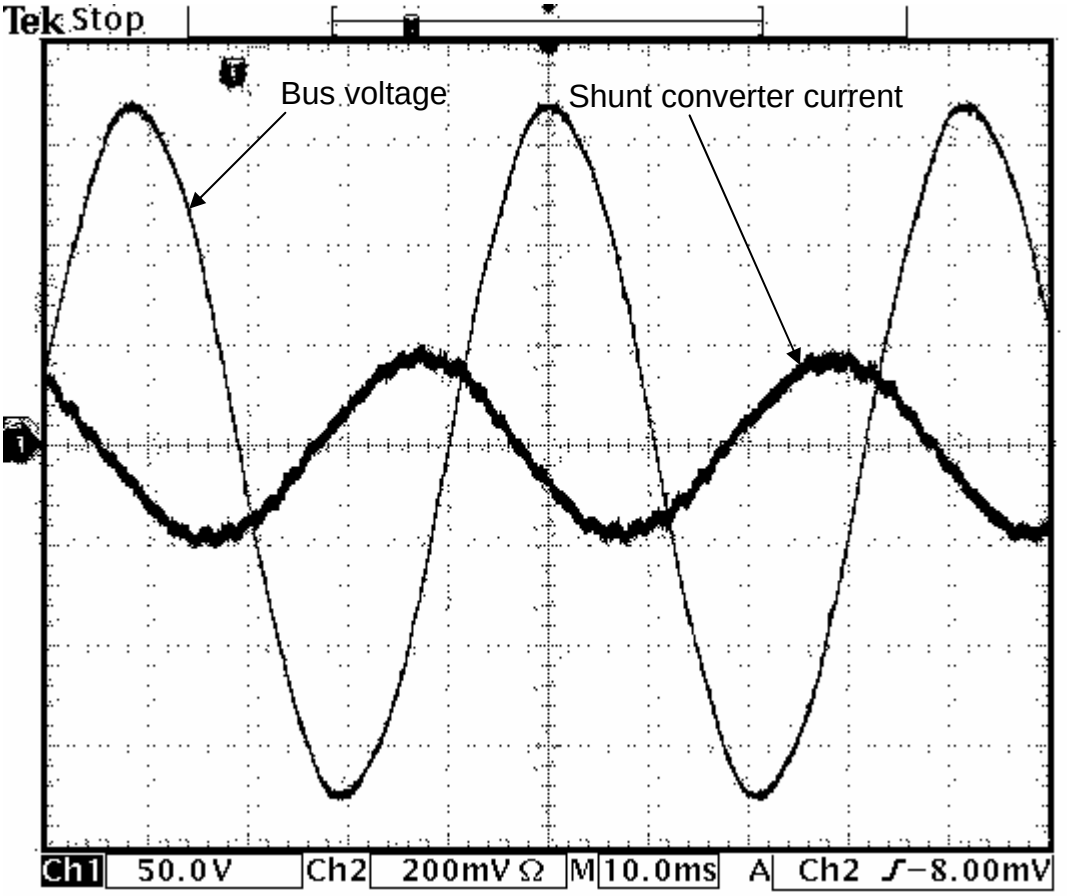


Figure 4.25 Bus voltage and the shunt converter current with leading power factor

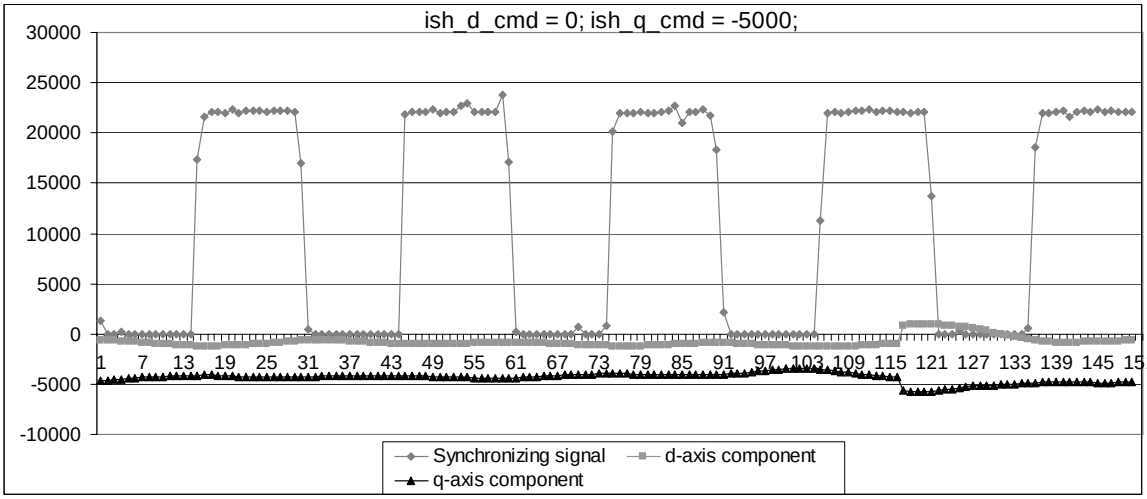


Figure 4.26 Shunt converter current d-q axis components with leading power factor

4.3.3.3 DC voltage control

Two DC capacitor banks of 1mF are used. The DC voltages are controlled to be 150 volts using a PI controller. The integral and proportional gains for the PI controller are:

k_{iDC} = 0x0014;

k_{pDC} = 0x0100.

The DC capacitor voltages taken from the oscilloscope are shown in Figure 4.27 and Figure 4.28. The measured DC capacitor voltages in DSP are illustrated in Figure 4.29.

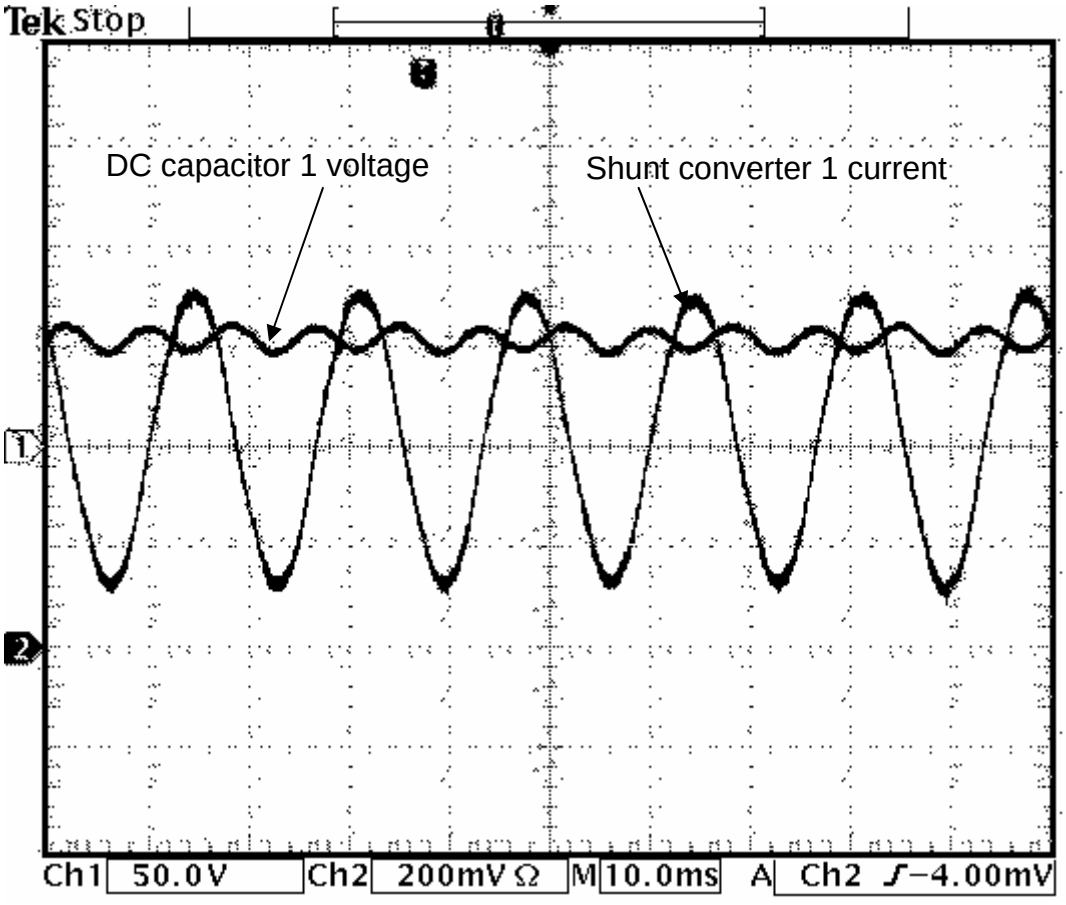


Figure 4.27 DC capacitor voltage 1 and shunt converter 1 current

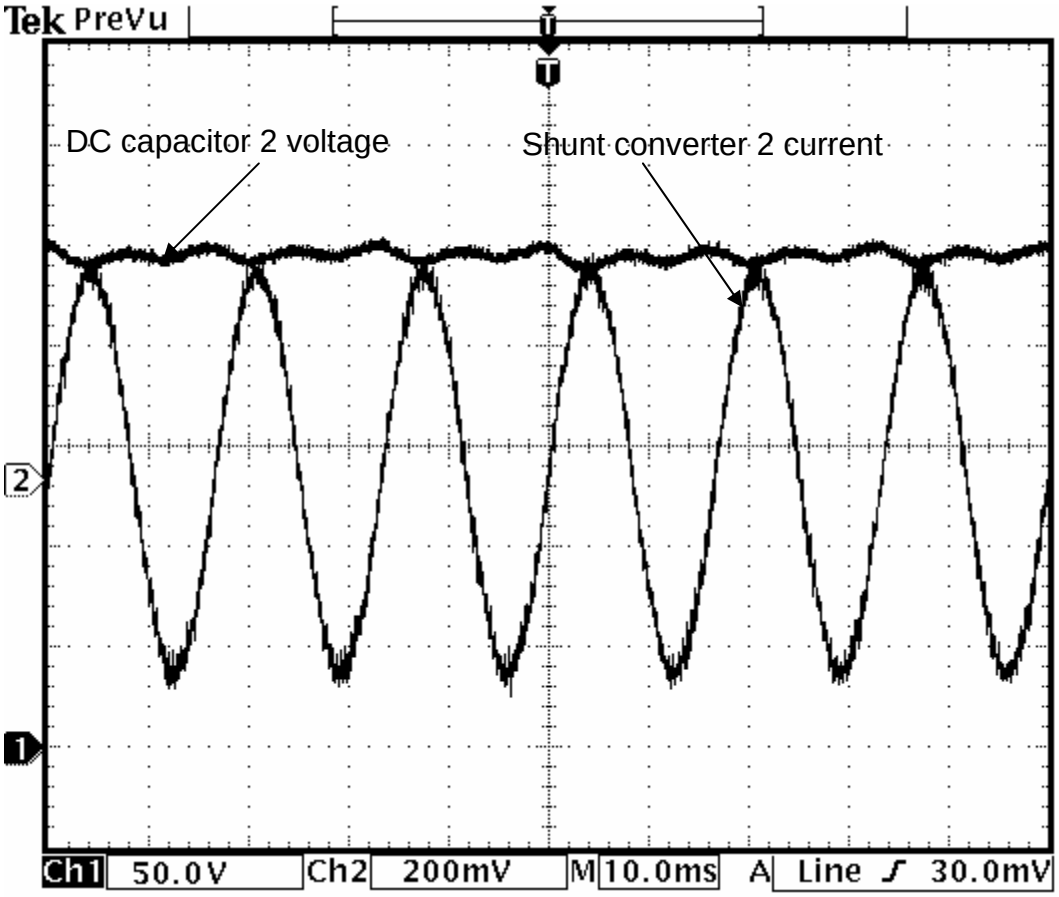


Figure 4.28 DC capacitor voltage 2 and shunt converter 2 current

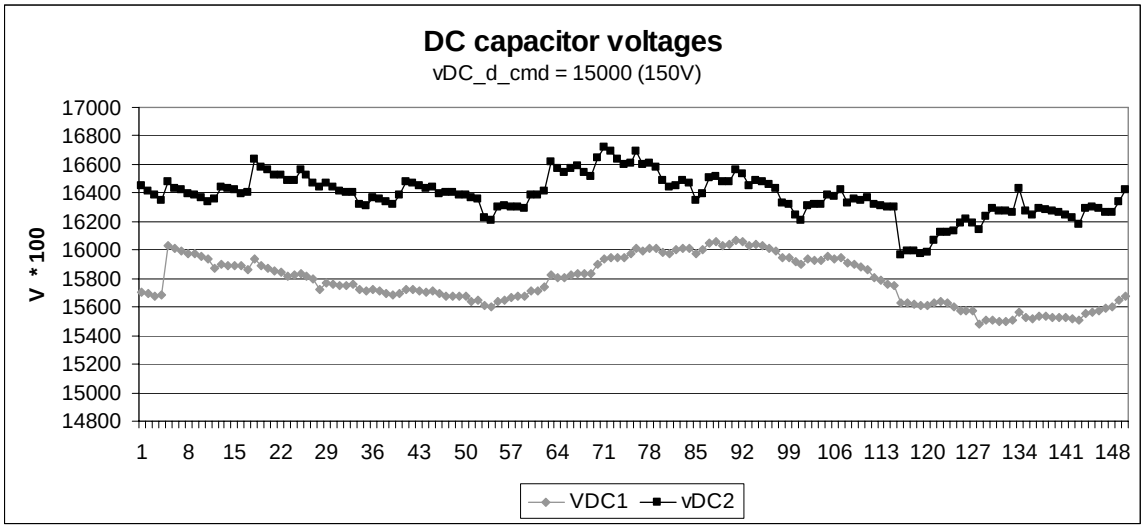


Figure 4.29 Recorded DC capacitor voltages

4.3.3.4 Two cases with CUPFC and two-unit DUPFC

(1) CUPFC case

In this case, the switch S1 is off, the switch S2 is on. The second DUPFC unit was disconnect from the system. Thus, this operation would be the CUPFC case. The power supply voltage was adjusted to 100 V. The series branch current command was selected to be I_{sed} = -1000, and I_{seq} = 5000 (I_{rms} = 3.4A real power flow from receiving end bus to sending end bus). The bus voltage and the series branch current are depicted in Figure 4.30. The injected series branch voltage is shown in Figure 4.31. The bus voltage with and without the UPFC, and the shunt branch current are illustrated in Figure 4.32. Figure 4.33 shows the d and q axis components (real and reactive components) of the measured series branch current. The measured bus voltage magnitude is shown in Figure 4.34.

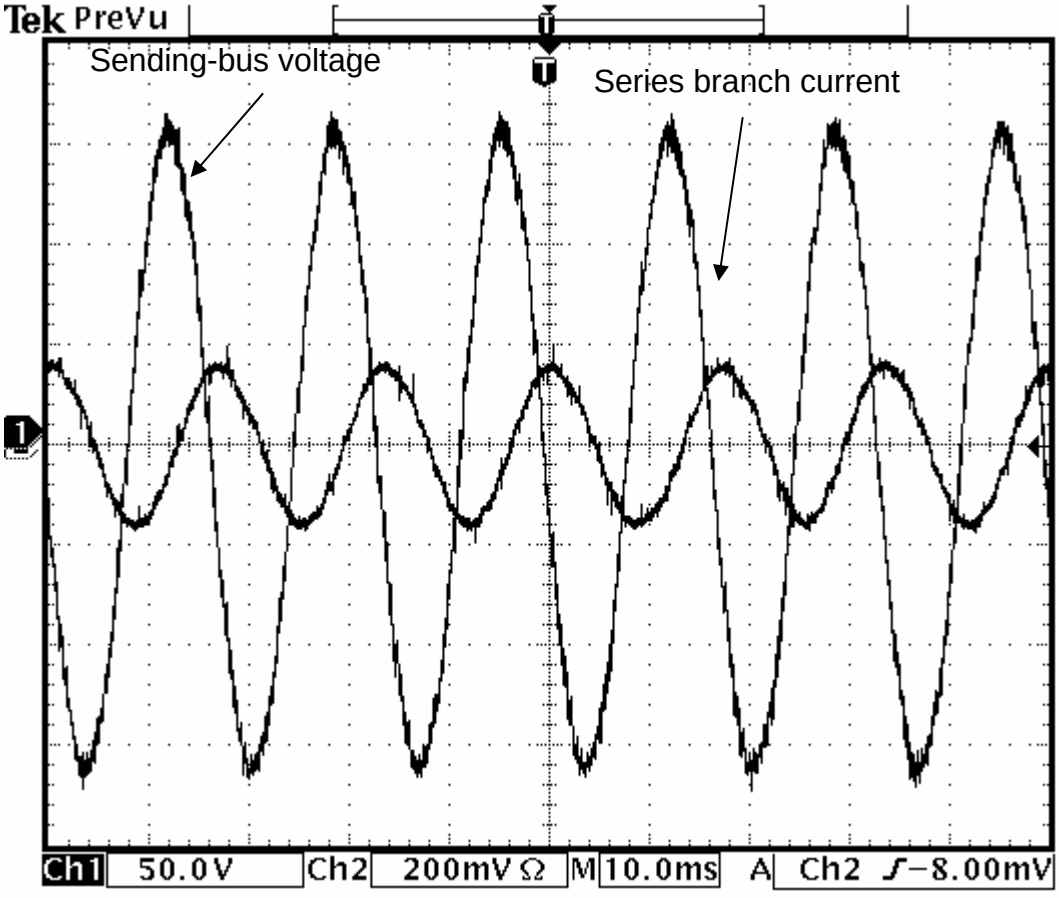


Figure 4.30 Sending bus voltage and series branch current with one UPFC unit

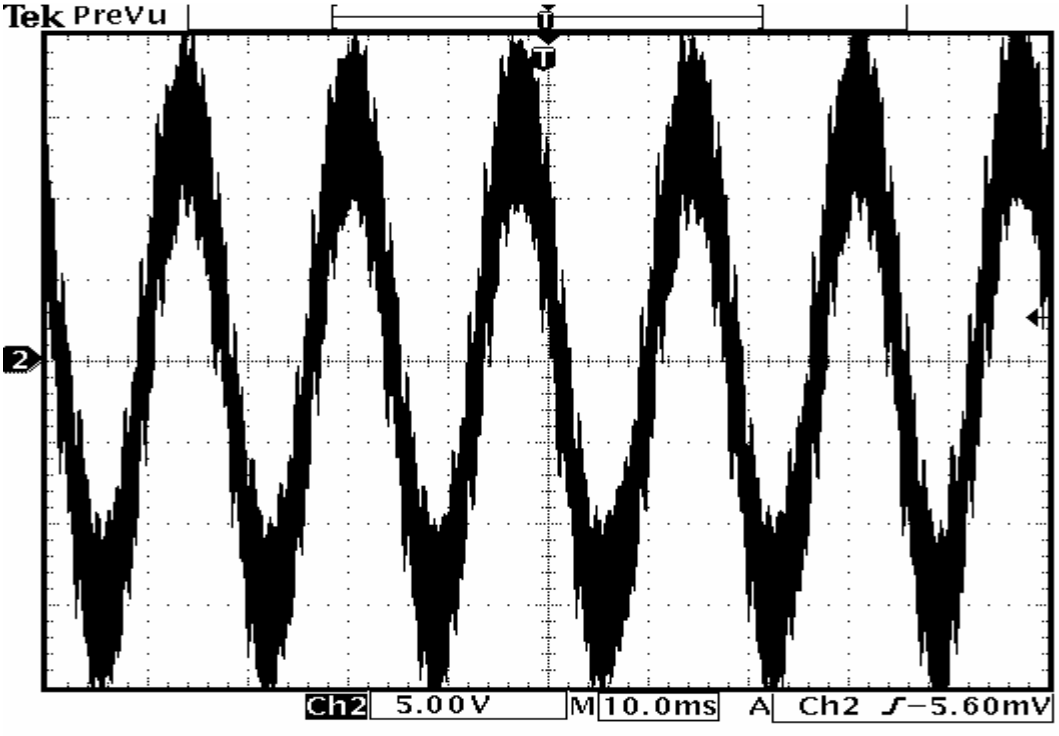


Figure 4.31 Injected series branch converter voltage

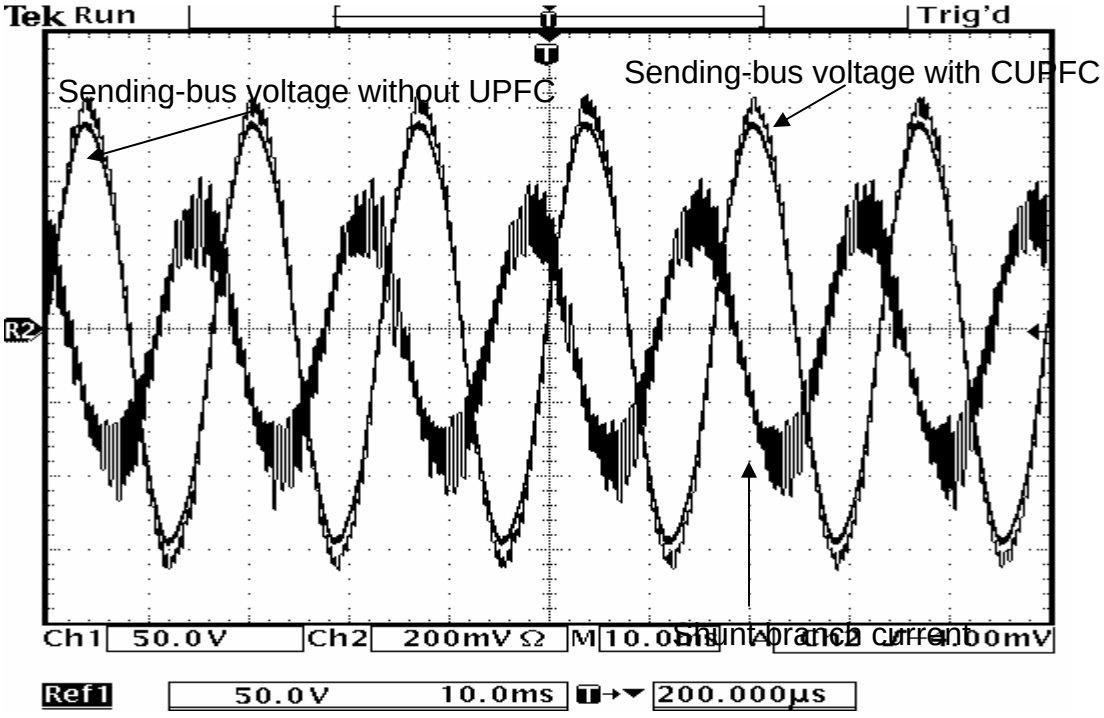


Figure 4.32 Sending-end bus voltage and shunt branch current with one UPFC unit

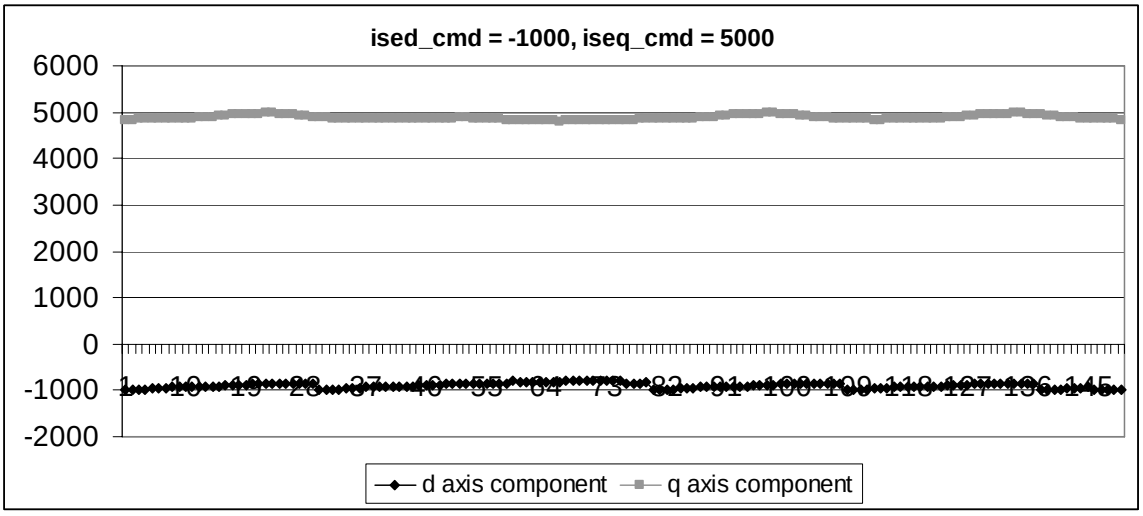


Figure 4.33 Measured d,q axis component of the series branch current with one unit operation

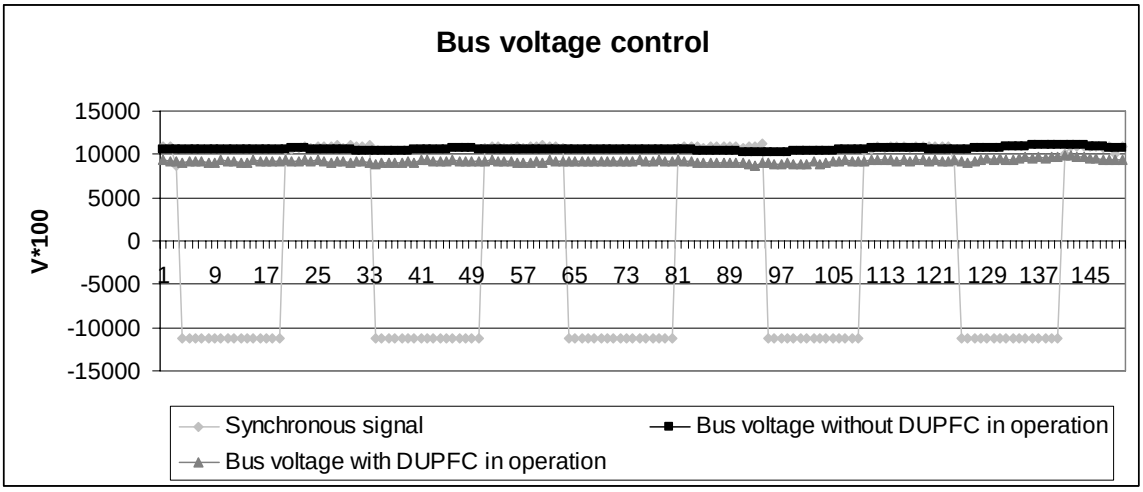


Figure 4.34 Sending-end bus voltage with and without the UPFC unit operation

The measured real and reactive components of the series branch current in Figure 4.33 verifies that the CUPFC realize its function by following the current commands in steady state operation. In Figure 4.34, the sending-end bus voltage magnitude is lower than 100 volts due to voltage drop on the internal inductance of the power supply. With the CUPFC operating, the sending-end bus voltage is controlled to 100 volts by reactive power compensation by the shunt device of the CUPFC.

(2) DUPFC case

In this case, two DUPFC units were put into operation with S1 switched on and S2 off. The power supply voltage was maintained to be 100 V. The series branch current command was kept to be I_{sed} = -1000, and I_{seq} = 5000 (same as in case 1). The sending-end bus voltage and the series branch current from simulation are shown in Figure 4.35. The corresponding signals from the experiment are depicted in Figure 4.36. The d-q axis components of the series branch current are illustrated in Figure 4.37. The two injected series branch voltages from the simulation and the experiment are shown in Figure 4.38 and Figure 4.39. The bus voltage and the first shunt branch current are depicted in Figure 4.40. The bus voltage with and without the UPFC, and the shunt branch 1 current in the experiment are illustrated in Figure 4.41. The sending-end bus voltage and the second shunt converter current from the simulation and the experiment are shown in Figure 4.42 and Figure 4.43. In the simulation, the switching circuit is not included. The switching harmonics are not presented in the snapshots.

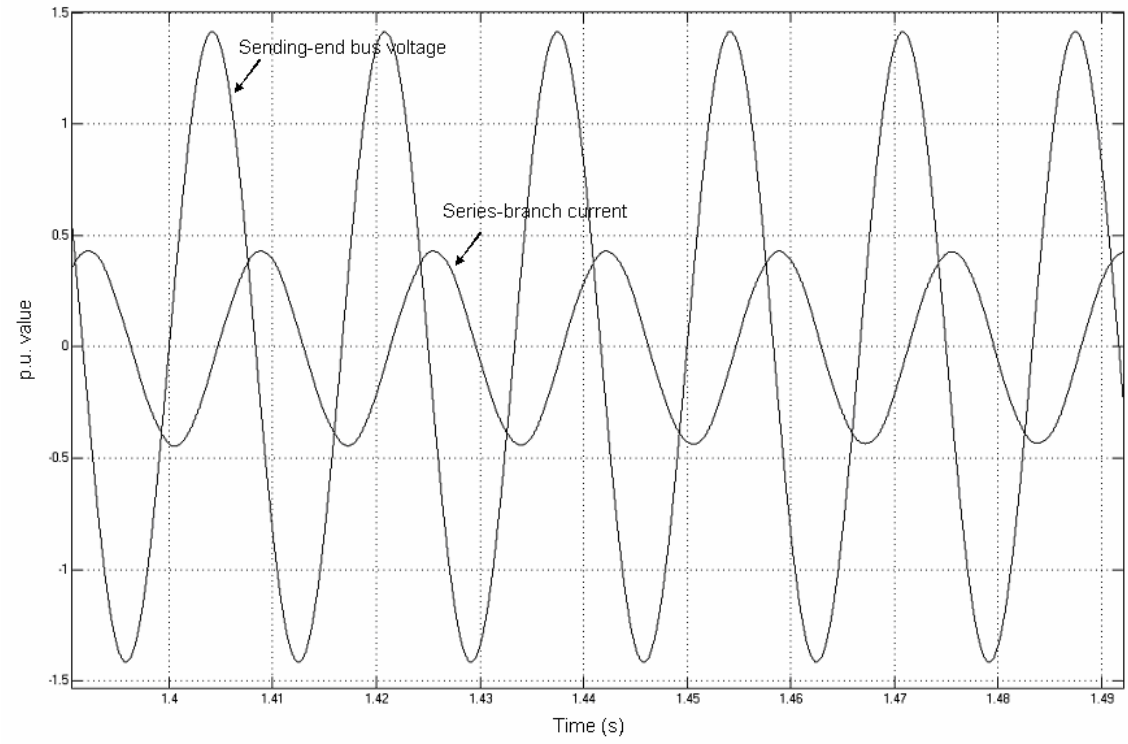


Figure 4.35 sending-end bus voltage and the series branch current from simulation

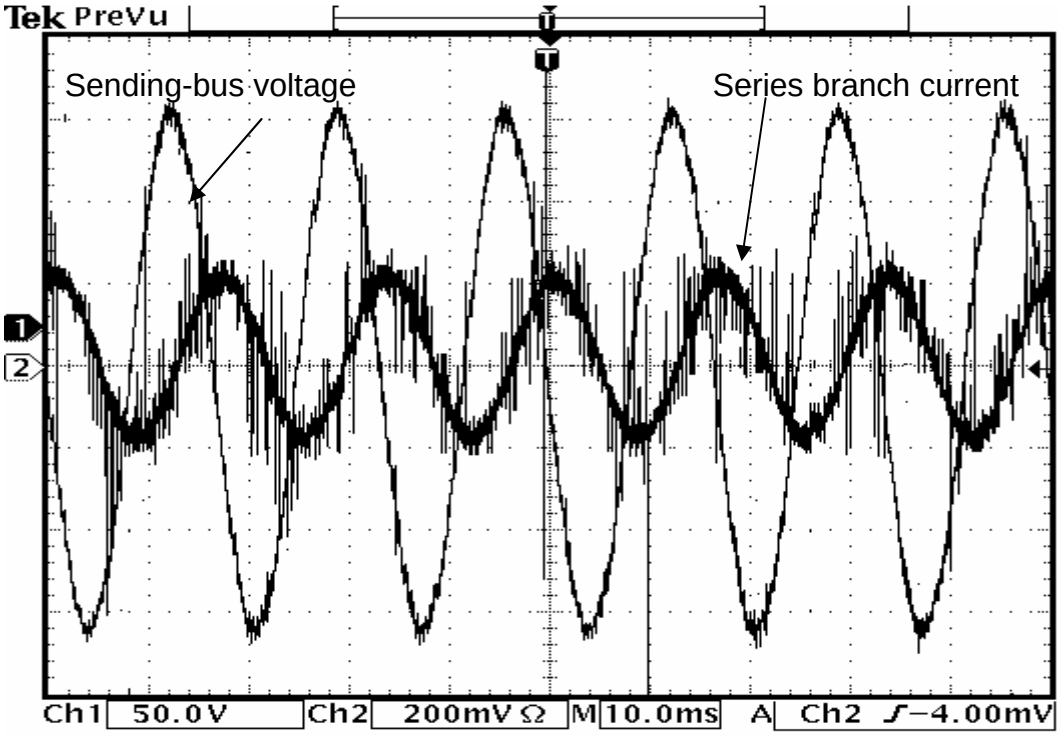


Figure 4.36 Sending-end bus voltage and the series branch current with two DUPFC units

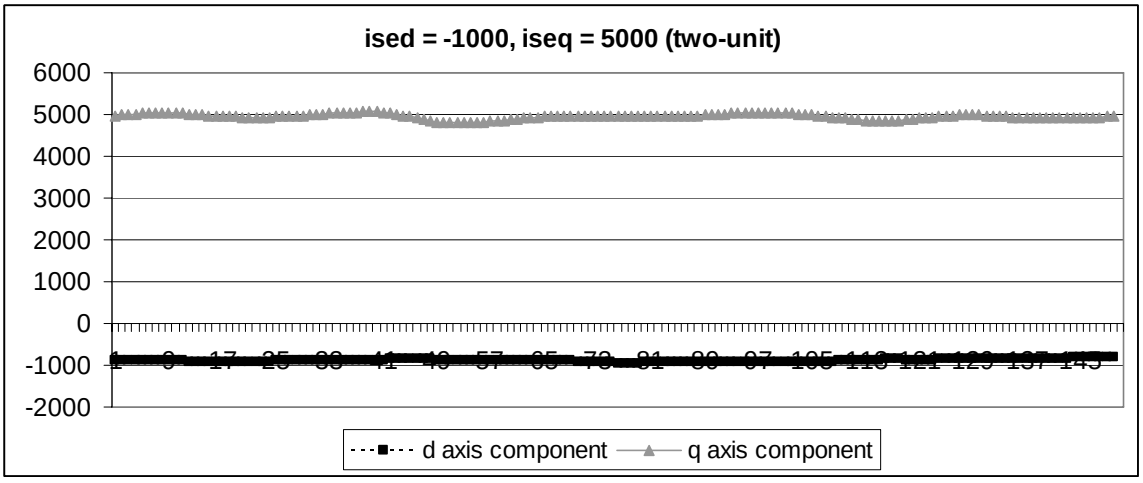


Figure 4.37 Measured d,q axis component of the series branch current with two unit operation

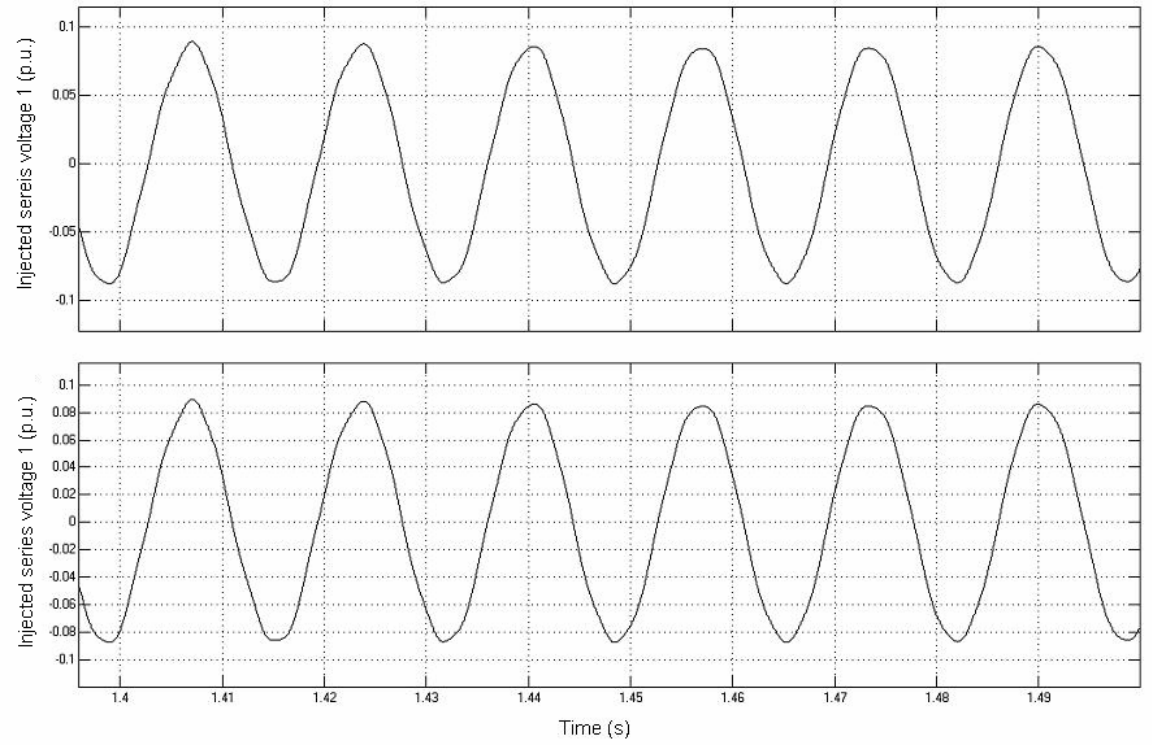


Figure 4.38 Injected series converter voltage from simulation

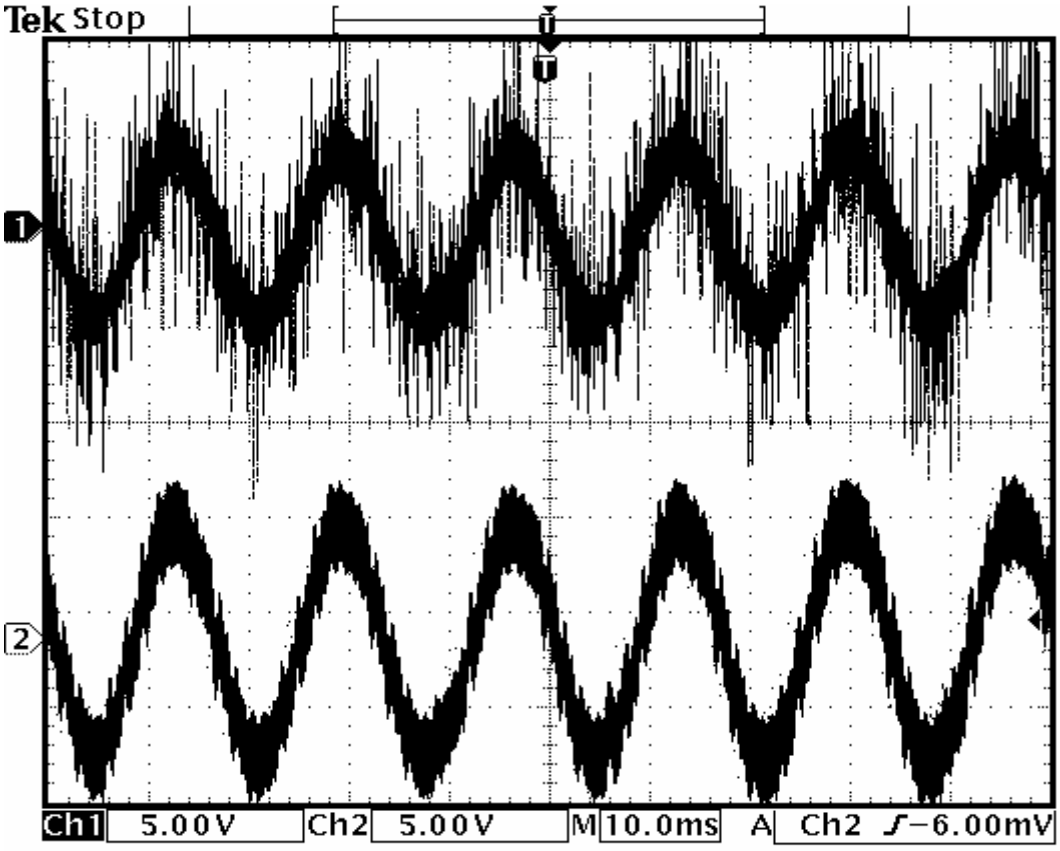


Figure 4.39 Injected series converter voltages

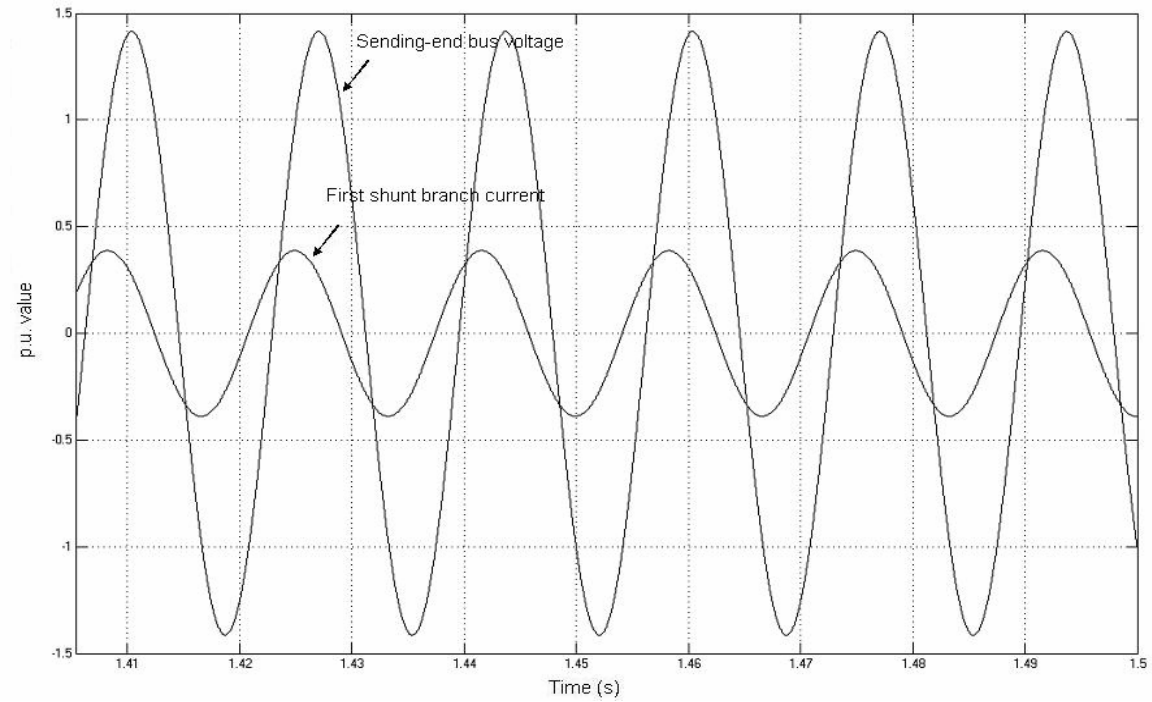


Figure 4.40 Sending-end bus voltage and the first shunt branch current from simulation

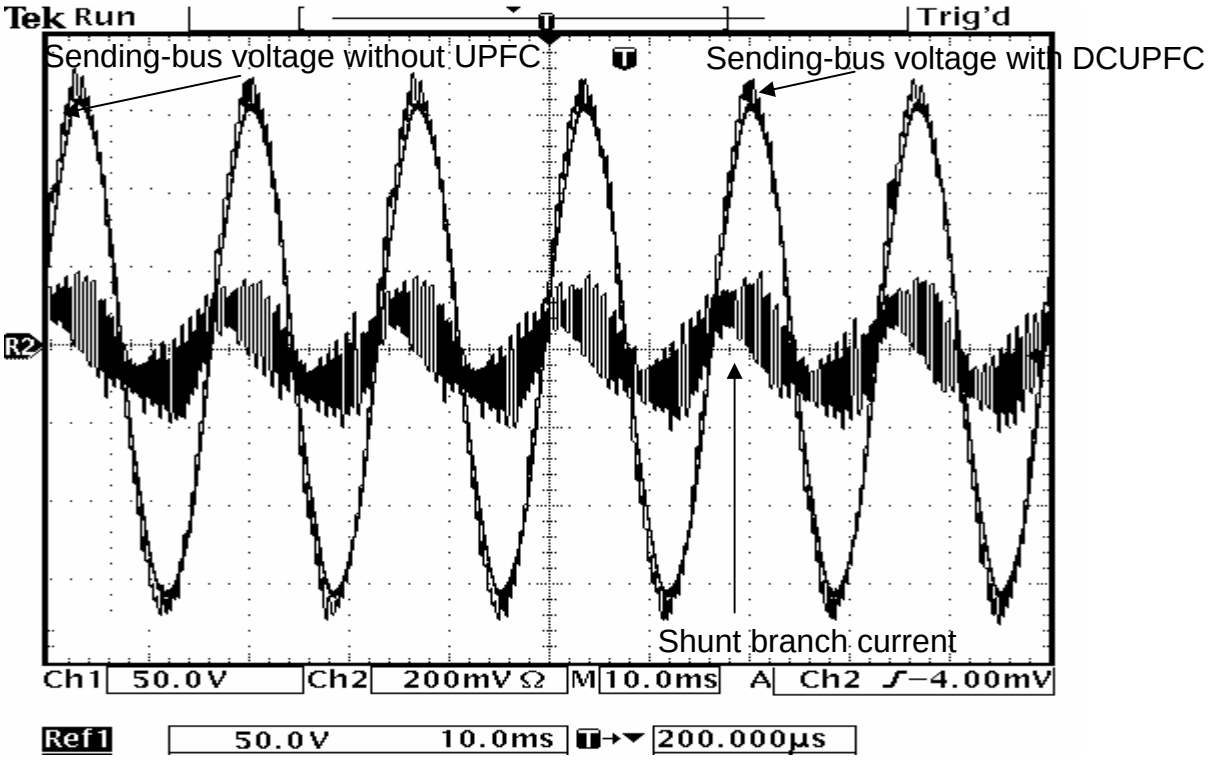


Figure 4.41 Sending-end bus voltage and the first shunt branch current with two UPFC units

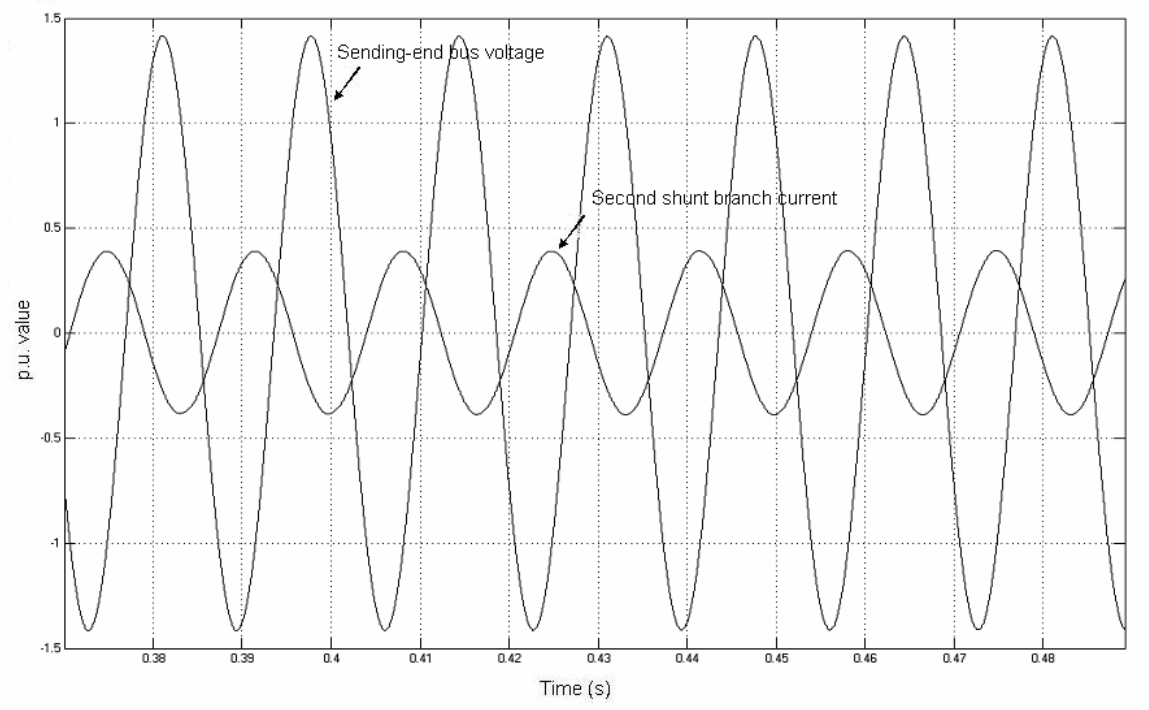


Figure 4.42 Sending-end bus voltage and the second shunt branch current from simulation

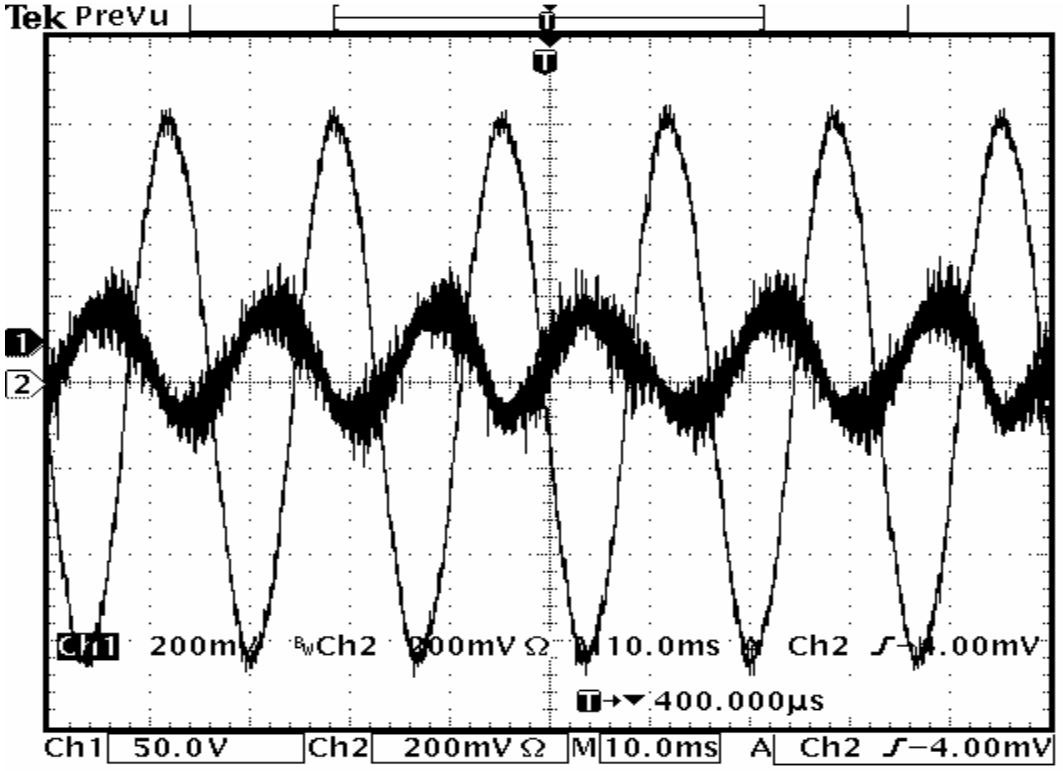


Figure 4.43 Sending-end bus voltage and the second shunt branch current with two UPFC units

The measured d and q components of the series branch current in Figure 4.37 follow the commands well. The measured data from the experiment matches the simulation results.

The simulation in chapter 3 and the experimental results in this chapter for both the CUPFC and DUPFC verify that both systems can realize the objective of the transmission line power flow control, and the bus voltage magnitude control. Thus, the DUPFC concept is proved to be feasible and functionally equivalent to the CUPFC. However, it is noticed that the two DUPFC units in the experiment affects with each other in operation. When setting the PI controller parameters, the PI control constants for the DUPFC cannot be set very large for the sake of stable operation. In the above mentioned two test cases, the PI controller for the CUPFC and DUPFC are list as in Table 4.2. The dynamic characteristic of the DUPFC system needs further study in future research.

Table 4.2 PI controller parameter for CUPFC and DUPFC

	CUPFC	DUPFC
AC voltage PI	ki_{v1} = 0x0010 kp_{v1} = 0x0800	ki_{v1} = 0x0008 kp_{v1} = 0x0800
DC voltage PI	ki_{DC} = 0x0010 kp_{DC} = 0x2000	ki_{DC1} = 0x0080 kp_{DC1} = 0x1000
		ki_{DC2} = 0x0068 kp_{DC2} = 0x1000
Shunt converter PI	kid_{sh} = 0x00E0 kpd_{sh} = 0x0010 kpq_{sh} = 0x1000	kid_{sh1} = 0x0080 kpd_{sh1} = 0x0010 kpq_{sh} = 0x1000
		kid_{sh2} = 0x0050 kpd_{sh2} = 0x0010 kpq_{sh} = 0x1000
Series converter PI	kid_{se} = 0x0020 kpd_{se} = 0x0200 kpq_{se} = 0x1000	kid_{se1} = 0x0010 kpd_{se1} = 0x0200 kpq_{se} = 0x1000

CHAPTER 5 CONTRIBUTION AND FUTURE RESEARCH

In this dissertation, a Distributed Unified Power Flow Controller (DUPFC) concept is proposed based on the conventional UPFC application. A control strategy is proposed, simulated, and implemented on a scaled test bed.

In a conventional Concentrated Unified Power Flow Controller (CUPFC) application, in which the total capacity is installed on a spot with bulky footprint, the series converter injected a voltage from power electronics based inverters with computed magnitude and phase angle according to control command (normally the transmission line real and/or reactive power) and the on-field signals. The shunt converter in a CUPFC is operated to maintain the bus voltage magnitude by providing or absorbing reactive power to the bus at the point where the CUPFC is installed. The potential flaws with the CUPFC includes: engineering reliability, economical cost, bulky footprint.

To address those problems inherent in the CUPFC, this dissertation comes up with a distributed UPFC concept. In the proposed DUPFC scheme, the function of the CUPFC is realized by more than one smaller-sized UPFC units. The injected voltage to control the power flow in the transmission line is produced, in a coordinated manner, by those series devices of the DUPFC. The shunt device in every DUPFC unit maintains the DC link voltage. By doing so, the real power, which is exchanged between the series devices and the voltage buses is provided or absorbed by the shunt devices. At the same time, the shunt devices realize the functionality of their counterpart in CUPFC application, which is to provide or absorb reactive power from the line. In this dissertation, the series injected voltage is obtained by producing voltages with equal magnitude and phase angle in all DUPFC units operating on the line. The provided or absorbed reactive power is shared among shunt devices of the DUPFC units equally. In such an arrangement, it is believed that the load is distributed equally among those distributed devices. This scheme has the following advantages:

(1) Every DUPFC unit provides part of the functionality of the CUPFC. In a failure scenario, only part, or even fraction if the number of the installed unit is large, of the capacity will be lost. Which increase the overall reliability of the whole system.

(2) The power rating of each unit is distributed equally. So that, the design of the DUPFC unit can be standardized. The manufacturing process can be automated on assembly lines to take advantage of the modernized manufacturing industry capability. In this way, the cost of the UPFC should be decreased dramatically. At the same time, the heat dissipation burden can be alleviated by distributing power load equally.

(3) Lower power rating decreases the size and weight of the DUPFC unit, which facilitate the installation of the devices. The footprint of the devices can be minimized or even eliminated. Equally distribution of power rating also standardizes the installation equipment and procedure.

The DUPFC is designed as a single-phase system, based on the practical application consideration. The full bridge AC/DC inverter is utilized to control the DC voltage and to produce the necessary AC voltages to allow power flow in both directions. For the purpose of effective control, the single phase signals are extended to three phase digitally. Instantaneous real and reactive powers are computed and separately controlled by using three-phase d-q transformation and closed loop PI controllers. Shunt devices of the DUPFC units are controlled to maintain both the proper DC link capacitor voltages and the bus voltage magnitude. The series devices of the DUPFC units are controlled to inject a voltage with proper magnitude and phase angle. Thus, the real and reactive power in the transmission line is controlled. The control algorithm is implemented on a fixed point Motorola DSP56F805 evaluation board.

The major purpose of this dissertation is to research the feasibility of the DUPFC concept. Some of the problems related to practical applications are omitted to make the topic solvable. These problems include insulation and

packaging problems related to high voltage, the re-conductoring of the existing transmission lines, the device protection, and some other issues. Those problems need to be investigated in future investigation.

In practical application, the two DUPFC units should have separated power circuit, and separated signal sampling and control system. In the experiment, the control algorithm of the two DUPFC units was implemented in one DSP, due to funds availability and time constraint. In this situation, isolation problem, especially ground problem is encountered and solved properly. In future research, the control of every DUPFC unit should be implemented in its own DSP. The higher hierarchy control and communication problem between devices need to be addressed.

The input board and the driving board in this project can be implemented into PCB board to assure secure connection between boards, and to reduce EMI noise in the circuit. This should be done in the future experiment.

The main focus of the dissertation is the steady-state operation of the DUPFC system. In future research, transient performance of the DUPFC system should be investigated.

The flexibility of the DUPFC needs to be further studied, especially the ability to maintain voltage profile in different buses along the transmission line. In this dissertation, only the sending-bus voltage control is implemented. If the command is to maintain the receiving end bus voltage, or even buses between sending-end and receiving-end bus, the ability of the DUPFC system to realize the control command needs to be addressed in the future.

APPENDICES

Appendix A. C code for the DSP

Only the C files programmed by the author are presented. The header files and the files generated by the code composer studio are not presented.

EventsVar.h

```
// This file defines the critical constants and public variables for control purpose
// alpha-beta coefficients
#define AL_BETA_CO_11 0x6883    // sqrt(2/3)
#define AL_BETA_CO_12 0xCBC1    // -(1/2)*sqrt(2/3)
#define AL_BETA_CO_13 0xCBC1    // -(1/2)*sqrt(2/3)
#define AL_BETA_CO_22 0x5A82    // 1/sqrt(2)
#define AL_BETA_CO_23 0xA57E    // -1/sqrt(2)
// alpha-beta coefficients

// inverse alpha-beta coefficients
#define INV_AL_BETA_CO_11 0x6883    // sqrt(2/3)
#define INV_AL_BETA_CO_21 0xCBC1    // -(1/2)*sqrt(2/3)
#define INV_AL_BETA_CO_22 0x5A82    // 1/sqrt(2)
// inverse alpha-beta coefficients

#define MAX_ARRAY_SIZE 150    // for test
#define BUFFER_SIZE 5          // for sampling delay to construct 3-phase
#define DEGREE_COMPENSATION 0    // delay compensation

#include "mathlib.h"

// ********************** PI control *************
#define kpd_se 0x0200       // Proportional coefficient
#define kid_se 0x0020       // Integrition coefficient
#define kpq_se 0x1000

#define kp_DC 0x1000 // DC voltage proportional constant
#define ki_DC 0x0080 // DC voltage integral constant

#define kp_DC2 0x2000 // DC voltage proportional constant
#define ki_DC2 0x0008 // DC voltage integral constant

#define ki_v1 0x0010    // AC voltage control proportional constant
#define Kp_v1 0x0800    // AC voltage control integral constant

#define kpd_sh 0x00E0    // ish proportional constant
#define kid_sh 0x0008    // ish integtegal constant
#define kpq_sh 0x1000
```

```
#define kpd_sh2 0x00E0    // ish proportional constant
#define kid_sh2 0x0010    // ish integtegal constant
#define kpq_sh2 0x1000

Frac16 ish1_d_command, ish1_q_command;
Frac16 ish2_d_command, ish2_q_command;
Frac16 vDC1_command, vDC2_command;
extern Frac16 pi_sh1_d, pi_sh1_q;
extern Frac16 pi_sh2_d, pi_sh2_q;//??????????
extern Frac16 pi_se_d, pi_se_q;
extern Frac16 pi_vDC1, pi_vDC2;
extern Frac16 pi_v1;
// ********************** PI control *************

// Modulation Index
int MI = 0x7fff; // 1
//int MI = 0x6000; // 3/4
//int MI = 0x4000; // 1/2
//int MI = 0x2000; // 1/4
//int MI = 0x1000; // 1/8
//int MI = 0x0800; // 1/16
int degree_sh = -10;
// for shunt converter degree control

//PI_params *PI_shunt_params_d, *PI_shunt_params_q;

// *************** PWM data
Frac16 duty_cycle_se, duty_cycle_sh1, duty_cycle_sh2;
// *************** PWM data

// ********************** filter coefficients **************
#define FIR_LENGTH 4
int mov_avg[FIR_LENGTH] =     // moving average filter
{
      0x2000, 0x2000, 0x2000, 0x2000 // 1/4
};
Frac16 vbus_d_tmp, vbus_q_tmp, ise_d_tmp, ise_q_tmp;
Frac16 vDC1_tmp, vDC2_tmp;
Frac16 ish1_d_tmp, ish1_q_tmp;
Frac16 ish2_d_tmp, ish2_q_tmp;
Frac16 ish1_A_tmp, ish2_A_tmp, ise_A_tmp;
int vbus_filter[FIR_LENGTH];
int ise_filter[FIR_LENGTH];
int ish1_filter[FIR_LENGTH];
Frac32 ish2_filter[FIR_LENGTH];
// ********************** filter coefficients **************

// ********************** inverse transform **************
Frac16 vse_alpha_command, vse_beta_command;
Frac16 vse_a_command;
Frac16 vse_d_command, vse_q_command;
Frac16 ise_d_command, ise_q_command;
Frac16 vsh1_d_command, vsh1_q_command;
Frac16 vsh1_alpha_command, vsh1_beta_command;
Frac16 vsh1_a_command;
```

```
Frac16 vsh2_d_command, vsh2_q_command;
Frac16 vsh2_alpha_command, vsh2_beta_command;
Frac16 vsh2_a_command;
Frac16 v1_command, ish_q_command;
// ********************** inverse transform **************

// ********************** vbus_dq filter data **************
#define FIR_DQ_LENGTH 6
int mov_dq_avg[FIR_DQ_LENGTH] =     // moving average filter
{
      0x1555, 0x1555, 0x1555,0x1555, 0x1555, 0x1555    /*1/6*/
};
//int vbus_d_filter[FIR_DQ_LENGTH];
//int vbus_q_filter[FIR_DQ_LENGTH];
int ise_d_filter[FIR_DQ_LENGTH];
int ise_q_filter[FIR_DQ_LENGTH];
int ish1_d_filter[FIR_DQ_LENGTH];
int ish1_q_filter[FIR_DQ_LENGTH];

int FIR_coeff[6] =     // FIR coefficients, Equiripple Lowpass 5th order filter
{                                  // Fpass = 60, Fs= 3600, Fstop = 300, Astop = 20dB,
      0x335d, /* 0.200646*2 */ 0x1134, /* 0.067211*2 */ 0x124a, /* 0.071442*2 */
      0x124a, /* 0.071442*2 */ 0x1134, /* 0.067211*2 */ 0x335d    /* 0.200646*2 */
};
// ********************** vbus_dq filter data **************

// ************************** used for 3-phase construction ***************
//int sh_A_delay_index;
Frac16 vbus_A_delay[BUFFER_SIZE];
Frac16 ise_A_delay[BUFFER_SIZE];
Frac16 ish1_A_delay[BUFFER_SIZE];
Frac16 ish2_A_delay[BUFFER_SIZE];
// ************************** used for 3-phase construction ***************

// ********************** bus degree detection ***************
int degree_vbus;
Frac16 vbus_zero_cross[2];
// ********************** bus degree detection ***************

// ******************** for test **************
int count_to_stop;
bool stop, debug;
Frac16 array_out_1[MAX_ARRAY_SIZE];
Frac16 array_out_2[MAX_ARRAY_SIZE];
Frac16 array_out_3[MAX_ARRAY_SIZE];
Frac16 array_out_4[MAX_ARRAY_SIZE];
// ******************** for test **************
```

Events

```
/** ###################################################################
**         Filename    : Events.C
**         Project     : Unified power flow controller
**         Processor : 56F805
**         Beantype    : Events
```

```
**         Version     : Driver 01.02
**         Compiler    : Metrowerks DSP C Compiler
**         Date/Time : 1/18/2006, 12:52 PM
**         Abstract    :
**              This module is used to control the series and shunt converter current.
/* Copy right 2006 Qiang Li, Dr. Jim Cathey
/* Power Equipment Research Lab, University of Kentucky
** ###################################################################*/
/* MODULE Events */

#include "Cpu.h"
#include "Events.h"
#include "Events_Var.h"
#include "mpy.h"

/*
** ===================================================================
**         Event           :   TimerLEDRed_Green_OnInterrupt (module Events)
**         Parameters    : None
**         Returns         : Nothing
** ===================================================================
*/
#pragma interrupt called
/* Comment this line if the appropriate 'Interrupt preserve registers' property */
/* is set to 'yes' (#pragma interrupt saveall is generated before the ISR)          */
void TimerLEDRed_Green_OnInterrupt(void)
{
      LEDGreen_Toggle();
}

/*
** ===================================================================
**         Event           :   TimerADCSync_OnInterrupt (module Events)
**         Description :
**         Parameters    : None
**         Returns         : Nothing
** ===================================================================
*/
#pragma interrupt saveall
/* Comment this line if the appropriate 'Interrupt preserve registers' property */
/* is set to 'yes' (#pragma interrupt saveall is generated before the ISR)          */
void TimerADCSync_OnInterrupt(void)
{
      Frac16 vbus_syn, vDC1, vDC2;

      Frac16 vbus_A, vbus_B, vbus_C;
      Frac16 sin_vbus, cos_vbus;
      Frac16 vbus_alpha, vbus_beta;
      Frac16 vbus_d, vbus_q;

      Frac16 ish1_A, ish1_B, ish1_C;
      Frac16 ish1_alpha, ish1_beta;
      Frac16 ish1_d, ish1_q;

      Frac16 ise_A, ise_B, ise_C;
      Frac16 ise_alpha, ise_beta;
```

```
	Frac16 ise_d, ise_q;

	Frac16 ish2_A, ish2_B, ish2_C;
	Frac16 ish2_alpha, ish2_beta;
	Frac16 ish2_d, ish2_q;

	Frac16 PI_error_sh1_d, PI_error_sh1_q;
	Frac16 PI_error_sh2_d, PI_error_sh2_q;
	Frac16 PI_error_se_d, PI_error_se_q;
	Frac16 PI_error_vDC1, PI_error_vDC2;
	Frac16 PI_error_V1;

	int k; // loop index
	Frac32 op_tmp;

	// ###########################################################################
	// *************** Voltage and current sampling0
	vbus_syn = PESL(ADC_A, ADC_READ_SAMPLE, 0);
	vbus_A = PESL(ADC_A, ADC_READ_SAMPLE, 5);
	ish1_A = PESL(ADC_A, ADC_READ_SAMPLE, 2);
	vDC1 = PESL(ADC_A, ADC_READ_SAMPLE, 3);
	ise_A = PESL(ADC_A, ADC_READ_SAMPLE, 1);
	ish2_A = PESL(ADC_A, ADC_READ_SAMPLE, 7);
	vDC2 = PESL(ADC_A, ADC_READ_SAMPLE, 6);
	// *************** Voltage and current sampling

	// ###########################################################################
	// *************** Synchronous voltage from ADCA0
	array_out_1[count_to_stop] = vbus_syn;    // shr_r(volt_syn,2); for test -------
	vbus_zero_cross[0] = vbus_zero_cross[1];
	vbus_zero_cross[1] = vbus_syn;
	if ((vbus_zero_cross[1] - vbus_zero_cross[0]) > 5000)
	{
		degree_vbus = DEGREE_COMPENSATION;
	}
	sin_vbus = math_sin(degree_vbus);    // degree compensation
	cos_vbus = math_cos(degree_vbus);    // degree compensation
	//array_out_2[count_to_stop] = sin_vbus;    // for test -----------
	//array_out_4[count_to_stop] = degree_vbus;    // for test -----------
	// *************** Synchronous voltage from ADCA0

	// ###########################################################################
	// statcom control open loop test
	//duty_cycle_sh = 0x0800 + mult_r(mult_r(0x0800,MI), sin_vbus);
	//array_out_3[count_to_stop]  =  math_sin(degree_vbus-degree_sh);  //duty_cycle_sh;  //  for
test
	//array_out_4[count_to_stop] = degree_vbus-degree_sh; //duty_cycle_sh; for test ------
	//

	// ###########################################################################
	// *************** Bus voltage    ********************
	// ******* Bus voltage filter.
	//array_out_2[count_to_stop] = vbus_A;         // for test ------
	vbus_filter[0] = vbus_filter[1];
	vbus_filter[1] = vbus_filter[2];
	vbus_filter[2] = vbus_filter[3];
```

```
vbus_filter[3] = vbus_A;

op_tmp = L_add(L_deposit_l(vbus_A),L_deposit_l(vbus_A));
op_tmp = L_add(op_tmp,mult_r(vbus_A,0x4000));
if(op_tmp > MAX_16)
	vbus_A = MAX_16;
else if(op_tmp < MIN_16)
	vbus_A =   MIN_16;
else
	vbus_A =   extract_l(op_tmp);
// ******* Construct 3 phases
vbus_C = -vbus_A_delay[0];
//array_out_2[count_to_stop] = vbus_C;   // for test ---------------
for (k=0;k<(BUFFER_SIZE-1);k++)
{
	vbus_A_delay[k] = vbus_A_delay[k+1];
}
vbus_A_delay[BUFFER_SIZE-1] = vbus_A;
vbus_B = -vbus_C - vbus_A;

array_out_2[count_to_stop] = vbus_A;   // for test ---------------
//array_out_3[count_to_stop] = vbus_B;   // for test ---------------
//array_out_4[count_to_stop] = vbus_C;   // for test ---------------
// ******* Construct 3 phases

// alpha-beta transform
vbus_alpha                                                                 =
mult_r(AL_BETA_CO_11,vbus_A)+mult_r(AL_BETA_CO_12,vbus_B)+mult_r(AL_BETA_CO_13,
vbus_C);
vbus_beta = mult_r(AL_BETA_CO_22,vbus_B)+mult_r(AL_BETA_CO_23,vbus_C);
//array_out_3[count_to_stop] = vbus_alpha;   // for test ---------------
//array_out_4[count_to_stop] = vbus_beta;   // for test ---------------
// alpha-beta transform

// vbus d-q transform
vbus_d = mult_r(vbus_alpha,sin_vbus) - mult_r(vbus_beta,cos_vbus);
vbus_q = -mult_r(vbus_alpha,cos_vbus) - mult_r(vbus_beta,sin_vbus);
//array_out_1[count_to_stop] = vbus_d;   // for test ---------------
//array_out_2[count_to_stop] = vbus_q;   // for test ---------------
vbus_d = mult_r(FRAC16(0.95),vbus_d_tmp)+mult_r(FRAC16(0.05),vbus_d);
vbus_d_tmp = vbus_d;
vbus_q = mult_r(FRAC16(0.95),vbus_q_tmp)+mult_r(FRAC16(0.05),vbus_q);
vbus_q_tmp = vbus_q;
//array_out_3[count_to_stop] = vbus_d;   // for test ---------------
//array_out_4[count_to_stop] = vbus_q;   // for test ---------------
//vbus d-q transform

// **********************************
// **********************************
// V1 voltage control - calculate shunt converter current command
op_tmp = L_sub(L_deposit_l(v1_command),L_deposit_l(vbus_d));
if(op_tmp > MAX_16)
	PI_error_v1 = MAX_16;
else if(op_tmp < MIN_16)
	PI_error_v1 =   MIN_16;
else
```

```
        PI_error_v1 =    extract_l(op_tmp);
// DC voltage error PI calculation
op_tmp = L_add(L_deposit_l(mult_r(PI_error_v1, ki_v1)), L_deposit_l(pi_v1));
if(op_tmp > 15000)
        pi_v1 = 15000;
else if(op_tmp < -15000)
        pi_v1 = -15000;
else
        pi_v1 = extract_l(op_tmp);
// shunt converter d-axis command to control DC voltage
op_tmp = L_add(L_deposit_l(pi_v1), L_deposit_l(mult_r(PI_error_v1,kp_v1)));
if(op_tmp > 23173)
        ish_q_command = 23173;
else if(op_tmp < -23173)
        ish_q_command =    -23173;
else
        ish_q_command =    extract_l(op_tmp);
ish1_q_command = multi_r(ish_q_command, FRAC16(0.5));
ish2_q_command = multi_r(ish_q_command, FRAC16(0.5));

// ###########################################################################
// *************** DC voltage 1 control
vDC1 = mult_r(FRAC16(0.95),vDC1_tmp) + mult_r(FRAC16(0.05),vDC1);
vDC1_tmp = vDC1;
vDC1 = vDC1 + 0x0100;    // calibration (Frac16 number = dc voltage * 100)
//array_out_4[count_to_stop] = vDC1;    // for test ----------------
//DC voltage error calculation
op_tmp = L_sub(L_deposit_l(vDC1_command),L_deposit_l(vDC1));
if(op_tmp > MAX_16)
        PI_error_vDC1 = MAX_16;
else if(op_tmp < MIN_16)
        PI_error_vDC1 =    MIN_16;
else
        PI_error_vDC1 =    extract_l(op_tmp);
// DC voltage error PI calculation
op_tmp = L_add(L_deposit_l(mult_r(PI_error_vDC1, ki_DC)), L_deposit_l(pi_vDC1));
if(op_tmp > 15000)
        pi_vDC1 = 15000;
else if(op_tmp < -15000)
        pi_vDC1 = -15000;
else
        pi_vDC1 = extract_l(op_tmp);
// shunt converter d-axis command to control DC voltage
op_tmp = L_add(L_deposit_l(pi_vDC1), L_deposit_l(mult_r(PI_error_vDC1,kp_DC)));
if(op_tmp > 23173)
        ish1_d_command = 23173;
else if(op_tmp < -23173)
        ish1_d_command =    -23173;
else
        ish1_d_command =    extract_l(op_tmp);
//ish_d_command = pi_VDC + kp_DC*(PI_error_vDC);
//array_out_2[count_to_stop] = PI_error_vDC1;    // for test ----------------
array_out_1[count_to_stop] = vDC1;    // for test ----------------
array_out_2[count_to_stop] = ish1_d_command;    // for test ----------------
// *************** DC voltage 1 control
```

```
	// ###########################################################################
	// ********** Shunt converter 1 current filter
	ish1_filter[0] = ish1_filter[1];
	ish1_filter[1] = ish1_filter[2];
	ish1_filter[2] = ish1_filter[3];
	ish1_filter[3] = ish1_A;
	ish1_A = fir(ish1_filter,mov_avg,FIR_LENGTH);
	// ********** Series current filter
	//array_out_2[count_to_stop] = ish1_A;    // for test ----------

	// ******* Construct 3 phases for i_sh
	ish1_C = -ish1_A_delay[0];
	for (k=0;k<(BUFFER_SIZE-1);k++)
	{
		ish1_A_delay[k] = ish1_A_delay[k+1];
	}
	ish1_A_delay[BUFFER_SIZE-1] = ish1_A;
	ish1_B = -ish1_C-ish1_A;
	//array_out_2[count_to_stop] = ish1_A;    // for test ----------
	//array_out_3[count_to_stop] = ish1_B;    // for test ----------
	//array_out_4[count_to_stop] = ish1_C;    // for test ----------
	// ******* Construct 3 phases for i_sh

	// alpha-beta transform
	ish1_alpha                                                                                                  =
mult_r(AL_BETA_CO_11,ish1_A)+mult_r(AL_BETA_CO_12,ish1_B)+mult_r(AL_BETA_CO_13,is
h1_C);
	ish1_beta = mult_r(AL_BETA_CO_22,ish1_B)+mult_r(AL_BETA_CO_23,ish1_C);
	// alpha-beta transform

	// d-q transform
	ish1_d = mult_r(ish1_alpha,sin_vbus) - mult_r(ish1_beta,cos_vbus);
	ish1_q = -mult_r(ish1_alpha,cos_vbus) - mult_r(ish1_beta,sin_vbus);
	ish1_d_filter[0] = ish1_d_filter[1];
	ish1_d_filter[1] = ish1_d_filter[2];
	ish1_d_filter[2] = ish1_d_filter[3];
	ish1_d_filter[3] = ish1_d_filter[4];
	ish1_d_filter[4] = ish1_d_filter[5];
	ish1_d_filter[5] = ish1_d;
	ish1_d=fir(ish1_d_filter,mov_dq_avg,FIR_DQ_LENGTH);
	ish1_d = mult_r(FRAC16(0.95),ish1_d_tmp)+mult_r(FRAC16(0.05),ish1_d);
	ish1_d_tmp = ish1_d;
	ish1_q_filter[0] = ish1_q_filter[1];
	ish1_q_filter[1] = ish1_q_filter[2];
	ish1_q_filter[2] = ish1_q_filter[3];
	ish1_q_filter[3] = ish1_q_filter[4];
	ish1_q_filter[4] = ish1_q_filter[5];
	ish1_q_filter[5] = ish1_q;
	ish1_q=fir(ish1_q_filter,FIR_coeff,FIR_DQ_LENGTH);
	ish1_q = mult_r(FRAC16(0.95),ish1_q_tmp)+mult_r(FRAC16(0.05),ish1_q);
	ish1_q_tmp = ish1_q;

	//array_out_2[count_to_stop] = ish1_q_command;    // for test -------
	array_out_3[count_to_stop] = ish1_d;    // for test ----------
	array_out_4[count_to_stop] = ish1_q;    // for test ----------
	// d-q transform
```

```
	// ************************************************
	// Shunt converter1 PI control
	// Calculate the PI error of d axis of ish
	op_tmp = L_sub(L_deposit_l(ish1_d_command),L_deposit_l(ish1_d));
	if(op_tmp > MAX_16)
		PI_error_sh1_d = MAX_16;
	else if(op_tmp < MIN_16)
		PI_error_sh1_d =    MIN_16;
	else
		PI_error_sh1_d =    extract_l(op_tmp);

	op_tmp = L_add(L_deposit_l(mult_r(PI_error_sh1_d, kid_sh)), L_deposit_l(pi_sh1_d));
	if(op_tmp > 20000)
		pi_sh1_d = 20000;
	else if(op_tmp < -20000)
		pi_sh1_d =    -20000;
	else
		pi_sh1_d = extract_l(op_tmp);
	// Calculate the PI error of q axis of ish
	op_tmp = L_sub(L_deposit_l(ish1_q_command),L_deposit_l(ish1_q));
	if(op_tmp > MAX_16)
		PI_error_sh1_q = MAX_16;
	else if(op_tmp < MIN_16)
		PI_error_sh1_q =    MIN_16;
	else
		PI_error_sh1_q =    extract_l(op_tmp);

	op_tmp = L_add(L_deposit_l(mult_r(PI_error_sh1_q, kid_sh)), L_deposit_l(pi_sh1_q));
	if(op_tmp > 20000)
		pi_sh1_q = 20000;
	else if(op_tmp < -20000)
		pi_sh1_q = -20000;
	else
		pi_sh1_q = extract_l(op_tmp);
	// Calculate d axis shunt voltage command
	//vsh_d_command = vbus_d - pi_sh_d - mult_r(kpd_sh,(ish_d_command - ish_d)) +
mult_r(kpq_sh, ish_q); // old
	//vsh_d_command = vbus_d - pi_sh_q - mult_r(kpd_sh,(ish_q_command - ish_q)); // +
mult_r(kpq_sh, ish_d);
	//op_tmp = L_add(L_deposit_l(vbus_d), L_deposit_l(-pi_sh_d));
	//op_tmp = L_add(op_tmp, L_deposit_l(mult_r(PI_error_sh_d,-kpd_sh)));
	//op_tmp = L_add(op_tmp, L_deposit_l(mult_r(ish_q,kpq_sh)));

	op_tmp = L_sub(L_deposit_l(vbus_d), L_deposit_l(pi_sh1_q));
	op_tmp = L_sub(op_tmp, L_deposit_l(mult_r(PI_error_sh1_q,kpd_sh)));
	op_tmp = L_add(op_tmp, L_deposit_l(mult_r(ish1_d,kpq_sh)));
	if(op_tmp > 23173)
		vsh1_d_command = 23173;
	else if(op_tmp < -23173)
		vsh1_d_command =    -23173;
	else
		vsh1_d_command =    extract_l(op_tmp);
	//vsh_d_command = vbus_d + pi_sh_d + mult_r(kpd_sh,PI_error_sh_d) - mult_r(kpq_sh,
ish_q);
```

```
	//array_out_1[count_to_stop] = pi_sh_q;    // for test ----------
	//array_out_2[count_to_stop] = ish_q; //pi_sh_d;    // for test ----------
	//array_out_3[count_to_stop] = vbus_d;    // for test ----------
	//array_out_3[count_to_stop] = mult_r(ish_d,kpq_sh);    // for test ----------
	//array_out_4[count_to_stop] = vsh_d_command;    // for test ----------

	// Calculate q axis shunt voltage command
	//vsh_q_command = -pi_sh_q - mult_r(kpd_sh,(ish_q_command - ish_q)) - mult_r(kpq_sh,
ish_d); // old
	//vsh_q_command = -pi_sh_q - mult_r(kpd_sh,(ish_q_command - ish_q)); // - mult_r(kpq_sh,
ish_d);
	op_tmp = L_add(L_deposit_l(pi_sh1_d), L_deposit_l(mult_r(PI_error_sh1_d,kpd_sh)));
	op_tmp = L_shl(op_tmp,3);
	op_tmp = L_add(op_tmp, L_deposit_l(mult_r(ish1_q,-kpq_sh)));
	if(op_tmp > 23173)
		vsh1_q_command = 23173;
	else if(op_tmp < -23173)
		vsh1_q_command =    -23173;
	else
		vsh1_q_command =    extract_l(op_tmp);

	//array_out_1[count_to_stop] = pi_sh1_d;    // for test ----------
	//array_out_2[count_to_stop] = mult_r(PI_error_sh1_d,kpd_sh);    // for test ----------
	//array_out_3[count_to_stop] = mult_r(ish1_q,kpq_sh);    // for test ----------
	//array_out_4[count_to_stop] = vsh1_q_command;    // for test ----------
	// Shunt PI control
	// ************************************************
	//vsh1_d_command = 14500;
	//vsh1_q_command = -14500;

	// degree compensation
	sin_vbus = math_sin(degree_vbus+0);
	cos_vbus = math_cos(degree_vbus+0);

	// ************************************************
	// Inverse d-q transform
	vsh1_alpha_command              =              mult_r(vsh1_d_command,sin_vbus)              -
mult_r(vsh1_q_command,cos_vbus);
	//array_out_3[count_to_stop] = vsh1_alpha_command;    // for test ----------

	// ************************************************
	// Inverse alpha-beta transform
	vsh1_a_command = mult_r(INV_AL_BETA_CO_11,vsh1_alpha_command);
	//array_out_4[count_to_stop] = vsh1_a_command;    // for test ----------

	// ********** duty cycle update ***********
	duty_cycle_sh1 = 0x0800 + mult_r(0x0800,vsh1_a_command);
	//duty_cycle_sh1 = 0x0800 + mult_r(0x0780,sin_vbus);
	if (duty_cycle_sh1 > 0x1000) duty_cycle_sh1 = 0x0e1f;
	if (duty_cycle_sh1 < 0) duty_cycle_sh1 = 0x01e0;
	// ********************** ish control
	// ************************************************
	//array_out_3[count_to_stop] = sin_vbus;    // for test ----------
	//array_out_4[count_to_stop] = vsh1_a_command;    // for test ----------

	// ##########################################################################
```

```
// *************** DC voltage 2 control
//if (vDC2 = 0)
//      vDC2 = vDC2_tmp;
//if (vDC2 > 200000)
//      vDC2 = vDC2_tmp;
//array_out_1[count_to_stop] = vDC2;    // for test ----------
op_tmp = L_add(L_deposit_l(vDC2),0); // , L_deposit_l(mult_r(vDC2,0x0360)));
if (op_tmp > MAX_16)
      vDC2 = MAX_16;
else
      vDC2 = extract_l(op_tmp);
vDC2 = mult_r(FRAC16(0.95),vDC2_tmp) + mult_r(FRAC16(0.05),vDC2);
vDC2_tmp = vDC2;
// DC voltage error calculation
op_tmp = L_sub(L_deposit_l(vDC2_command),L_deposit_l(vDC2));
if(op_tmp > MAX_16)
      PI_error_vDC2 = MAX_16;
else if(op_tmp < MIN_16)
      PI_error_vDC2 =    MIN_16;
else
      PI_error_vDC2 =    extract_l(op_tmp);
// DC voltage error PI calculation
op_tmp = L_add(L_deposit_l(mult_r(PI_error_vDC2, ki_DC2)), L_deposit_l(pi_vDC2));
if(op_tmp > 15000)
      pi_vDC2 = 15000;
else if(op_tmp < -15000)
      pi_vDC2 = -15000;
else
      pi_vDC2 = extract_l(op_tmp);
// shunt converter d-axis command to control DC voltage
op_tmp = L_add(L_deposit_l(pi_vDC2), L_deposit_l(mult_r(PI_error_vDC2,kp_DC2)));
if(op_tmp > 23173)
      ish2_d_command = 23173;
else if(op_tmp < -23173)
      ish2_d_command =    -23173;
else
      ish2_d_command =    extract_l(op_tmp);
//ish_d_command = pi_VDC + kp_DC*(PI_error_vDC);
//array_out_4[count_to_stop] = vDC2;    // for test ----------
//array_out_2[count_to_stop] = ish2_d_command;    // for test ----------
//array_out_4[count_to_stop] = ish2_d_command;    // for test ----------
// *************** DC voltage 2 control

// ##########################################################################
// *************** Shunt converter 2 current filter
ish2_filter[0] = ish2_filter[1];
ish2_filter[1] = ish2_filter[2];
ish2_filter[2] = ish2_filter[3];
ish2_filter[3] = L_deposit_l(ish2_A);

op_tmp = L_add(ish2_filter[3],ish2_filter[2]);
op_tmp = L_add(op_tmp,ish2_filter[1]);
op_tmp = L_add(op_tmp,ish2_filter[0]);
ish2_A = extract_l(L_mult_ls(op_tmp, FRAC16(0.25)));
//array_out_3[count_to_stop] = ish2_A;    // for test ----------
// *************** Shunt converter 2 current filter
```

```
	// ******* Construct 3 phases for i_sh
	ish2_C = -ish2_A_delay[0];
	for (k=0;k<(BUFFER_SIZE-1);k++)
	{
		ish2_A_delay[k] = ish2_A_delay[k+1];
	}
	ish2_A_delay[BUFFER_SIZE-1] = ish2_A;
	ish2_B = -ish2_C-ish2_A;

	//array_out_2[count_to_stop] = ish2_A;	// for test ----------
	//array_out_3[count_to_stop] = ish2_B;	// for test ----------
	//array_out_4[count_to_stop] = ish2_C;	// for test ----------
	// ******* Construct 3 phases for i_sh

	// alpha-beta transform
	ish2_alpha                                                                                                  =
mult_r(AL_BETA_CO_11,ish2_A)+mult_r(AL_BETA_CO_12,ish2_B)+mult_r(AL_BETA_CO_13,is
h2_C);
	ish2_beta = mult_r(AL_BETA_CO_22,ish2_B)+mult_r(AL_BETA_CO_23,ish2_C);
	// alpha-beta transform

	// degree compensation
	//sin_vbus = math_sin(degree_vbus-0);
	//cos_vbus = math_cos(degree_vbus-0);

	// d-q transform
	ish2_d = mult_r(ish2_alpha,sin_vbus) - mult_r(ish2_beta,cos_vbus);
	ish2_q = -mult_r(ish2_alpha,cos_vbus) - mult_r(ish2_beta,sin_vbus);
	ish2_d = mult_r(FRAC16(0.95),ish2_d_tmp)+mult_r(FRAC16(0.05),ish2_d);
	ish2_d_tmp = ish2_d;
	ish2_q = mult_r(FRAC16(0.95),ish2_q_tmp)+mult_r(FRAC16(0.05),ish2_q);
	ish2_q_tmp = ish2_q;

	//array_out_2[count_to_stop] = ish2_q_command;	// for test -------
	//array_out_3[count_to_stop] = ish2_d;	// for test ----------
	//array_out_4[count_to_stop] = ish2_q;	// for test ----------
	// d-q transform

	// ************************************************
	// Shunt converter2 PI control
	// Calculate the PI error of d axis of ish
	op_tmp = L_sub(L_deposit_l(ish2_d_command),L_deposit_l(ish2_d));
	if(op_tmp > MAX_16)
		PI_error_sh2_d = MAX_16;
	else if(op_tmp < MIN_16)
		PI_error_sh2_d =    MIN_16;
	else
		PI_error_sh2_d =    extract_l(op_tmp);

	op_tmp = L_add(L_deposit_l(mult_r(PI_error_sh2_d, kid_sh2)), L_deposit_l(pi_sh2_d));
	if(op_tmp > 20000)
		pi_sh2_d = 20000;
	else if(op_tmp < -20000)
		pi_sh2_d =    -20000;
	else
```

```
        pi_sh2_d = extract_l(op_tmp);
    // Calculate the PI error of q axis of ish
    op_tmp = L_sub(L_deposit_l(ish2_q_command),L_deposit_l(ish2_q));
    if(op_tmp > MAX_16)
        PI_error_sh2_q = MAX_16;
    else if(op_tmp < MIN_16)
        PI_error_sh2_q =    MIN_16;
    else
        PI_error_sh2_q =    extract_l(op_tmp);

    op_tmp = L_add(L_deposit_l(mult_r(PI_error_sh2_q, kid_sh2)), L_deposit_l(pi_sh2_q));
    if(op_tmp > 20000)
        pi_sh2_q = 20000;
    else if(op_tmp < -20000)
        pi_sh2_q = -20000;
    else
        pi_sh2_q = extract_l(op_tmp);

    // Calculate d axis shunt voltage command
    //vsh2_d_command = vbus_d - pi_sh2_q - mult_r(kpd_sh,PI_error_sh2_q) + mult_r(kpq_sh,
ish2_d);
    //op_tmp = L_add(L_deposit_l(vbus_d), L_deposit_l(pi_sh2_d));
    //op_tmp = L_add(op_tmp, L_deposit_l(mult_r(PI_error_sh2_d,kpd_sh2)));
    //op_tmp = L_add(op_tmp, L_deposit_l(mult_r(ish2_q,kpq_sh2)));

    op_tmp = L_sub(L_deposit_l(vbus_d), L_deposit_l(pi_sh2_q));
    op_tmp = L_sub(op_tmp, L_deposit_l(mult_r(PI_error_sh2_q,kpd_sh2)));
    op_tmp = L_add(op_tmp, L_deposit_l(mult_r(ish2_d,kpq_sh2)));
    if(op_tmp > 23173)
        vsh2_d_command = 23173;
    else if(op_tmp < -23173)
        vsh2_d_command =    -23173;
    else
        vsh2_d_command =    extract_l(op_tmp);

    //array_out_1[count_to_stop] = ish2_q; //pi_sh_d;    // for test ----------
    //array_out_2[count_to_stop] = PI_error_sh2_q;    // for text    ----------
    //array_out_3[count_to_stop] = pi_sh2_q;    // for test ----------
    //array_out_3[count_to_stop] = vbus_d;    // for test ----------
    //array_out_3[count_to_stop] = mult_r(ish2_d,kpq_sh);    // for test ----------
    //array_out_4[count_to_stop] = vsh2_d_command;    // for test ----------

    // Calculate q axis shunt voltage command
   //vsh_q_command = -pi_sh2_q - mult_r(kpd_sh,(ish2_q_command - ish2_q)) - mult_r(kpq_sh,
ish2_d); // old
    //vsh_q_command = pi_sh2_d + mult_r(kpd_sh,PI_error_sh2_d) - mult_r(kpq_sh, ish2_q);
    //op_tmp = L_add(L_deposit_l(-pi_sh2_d), L_deposit_l(mult_r(PI_error_sh2_d,-kpd_sh2)));
    //op_tmp = L_shl(op_tmp,3);
    //op_tmp = L_add(op_tmp, L_deposit_l(mult_r(ish2_q,-kpq_sh2)));

    op_tmp = L_add(L_deposit_l(pi_sh2_d), L_deposit_l(mult_r(PI_error_sh2_d,kpd_sh2)));
    op_tmp = L_shl(op_tmp,3);
    op_tmp = L_add(op_tmp, L_deposit_l(mult_r(ish2_q,-kpq_sh2)));
    if(op_tmp > 23173)
        vsh2_q_command = 23173;
    else if(op_tmp < -23173)
```

```
        vsh2_q_command =    -23173;
    else
        vsh2_q_command =    extract_l(op_tmp);

    //array_out_1[count_to_stop] = vDC2;    // for test ----------
    //array_out_1[count_to_stop] = ish2_d_command;    // for test ----------
    //array_out_1[count_to_stop] = pi_sh2_d;    // for test ----------
    //array_out_2[count_to_stop] = mult_r(PI_error_sh2_d,kpd_sh);    // for test ----------
    //array_out_3[count_to_stop] = mult_r(ish2_q,kpq_sh);    // for test ----------
    //array_out_4[count_to_stop] = vsh2_q_command;    // for test ----------
    // Shunt PI control
    // ************************************************

    sin_vbus = math_sin(degree_vbus + 0);    // degree compensation
    cos_vbus = math_cos(degree_vbus + 0);    // degree compensation

    // ************************************************
    // Inverse d-q transform
    vsh2_alpha_command              =              mult_r(vsh2_d_command,sin_vbus)              -
mult_r(vsh2_q_command,cos_vbus);
    //array_out_3[count_to_stop] = vsh_alpha_command;    // for test ----------

    // ************************************************
    // Inverse alpha-beta transform
    vsh2_a_command = mult_r(INV_AL_BETA_CO_11,vsh2_alpha_command);

    // ********** duty cycle update ************
    duty_cycle_sh2 = 0x0800 + mult_r(0x0800,vsh2_a_command);
    //duty_cycle_sh2 = 0x0800 + mult_r(0x0780,sin_vbus);
    if (duty_cycle_sh2 > 0x1000) duty_cycle_sh2 = 0x0e1f;
    if (duty_cycle_sh2 < 0) duty_cycle_sh2 = 0x01e0;
    // ********************** ish control
    // ************************************************
    //array_out_4[count_to_stop] = duty_cycle_sh2;    // for test ----------

    // ##########################################################################
    // *************** Series current filter
    ise_filter[0] = ise_filter[1];
    ise_filter[1] = ise_filter[2];
    ise_filter[2] = ise_filter[3];
    ise_filter[3] = ise_A;
    ise_A = fir(ise_filter,mov_avg,FIR_LENGTH);
    // *************** Series current filter

    ise_C = negate(ise_A_delay[0]);
    for (k=0;k<(BUFFER_SIZE-1);k++)
    {
        ise_A_delay[k] = ise_A_delay[k+1];
    }
    ise_A_delay[BUFFER_SIZE-1] = ise_A;
    ise_B = -ise_C-ise_A;
    //array_out_2[count_to_stop] = ise_A;    // for test ----------
    //array_out_3[count_to_stop] = ise_B;    // for test ----------
    //array_out_4[count_to_stop] = ise_C;    // for test ----------
    // ******* Construct 3 phases for i_sh
```

```
// alpha-beta transform
ise_alpha = mult_r(AL_BETA_CO_11,ise_A)+mult_r(AL_BETA_CO_12,ise_B)+mult_r(AL_BETA_CO_13,ise_C);
ise_beta = mult_r(AL_BETA_CO_22,ise_B)+mult_r(AL_BETA_CO_23,ise_C);
//array_out_3[count_to_stop] = ise_alpha;   // for test ---------------
//array_out_4[count_to_stop] = ise_beta;   // for test ---------------
// alpha-beta transform

// d-q transform
ise_d = mult_r(ise_alpha,sin_vbus) - mult_r(ise_beta,cos_vbus);
ise_q = -mult_r(ise_alpha,cos_vbus) - mult_r(ise_beta,sin_vbus);
ise_d_filter[0] = ise_d_filter[1];
ise_d_filter[1] = ise_d_filter[2];
ise_d_filter[2] = ise_d_filter[3];
ise_d_filter[3] = ise_d_filter[4];
ise_d_filter[4] = ise_d_filter[5];
ise_d_filter[5] = ise_d;
ise_d=fir(ise_d_filter,mov_dq_avg,FIR_DQ_LENGTH);
ise_d = mult_r(FRAC16(0.95),ise_d_tmp)+mult_r(FRAC16(0.05),ise_d);
ise_d_tmp = ise_d;
ise_q_filter[0] = ise_q_filter[1];
ise_q_filter[1] = ise_q_filter[2];
ise_q_filter[2] = ise_q_filter[3];
ise_q_filter[3] = ise_q_filter[4];
ise_q_filter[4] = ise_q_filter[5];
ise_q_filter[5] = ise_q;
ise_q=fir(ise_q_filter,FIR_coeff,FIR_DQ_LENGTH);
ise_q = mult_r(FRAC16(0.95),ise_q_tmp)+mult_r(FRAC16(0.05),ise_q);
ise_q_tmp = ise_q;
//array_out_3[count_to_stop] = ise_d;   // for test ---------------
//array_out_4[count_to_stop] = ise_q;   // for test ---------------
// d-q transform

// Series real and reactive current control
op_tmp = L_sub(L_deposit_l(ise_d_command),L_deposit_l(ise_d));
if(op_tmp > MAX_16)
    PI_error_se_d = MAX_16;
else if(op_tmp < MIN_16)
    PI_error_se_d =   MIN_16;
else
    PI_error_se_d =   extract_l(op_tmp);

op_tmp = L_add(L_deposit_l(mult_r(PI_error_se_d, kid_se)), L_deposit_l(pi_se_d));
if(op_tmp > 20000)
    pi_se_d = 20000;
else if(op_tmp < -20000)
    pi_se_d =   -20000;
else
    pi_se_d = extract_l(op_tmp);

//vse_d_command = mult_r(kpd_se,(ise_d_command - ise_d)) - mult_r(kpq_se,ise_q);
op_tmp = L_add(L_deposit_l(pi_se_d), L_deposit_l(mult_r(PI_error_se_d,kpd_se)));
//op_tmp = L_sub(op_tmp, L_deposit_l(mult_r(ise_q,kpq_se)));
if(op_tmp > 23173)
    vse_d_command = 23173;
```

```
    else if(op_tmp < -23173)
        vse_d_command =    -23173;
    else
        vse_d_command =    extract_l(op_tmp);
    //array_out_1[count_to_stop] = pi_se_d;    // for test ----------
    //array_out_2[count_to_stop] = mult_r(PI_error_se_d, kpd_se);    // for test ----------
    //array_out_3[count_to_stop] = vse_d_command;    // for test ----------
    //array_out_4[count_to_stop] = ise_d; // for test ----------

    //vse_q_command = mult_r(kpq_se,(ise_d_command - ise_d)) + mult_r(kpd_se,ise_q);
    op_tmp = L_sub(L_deposit_l(ise_q_command),L_deposit_l(ise_q));
    if(op_tmp > MAX_16)
        PI_error_se_q = MAX_16;
    else if(op_tmp < MIN_16)
        PI_error_se_q =    MIN_16;
    else
        PI_error_se_q =    extract_l(op_tmp);

    op_tmp = L_add(L_deposit_l(mult_r(PI_error_se_q, kid_se)), L_deposit_l(pi_se_q));
    if(op_tmp > 20000)
        pi_se_q = 20000;
    else if(op_tmp < -20000)
        pi_se_q = -20000;
    else
        pi_se_q = extract_l(op_tmp);
    //array_out_1[count_to_stop] = pi_se_q;    // for test ----------

    //vse_q_command = mult_r(kpd_se,(ise_q_command - ise_q)) + mult_r(kpq_se,ise_d);
    op_tmp = L_add(L_deposit_l(pi_se_q), L_deposit_l(mult_r(PI_error_se_q,kpd_se)));
    //op_tmp = L_add(op_tmp, L_deposit_l(mult_r(ise_d,kpq_se)));
    if(op_tmp > 23173)
        vse_q_command = 23173;
    else if(op_tmp < -23173)
        vse_q_command =    -23173;
    else
        vse_q_command =    extract_l(op_tmp);
    //array_out_1[count_to_stop] = pi_se_q;    // for test ----------
    //array_out_2[count_to_stop] = mult_r(PI_error_se_q, kpd_se);    // for test ----------
    //array_out_3[count_to_stop] = ise_d;    // for test ----------
    //array_out_4[count_to_stop] = ise_q; //pi_sh_d;    // for test ----------
    //vse_d_command = mult_r(kpd,(ise_d_command - ise_d)) - mult_r(kpq, ise_q);
    //vse_q_command    =    mult_r(kpq,    ise_d)    +    mult_r(kpd,(ise_q_command    -    ise_q))    -
mult_r(0x7fff, vbus_q);
    // series PI control

    // ************************************************
    //vse_d_command = -450;
    //vse_q_command = -15300;

    sin_vbus = math_sin(degree_vbus+6);
    cos_vbus = math_cos(degree_vbus+6);
    // ************************************************
    // Inverse d-q transform
    //vse_alpha_command = mult_r(vbus_d,sin_vbus) - mult_r(vbus_q,cos_vbus);
    //vse_beta_command = -mult_r(vbus_d,cos_vbus) - mult_r(vbus_q,sin_vbus);
            // The above two lines were used to debug to reproduce the input voltage
```

```
	//vse_d_command = 12000; vbus_q_command = 2500;
	vse_alpha_command		=		mult_r(vse_d_command,sin_vbus)		-
mult_r(vse_q_command,cos_vbus);
	vse_beta_command		=		-mult_r(vse_d_command,cos_vbus)		-
mult_r(vse_q_command,sin_vbus);
	//array_out_2[count_to_stop] = sin_vbus;	// for test ----------
	//array_out_3[count_to_stop] = cos_vbus;	// for test ----------
	// Inverse d-q transform
	// ************************************************

	// ************************************************
	// Inverse alpha-beta transform
	vse_a_command = mult_r(INV_AL_BETA_CO_11,vse_alpha_command);
	//array_out_3[count_to_stop] = vse_a_command;	// for test ----------
	// Inverse alpha-beta transform
	// ************************************************

	// ********** duty cycle update ************
	//duty_cycle_se = 0x0800;	// for open loop test
	duty_cycle_se = 0x0800 + mult_r(0x0800,vse_a_command);
	if (duty_cycle_se > 0x1000) duty_cycle_se = 0x0e1f;
	if (duty_cycle_se < 0) duty_cycle_se = 0x01e0;
	//array_out_4[count_to_stop] = duty_cycle_se;	// for test ----------
	// ********** duty cycle update ************

	// ###########################################################################
	// ********** update variables
	degree_vbus+=12;
	// ********** update variables

	// ###########################################################################
	// ********** for test
	if ((stop == TRUE)) //&&(count_to_stop == MAX_ARRAY_SIZE))
	{
		PESL(PWM_A, PWM_OUTPUT_PAD, PWM_DISABLE);
		PESL(PWM_B, PWM_OUTPUT_PAD, PWM_DISABLE);
		debug = TRUE;
		TimerADCSync_Disable();
		asm(bfset #$0300,sr);
	}

	if ((count_to_stop++)>=MAX_ARRAY_SIZE)
	{
		count_to_stop = 0;
		//PESL(PWM_A, PWM_OUTPUT_PAD, PWM_DISABLE);
		//asm(bfset #$0300,sr);
		//debug = TRUE;
	}

	// ********** Clear interrupt status bit
	PESL(ADC_A, ADC_CLEAR_STATUS_EOSI,NULL);
}

#pragma interrupt saveall
void PWM_1_Reload_Interrupt(void)
{
```

```
    PESL(PWM_A, PWM_WRITE_VALUE_REG_0, duty_cycle_sh1);
    PESL(PWM_A, PWM_WRITE_VALUE_REG_2, duty_cycle_se);

    PESL(PWM_A, PWM_CLEAR_RELOAD_FLAG, NULL);
    PESL(PWM_A, PWM_LOAD_OK, NULL);
}

/*
** ===================================================================
**     Event       :  PWMC1_OnReload (module Events)
**     Parameters  : None
**     Returns     : Nothing
** ===================================================================
*/
#pragma interrupt saveall /* Comment this line if the appropriate 'Interrupt preserve registers' property */
                          /* is set to 'yes' (#pragma interrupt saveall is generated before the ISR) */
void PWM_2_Reload_Interrupt(void)
{
    PESL(PWM_B, PWM_WRITE_VALUE_REG_0, duty_cycle_sh2);
    PESL(PWM_B, PWM_WRITE_VALUE_REG_2, duty_cycle_se);
    PESL(PWM_B, PWM_WRITE_VALUE_REG_4, 0x0400);

    PESL(PWM_B, PWM_CLEAR_RELOAD_FLAG, NULL);
    PESL(PWM_B, PWM_LOAD_OK, NULL);

    //PESL(PWM_B, PWM_OUTPUT_PAD, PWM_DISABLE); // disable PWM
}

/*
** ===================================================================
**     Event       :  Int_IRQA_OnInterrupt (module Events)
**     Parameters  : None
**     Returns     : Nothing
** ===================================================================
*/
#pragma interrupt called /* Comment this line if the appropriate 'Interrupt preserve registers' property */
                         /* is set to 'yes' (#pragma interrupt saveall is generated before the ISR) */
void Int_IRQA_OnInterrupt(void)
{
    stop = TRUE;
}

/*
** ===================================================================
**     Event       :  Int_IRQB_OnInterrupt (module Events)
**     Parameters  : None
**     Returns     : Nothing
** ===================================================================
*/
#pragma interrupt called /* Comment this line if the appropriate 'Interrupt preserve registers' property */
```

```
                                    /* is set to 'yes' (#pragma interrupt saveall is generated before the ISR)
*/
void Int_IRQB_OnInterrupt(void)
{
      ise_q_command = ise_q_command - 20000;
      if (ise_q_command < -20000)
      ise_q_command = -20000;

      // shunt command change positively
      ish1_q_command = ish1_q_command - 3000;
      if (ish1_q_command < -20000)
      ish1_q_command = -20000;
}

/*
** ===================================================================
**      Event           :    Int_GP1_OnInterrupt (module Events)
**      Parameters    : None
**      Returns         : Nothing
** ===================================================================
*/
#pragma interrupt called /* Comment this line if the appropriate 'Interrupt preserve registers'
property */
                                    /* is set to 'yes' (#pragma interrupt saveall is generated before the ISR)
*/
void Int_GP1_OnInterrupt(void)
{
      // series command change positively
      ise_q_command = ise_q_command + 1000;
      if (ise_q_command > 20000)
      ise_q_command = 20000;

      // shunt command change positively
      //ish1_q_command = ish1_q_command + 3000;
      //if (ish1_q_command > 20000)
      //ish1_q_command = 20000;
}

/* END Events */
```

Defined functions to calculate sine and cosine

```
#include "mathlib.h"
#include "mpy.h"

#pragma use_rodata on
const int SinTable[360] =
{
0x0000,0x023D,0x047A,0x06B7,0x08F4,0x0B2F,0x0D6A,0x0FA4,0x11DD,0x1414,0x1649,
0x187D,0x1AAF,0x1CDF,0x1F0C,0x2138,0x2360,0x2586,0x27A9,0x29C8,0x2BE5,0x2DFE,
0x3013,0x3225,0x3432,0x363C,0x3841,0x3A42,0x3C3F,0x3E36,0x4029,0x4217,0x43FF,
0x45E2,0x47C0,0x4998,0x4B6A,0x4D37,0x4EFD,0x50BD,0x5277,0x542A,0x55D7,0x577D,
0x591C,0x5AB5,0x5C46,0x5DCF,0x5F52,0x60CD,0x6240,0x63AC,0x6510,0x666C,0x67C0,
0x690C,0x6A4F,0x6B8A,0x6CBD,0x6DE7,0x6F09,0x7022,0x7132,0x7239,0x7338,0x742D,
0x7519,0x75FC,0x76D6,0x77A6,0x786D,0x792B,0x79DF,0x7A89,0x7B2A,0x7BC2,0x7C4F,
```

```
0x7CD3,0x7D4D,0x7DBD,0x7E24,0x7E80,0x7ED3,0x7F1B,0x7F5A,0x7F8E,0x7FB9,0x7FDA,
0x7FF0,0x7FFD,0x7FFF,0x7FF8,0x7FE6,0x7FCB,0x7FA5,0x7F75,0x7F3C,0x7EF8,0x7EAB,
0x7E53,0x7DF2,0x7D86,0x7D11,0x7C92,0x7C0A,0x7B77,0x7ADB,0x7A35,0x7986,0x78CD,
0x780B,0x773F,0x766A,0x758C,0x74A4,0x73B4,0x72BA,0x71B7,0x70AB,0x6F97,0x6E79,
0x6D53,0x6C25,0x6AEE,0x69AE,0x6867,0x6717,0x65BF,0x645F,0x62F7,0x6188,0x6010,
0x5E92,0x5D0B,0x5B7E,0x59E9,0x584E,0x56AB,0x5502,0x5352,0x519B,0x4FDE,0x4E1B,
0x4C51,0x4A82,0x48AD,0x46D2,0x44F1,0x430B,0x4120,0x3F30,0x3D3B,0x3B41,0x3942,
0x373F,0x3538,0x332C,0x311C,0x2F09,0x2CF2,0x2AD7,0x28B9,0x2698,0x2473,0x224C,
0x2022,0x1DF6,0x1BC7,0x1996,0x1763,0x152F,0x12F8,0x10C0,0x0E87,0x0C4D,0x0A12,
0x07D6,0x0599,0x035C,0x011E,0xFEE2,0xFCA4,0xFA67,0xF82A,0xF5EE,0xF3B3,0xF179,
0xEF40,0xED08,0xEAD1,0xE89D,0xE66A,0xE439,0xE20A,0xDFDE,0xDDB4,0xDB8D,0xD968,
0xD747,0xD529,0xD30E,0xD0F7,0xCEE4,0xCCD4,0xCAC8,0xC8C1,0xC6BE,0xC4BF,0xC2C5,
0xC0D0,0xBEE0,0xBCF5,0xBB0F,0xB92E,0xB753,0xB57E,0xB3AF,0xB1E5,0xB022,0xAE65,
0xACAE,0xAAFE,0xA955,0xA7B2,0xA617,0xA482,0xA2F5,0xA16E,0x9FF0,0x9E78,0x9D09,
0x9BA1,0x9A41,0x98E9,0x9799,0x9652,0x9512,0x93DB,0x92AD,0x9187,0x9069,0x8F55,
0x8E49,0x8D46,0x8C4C,0x8B5C,0x8A74,0x8996,0x88C1,0x87F5,0x8733,0x867A,0x85CB,
0x8525,0x8489,0x83F6,0x836E,0x82EF,0x827A,0x820E,0x81AD,0x8155,0x8108,0x80C4,
0x808B,0x805B,0x8035,0x801A,0x8008,0x8001,0x8003,0x8010,0x8026,0x8047,0x8072,
0x80A6,0x80E5,0x812D,0x8180,0x81DC,0x8243,0x82B3,0x832D,0x83B1,0x843E,0x84D6,
0x8577,0x8621,0x86D5,0x8793,0x885A,0x892A,0x8A04,0x8AE7,0x8BD3,0x8CC8,0x8DC7,
0x8ECE,0x8FDE,0x90F7,0x9219,0x9343,0x9476,0x95B1,0x96F4,0x9840,0x9994,0x9AF0,
0x9C54,0x9DC0,0x9F33,0xA0AE,0xA231,0xA3BA,0xA54B,0xA6E4,0xA883,0xAA29,0xABD6,
0xAD89,0xAF43,0xB103,0xB2C9,0xB496,0xB668,0xB840,0xBA1E,0xBC01,0xBDE9,0xBFD7,
0xC1CA,0xC3C1,0xC5BE,0xC7BF,0xC9C4,0xCBCE,0xCDDB,0xCFED,0xD202,0xD41B,0xD638
,
0xD857,0xDA7A,0xDCA0,0xDEC8,0xE0F4,0xE321,0xE551,0xE783,0xE9B7,0xEBEC,0xEE23,
0xF05C,0xF296,0xF4D1,0xF70C,0xF949,0xFB86,0xFDC3,0x0000
};     // sin function table, x[0,2*pi,360], y[-1,1,360]

const int CosTable[360] =
{
0x7FFF,0x7FFA,0x7FEB,0x7FD2,0x7FAF,0x7F82,0x7F4B,0x7F0A,0x7EBF,0x7E6A,0x7E0B,
0x7DA2,0x7D2F,0x7CB3,0x7C2D,0x7B9D,0x7B03,0x7A60,0x79B3,0x78FC,0x783C,0x7773,
0x76A0,0x75C4,0x74DF,0x73F1,0x72F9,0x71F8,0x70EF,0x6FDD,0x6EC1,0x6D9E,0x6C71,
0x6B3C,0x69FF,0x68B9,0x676C,0x6616,0x64B8,0x6352,0x61E4,0x606F,0x5EF2,0x5D6E,
0x5BE2,0x5A4F,0x58B5,0x5714,0x556D,0x53BE,0x5209,0x504E,0x4E8C,0x4CC4,0x4AF6,
0x4923,0x4749,0x456A,0x4385,0x419C,0x3FAD,0x3DB9,0x3BC0,0x39C2,0x37C0,0x35BA,
0x33AF,0x31A1,0x2F8E,0x2D78,0x2B5E,0x2941,0x2720,0x24FD,0x22D6,0x20AD,0x1E81,
0x1C53,0x1A23,0x17F0,0x15BC,0x1386,0x114F,0x0F16,0x0CDC,0x0AA1,0x0865,0x0628,
0x03EB,0x01AE,0xFF71,0xFD34,0xFAF6,0xF8BA,0xF67D,0xF442,0xF207,0xEFCE,0xED96,
0xEB5F,0xE92A,0xE6F6,0xE4C5,0xE296,0xE069,0xDE3E,0xDC16,0xD9F1,0xD7CF,0xD5B0,
0xD395,0xD17D,0xCF68,0xCD58,0xCB4B,0xC942,0xC73E,0xC53E,0xC343,0xC14D,0xBF5B,
0xBD6F,0xBB88,0xB9A6,0xB7C9,0xB5F3,0xB422,0xB257,0xB092,0xAED4,0xAD1B,0xAB6A,
0xA9BF,0xA81A,0xA67D,0xA4E6,0xA357,0xA1CF,0xA04F,0x9ED5,0x9D64,0x9BFA,0x9A98,
0x993E,0x97EC,0x96A3,0x9561,0x9428,0x92F7,0x91CF,0x90B0,0x8F99,0x8E8B,0x8D86,
0x8C8A,0x8B97,0x8AAD,0x89CD,0x88F5,0x8827,0x8762,0x86A7,0x85F5,0x854D,0x84AF,
0x841A,0x838F,0x830E,0x8296,0x8228,0x81C4,0x816A,0x811A,0x80D4,0x8098,0x8066,
0x803E,0x8020,0x800C,0x8002,0x8002,0x800C,0x8020,0x803E,0x8066,0x8098,0x80D4,
0x811A,0x816A,0x81C4,0x8228,0x8296,0x830E,0x838F,0x841A,0x84AF,0x854D,0x85F5,
0x86A7,0x8762,0x8827,0x88F5,0x89CD,0x8AAD,0x8B97,0x8C8A,0x8D86,0x8E8B,0x8F99,
0x90B0,0x91CF,0x92F7,0x9428,0x9561,0x96A3,0x97EC,0x993E,0x9A98,0x9BFA,0x9D64,
0x9ED5,0xA04F,0xA1CF,0xA357,0xA4E6,0xA67D,0xA81A,0xA9BF,0xAB6A,0xAD1B,0xAED4,
0xB092,0xB257,0xB422,0xB5F3,0xB7C9,0xB9A6,0xBB88,0xBD6F,0xBF5B,0xC14D,0xC343,
0xC53E,0xC73E,0xC942,0xCB4B,0xCD58,0xCF68,0xD17D,0xD395,0xD5B0,0xD7CF,0xD9F1,
0xDC16,0xDE3E,0xE069,0xE296,0xE4C5,0xE6F6,0xE92A,0xEB5F,0xED96,0xEFCE,0xF207,
0xF442,0xF67D,0xF8BA,0xFAF6,0xFD34,0xFF71,0x01AE,0x03EB,0x0628,0x0865,0x0AA1,
```

```
0x0CDC,0x0F16,0x114F,0x1386,0x15BC,0x17F0,0x1A23,0x1C53,0x1E81,0x20AD,0x22D6,
0x24FD,0x2720,0x2941,0x2B5E,0x2D78,0x2F8E,0x31A1,0x33AF,0x35BA,0x37C0,0x39C2,
0x3BC0,0x3DB9,0x3FAD,0x419C,0x4385,0x456A,0x4749,0x4923,0x4AF6,0x4CC4,0x4E8C,
0x504E,0x5209,0x53BE,0x556D,0x5714,0x58B5,0x5A4F,0x5BE2,0x5D6E,0x5EF2,0x606F,
0x61E4,0x6352,0x64B8,0x6616,0x676C,0x68B9,0x69FF,0x6B3C,0x6C71,0x6D9E,0x6EC1,
0x6FDD,0x70EF,0x71F8,0x72F9,0x73F1,0x74DF,0x75C4,0x76A0,0x7773,0x783C,0x78FC,
0x79B3,0x7A60,0x7B03,0x7B9D,0x7C2D,0x7CB3,0x7D2F,0x7DA2,0x7E0B,0x7E6A,0x7EBF,
0x7F0A,0x7F4B,0x7F82,0x7FAF,0x7FD2,0x7FEB,0x7FFA,0x7FFF
};    // Cos Func Table, x[0,2*pi,360], y[-1,1,360]
#pragma use_rodata off

Frac16 math_sin(int degree)
{
      Frac16 result;

      if (degree < 0)
      {
            result = pmemreads((void*)&SinTable[degree+360]);
      }
      else if (degree >= 360)
      {
            result = pmemreads((void*)&SinTable[degree-360]);
      }
      else
      {
            result = pmemreads((void*)&SinTable[degree]);
      }

      return result;
}

Frac16 math_cos(int degree)
{
      Frac16 result;

      if (degree < 0)
      {
            result = pmemreads((void*)&CosTable[degree+360]);
      }
      else if (degree >= 360)
      {
            result = pmemreads((void*)&CosTable[degree-360]);
      }
      else
      {
            result = pmemreads((void*)&CosTable[degree]);
      }

      return result;
}
```

Appendix B. Program to change fraction number into integer format

```
%this program is used to calculate the sine and cosine in 16-bit integal format
theta=linspace(0,pi*2,360);
sin_theta=sin(theta);
FID_sin=fopen('sintable.txt', 'wt');

%*****************************************************************************
for number_of_theta=1:length(theta)
      frac1=sin_theta(number_of_theta;
      bit=[0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0];
      if frac1<0
            bit(1) = 1;
            frac1=frac1*(-1);
      end

      for I=2:16,
            int=frac1/(2^(-(I-1)));
            if int < 1
                  bit(I)=0;
                  continue;
            else
                  bit(I)=1;
                  frac1=frac1-2^(-(I-1));
            end
      end

      %dealwith negative number:
      if bit(1)==1
            for I=2:16
                  if bit(I)==0
                        bit(I)=1;
                  else
                        bit(I)=0;
                  end
            end

            carry=0;
            a=bit(16)+1;
            if a ==2
                  bit(16)=0;
                  carry=1;
            else
                  bit(16)=1;
            end
            I=1;
            if carry == 1
                  for I=0:13
                        a=bit(15-I)+carry;
                        if a==2
                              bit(15-I)=0;
```

```
                carry=1;
            else
                bit(15-I)=1;
                break;
            end
        end
    end
end

out=[bit(1:4); bit(5:8); bit(9:12); bit(13:16)]';
outstr=['0' '0' '0' '0'];
count = 0;
for I=1:4:16,
    count=count+1;
    switch int2str(out(I:I+3))
        case '0   0   0   0'
            outstr(count)='0';
        case '0   0   0   1'
            outstr(count)='1';
        case '0   0   1   0'
            outstr(count)='2';
        case '0   0   1   1'
            outstr(count)='3';
        case '0   1   0   0'
            outstr(count)='4';
        case '0   1   0   1'
            outstr(count)='5';
        case '0   1   1   0'
            outstr(count)='6';
        case '0   1   1   1'
            outstr(count)='7';
        case '1   0   0   0'
            outstr(count)='8';
        case '1   0   0   1'
            outstr(count)='9';
        case '1   0   1   0'
            outstr(count)='A';
        case '1   0   1   1'
            outstr(count)='B';
        case '1   1   0   0'
            outstr(count)='C';
        case '1   1   0   1'
            outstr(count)='D';
        case '1   1   1   0'
            outstr(count)='E';
        case '1   1   1   1'
            outstr(count)='F';
        otherwise
            disp('')
    end
end
fprintf(FID_sin, '0x');
fprintf(FID_sin, outstr);
fprintf(FID_sin, ',');
if ((number_of_theta-floor(number_of_theta/11)*11) ==0)
    fprintf(FID_sin, '\n');
```

```
    end
end
fclose(FID_sin);
cos_theta=cos(theta);
FID_cos=fopen('costable.txt', 'wt');
%*********************************************************************************
for number_of_theta=1:length(theta)
    frac1=cos_theta(number_of_theta);                    %input('Enter a fractional number:');
    bit=[0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0];

    if frac1<0
        bit(1) = 1;
        frac1=frac1*(-1);
    end

    for I=2:16,
        int=frac1/(2^(-(I-1)));
        if int < 1
            bit(I)=0;
            continue;
        else
            bit(I)=1;
            frac1=frac1-2^(-(I-1));
        end
    end

    %dealwith negative number:
    if bit(1)==1
        for I=2:16
            if bit(I)==0
                bit(I)=1;
            else
                bit(I)=0;
            end
        end

        carry=0;
        a=bit(16)+1;
        if a ==2
            bit(16)=0;
            carry=1;
        else
            bit(16)=1;
        end
        I=1;
        if carry == 1
            for I=0:13
                a=bit(15-I)+carry;
                if a==2
                    bit(15-I)=0;
                    carry=1;
                else
                    bit(15-I)=1;
                    break;
                end
            end
```

```
        end
    end
    out=[bit(1:4); bit(5:8); bit(9:12); bit(13:16)]';
    outstr=['0' '0' '0' '0'];
    count = 0;
    for I=1:4:16,
        count=count+1;
        switch int2str(out(I:I+3))
            case '0   0   0   0'
                outstr(count)='0';
            case '0   0   0   1'
                outstr(count)='1';
            case '0   0   1   0'
                outstr(count)='2';
            case '0   0   1   1'
                outstr(count)='3';
            case '0   1   0   0'
                outstr(count)='4';
            case '0   1   0   1'
                outstr(count)='5';
            case '0   1   1   0'
                outstr(count)='6';
            case '0   1   1   1'
                outstr(count)='7';
            case '1   0   0   0'
                outstr(count)='8';
            case '1   0   0   1'
                outstr(count)='9';
            case '1   0   1   0'
                outstr(count)='A';
            case '1   0   1   1'
                outstr(count)='B';
            case '1   1   0   0'
                outstr(count)='C';
            case '1   1   0   1'
                outstr(count)='D';
            case '1   1   1   0'
                outstr(count)='E';
            case '1   1   1   1'
                outstr(count)='F';
            otherwise
                disp('')
        end
    end
    fprintf(FID_cos, '0x');
    fprintf(FID_cos, outstr);
    fprintf(FID_cos, ',');
    if ((number_of_theta-floor(number_of_theta/11)*11) ==0)
        fprintf(FID_sin, '\n');
    end
end
fclose(FID_cos);
```

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